ERODE SENGUNTHAR ENGINEERING COLLEGE

(An Autonomous Institution, Affiliated to Anna University)
PERUNDURAI, ERODE - 638 057

PG Curriculum and Syllabus

(1 to 4 Semesters)

M.E. APPLIED ELECTRONICS

Choice Based Credit System (CBCS)

REGULATION 2019

M.E. APPLIED ELECTRONICS
Minimum credits to be earned : 69

FIRST SEMESTER

Code No	Course	Objective & Outcomes		L	T	P	C	Maximum Marks			Category
		PEOs	POs					CA	ES	Total	
19AE101	Mathematics for Electronic Systems	I,II	1,2,3,4,12	3	1	0	4	40	60	100	BS
19AE102	Advanced Digital System Design	I,II,III	1,2,3,4,5,12	3	1	0	4	40	60	100	PC
19AE103	CMOS VLSI Design	I,II,III	1,3,4,5,12	3	0	0	3	40	60	100	PC
19AE104	Embedded System Design	I,II,III	1,2,4,5,12	3	0	0	3	40	60	100	PC
19AE105	Computational Intelligence Techniques	I,II,III	1,2,12	3	0	0	3	40	60	100	PC
19AE106	System Theory	I,II,III	1,2,3,4,12	3	1	0	4	40	60	100	PC
			PRACTICALS								
19AE107	Real Time Embedded System Laboratory	I,II,III	1,2,3,4,5,12	0	0	4	2	60	40	100	PC
19AE108	Technical Seminar	I,IV	1,2,3,4,9,10	0	0	2	0	60	40	100	EEC
			TOTAL	18	3	6	23	360	440	800	-

SECOND SEMESTER

Code No	Course	Objective & Outcomes		L	T	P	C	Maximum Marks			Category
		PEOs	POs					CA	ES	Total	
19AE201	Advanced Digital Signal Processing	I,II,III	1,2,3,4,5,12	3	1	0	4	40	60	100	PC
19AE202	VLSI Signal Processing	I,II,III	1,2,3,4,5,12	3	1	0	4	40	60	100	PC
19AE203	Low Power VLSI Design	I,II,III	1,2,3,4,12	3	0	0	3	40	60	100	PC
	Professional Elective-I	-	-	3	0	0	3	40	60	100	PE
	Professional Elective-II	-	-	3	0	0	3	40	60	100	PE
	Professional Elective-III	-	-	3	0	0	3	40	60	100	PE

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PRACTICALS											
19AE204	VLSI laboratory	I,II,III	1,2,3,4,5,12	0	0	4	2	60	40	100	PC
			Total	18	2	4	22	300	400	700	-

THIRD SEMESTER

Code No	Course	Objective & Outcomes		L	T	P	C	Maximum Marks			Category
		PEOs	POs					CA	ES	Total	
	Professional Elective-IV	-	-	3	0	0	3	40	60	100	PE
	Professional Elective-V	-	-	3	0	0	3	40	60	100	PE
PRACTICALS											
19AE301	Project Work Phase-I	I,II,III,IV	1,2,3,4,5,6,7,8, 9,10,11,12	0	0	12	6	60	40	100	EEC
			Total	6	0	12	12	140	160	300	-

FOURTH SEMESTER

Code No	Course	Objective & Outcomes		L	T	P	C	Maximum Marks			Category
		PEOs	POs					CA	ES	Total	
19AE401	Project Work Phase-II	I,II,III,IV	1,2,3,4,5,6,7,8, 9,10,11,12	0	0	24	12	60	40	100	EEC
			Total	0	0	24	12	60	40	100	-

ELECTIVES

PROFESSIONAL ELECTIVES							
Code No	Course	Objective & Outcomes		L	T	P	C
		PEOs	POs				
ELECTIVES-I							
19AEX01	Sensors, Actuators and Interface Electronics	I,II,III	1,2,3,4,12	3	0	0	3
19AEX02	Computer Architecture and Parallel Processing	I,II,III	1,2,3,4,12	3	0	0	3
19AEX03	Hardware – Software Co-design	I,II,III	1,2,3,4,12	3	0	0	3
19AEX04	Programmable Logic Controllers	I,II,III	1,2,3,4,12	3	0	0	3
ELECTIVES-II							
19AEX05	CAD for VLSI	I,II,III	1,2,3,4,12	3	0	0	3
19AEX06	ASIC and FPGA Design	I,II,III	1,2,3,4,12	3	0	0	3
19AEX07	System on Chip Design	I,II,III	1,2,3,4,12	3	0	0	3

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19AEX08	Genetic Algorithms	I,II,III	1,2,3,4,12	3	0	0	3
ELECTIVES-III							
19AEX09	Pattern Recognition	I,II,III	1,2,3,4,12	3	0	0	3
19AEX10	Advanced Digital Image Processing	I,II,III	1,2,3,4,5, 12	3	0	0	3
19AEX11	Soft Computing and Optimization Techniques	I,II,III	1,2,3,4,12	3	0	0	3
19AEX12	Synthesis and Optimization of Digital Circuits	I,II,III	1,2,3,4,5, 12	3	0	0	3
ELECTIVES-IV							
19AEX13	Electromagnetic Interference and Compatibility	I,II,III	1,2,3,4,12	3	0	0	3
19AEX14	Nano Electronics	I,II,III	1,2,3,4,12	3	0	0	3
19AEX15	MEMS and NEMS	I,II,III	1,2,3,4,12	3	0	0	3
19AEX16	System Identification and Adaptive Control	I,II,III	1,2,3,4,12	3	0	0	3
ELECTIVES-V							
19AEX17	DSP Architectures and Programming	I,II,III	1,2,3,4,5, 12	3	0	0	3
19AEX18	Speech and Audio Signal Processing	I,II,III	1,2,3,4,5, 12	3	0	0	3
19AEX19	Multimedia Compression Techniques	I,II,III	1,2,3,4,5, 12	3	0	0	3
19AEX20	Wavelet Transforms and its Application	I,II,III	1,2,3,4,12	3	0	0	3

S.No.	Category	I	II	III	IV	Total Credit	Credits in %	Range of Total Credits	
								Min	Max
1	BS	4	-	-	-	4	5.79	5%	10%
2	ES	-	-	-	-	-	-	-	-
3	HS	-	-	-	-	-	-	-	-
4	PC	19	13	-	-	32	46.37	40%	50%
5	PE		9	6	-	15	21.73	20%	25%
6	EEC	-	-	6	12	18	26.08	25%	30%
	Total	23	22	12	12	69	100		

BS- Basic Science

ES-Engineering Science

HSS-Humanities and Social Science

PE- Professional Elective

EEC-Employability Enhancement Course

PC- Professional Core

MC – Mandatory course

CA – Continuous Assessment

ES- End semester Examination

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SEMESTER-I

Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	I
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AE101	MATHEMATICS FOR ELECTRONIC SYSTEMS	3	1	0	4	60	100	

Course Objective (s): The purpose of learning this course is to

- Use computational techniques and algebraic skills essential for the study of matrix theory, Cholesky decomposition
- Algebraic skills essential for the study of Toeplitz matrices and Circulant matrices.
- Construct mathematical arguments that relate to the study of Calculus of variations
- Construct mathematical arguments that relate to the study of Stochastic process
- Compute queuing models and graph theory.

Course Outcomes: At the end of this course, learners will be able to:

- Apply the matrix theory, and calculus of variations
- Critically analyze Calculus of variations
- Critically analyze Stochastic process
- Apply the queuing models in Engineering Applications.
- Apply the graph theory in Engineering Applications.

Unit I	MATRIX THEORY	12

Matrix factorizations – LU decomposition – The Cholesky decomposition – QR factorization – Least squares method – Generalized inverses – Singular value decomposition – Toeplitz matrices and Circulant matrices.

Unit II	GRAPH THEORY	12

Introduction of graphs – Isomorphism – Subgraphs – Walks, paths and circuits – Connected graphs – Eulerian Graphs – Hamiltonian Paths and circuits – Digraph –Some types of digraphs – Connectedness – Adjacency matrix and incidence matrix of graphs – Shortest path algorithms – Dijkstra's algorithm – Warshall's algorithm – Trees – Properties of trees – Spanning trees – Minimal spanning trees – Prim's Algorithm – Kruskal's algorithm.

Unit III	CALCULUS OF VARIATIONS	12

Concept of variation – Euler equation – Variational problems with fixed boundaries – Variational problems involving several unknown functions – Functional involving first and second order derivatives – Functional involving several independent variables – Isoperimetric problems – Direct methods – Ritz method – Kantorowich method.

Unit IV	STOCHASTIC PROCESS	12

Definition – Classification of Stochastic Processes – Markov Chain -Transition Probability Matrices – Chapman Kolmogorov Equations - Classification of States – Continuous Time Markov Chains – Poisson Process - Birth and Death Processes.

Unit V	QUEUING MODELS	12

Markovian queues – Single and Multi-server Models – Little's formula – Machine Interference Model - Non-Markovian Queues – Pollaczek Khintchine Formula.

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REFERENCE(S):	
1.	Richard Bronson Matrix Operation, Schaum's outline series, 2nd Edition, McGraw Hill, 2011.
2.	Sheldon M. Ross Introduction To Probability And Statistics For Engineers And Scientists-Elsevier
3.	Roy D.Yates and David J Goodman, Probability and Stochastic Processes – A friendly Introduction for Electrical and Computer Engineers", John Wiley & Sons, 2005.
4.	Lev Elsgot- Differential Equations and the Calculus of Variations

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Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	I
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AE102	ADVANCED DIGITAL SYSTEM DESIGN	3	1	0	4	60	100	

Course Objective (s): The purpose of learning this course is

- Understand the design procedures of sequential logic design
- Understand the design procedures using VHDL
- Understand the various types of Field Programmable Gate Array
- Understand the methods of fault modeling and simulation
- Understand the fault diagnosis and testability algorithms

Course Outcomes: At the end of this course, learners will be able to:

- Apply the design procedures of sequential logic design
- Describe the design procedures using VHDL
- Discuss the various types of Field Programmable Gate Array
- Describe the various methods of fault modeling and simulation
- Apply the methods of the fault diagnosis and testability algorithms

Unit I	ADVANCED TOPIC IN SEQUENTIAL LOGIC DESIGN	12

ASM Chart – ASM Realization for Synchronous Logic circuit –Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment – Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards.

Unit II	SYSTEM DESIGN USING VHDL	12

VHDL Description of Combinational Circuits – Arrays – VHDL Operators – Compilation and Simulation of VHDL Code – Modeling using VHDL – Flip Flops – Registers - Counters – Sequential Machine – Combinational Logic Circuits – VHDL Code for Serial Adder, Binary Multiplier – Binary Divider – Complete Sequential Systems – Design of a Simple Microprocessor.

Unit III	FIELD PROGRAMMABLE GATE ARRAYS	12

Types of FPGA – XILINX XC3000 series – Logic Cell Array (LCA) – Configurable Logic Blocks (CLB) – Input/ Output Blocks (IOB) – Programmable Interconnection Points (PIP) – XILINX XC4000 Series – Introduction to Xilinx SPARTAN, VIRTEX FPGA – Design examples.

Unit IV	FAULT MODELING AND SIMULATION	12

Introduction to Testing – Faults in digital circuits – Modeling of faults - Logical Fault Models – Fault detection – Fault location – Fault dominance – Logic Simulation – Types of simulation – Delay models – Gate level Event Driven simulation.

Unit V	FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS	12

Fault Table Method – Path Sensitization Method – Boolean Difference Method – D Algorithm – Tolerance Techniques – The Compact Algorithm – Practical PLA's – Fault in PLA – Test Generation – Masking Cycle – DFT Schemes – Built-in Self Test.

REFERENCE(S):

1. Roth Jr. Charles H. Lizy Kurian John, "Digital System Design Using VHDL", 2/e, Cengage learning publication, 2012.
2. Michael L Bushnell, Vishwani D Agrawal, Essentials of Electronic Testing For digital memory and mixed signal VLSI circuit, Kluwer academic Publications, USA, 2014.
3. Nripendra N Biswas ogic Design Theory Prentice Hall of India, 2015.

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4.	Parag K.Lala, An Introduction to Logic Circuit Testing Morgan and Claypool publishers, 2011.
5.	Balabanian, Digital Logic Design Principles, Wiley publication, 2007.
6.	Stephen D Brown, Fundamentals of Digital Logic, TMH publication, 2007.

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Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	I
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AE103	CMOS VLSI DESIGN	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is

- Understand the process of VLSI and Basic CMOS
- Understand the design procedures of CMOS and its characterization
- Understand the performance estimation of CMOS characteristics
- Understand the methods of logic synthesis and simulation
- Understand the methods of system partitioning and routing

Course Outcomes: At the end of this course, learners will be able to:

- Describe the process of VLSI and Basic CMOS
- Design the CMOS circuits
- Discuss the performance estimation of CMOS characteristics
- Describe the methods of logic synthesis and simulation
- Describe the methods of system partitioning and routing

Unit I	VLSI DESIGN PROCESS AND BASIC CMOS	9

Types of ASICs - Design flow -VLSI Design Process – Architectural Design – Logical Design – Physical Design – Layout Styles –Full custom, Semicustom approaches. NMOS and PMOS transistors, Threshold voltage- Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics.

Unit II	INVERTERS, CMOS LOGIC AND CIRCUIT CHARACTERIZATION	9

Basic CMOS technology NMOS and CMOS Inverters - Stick diagram, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads - CMOS logic structures - Transmission gates - Static CMOS design - dynamic CMOS design - Résistance estimation - Capacitance estimation.

Unit III	PERFORMANCE ESTIMATION	9

MOS capacitor characteristics - Device capacitances - Diffusion capacitance - SPICE modeling of MOS capacitance - Routing capacitance - Distributed RC effects - Inductance - Switching characteristics - Rise time - Fall time - Delay time - Empirical delay models - Gate delays - CMOS gate transistor sizing - Power dissipation- Scaling of MOS transistor dimensions.

Unit IV	LOGIC SYNTHESIS AND SIMULATION	9

Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis.

Unit V	SYSTEM PARTITIONING AND ROUTING	9

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow –global routing - detailed routing - special routing - circuit extraction - DRC.

REFERENCE(S):

1. Neil H.E. Weste CMOS VLSI Design: A Circuits and Systems Perspective (For VTU), 3/e, Pearson Education, 2012.
2. Gerez S.H., Algorithms for VLSI Design Automation, John Wiley & Sons, reprint 2018.
3. M.J.S. Smith, Application Specific Integrated Circuits, Pearson Education, 2016.
4. Wolf Wayne, Modern VLSI Design-System on chip Design, Prentice Hall Inc., Third Edition, 2012.

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Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	I
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AE104	EMBEDDED SYSTEM DESIGN	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is

- Understand the design methodology of embedded system
- Understand the characteristics of general and single purpose processor
- Understand the types of Bus structures
- Understand the state machine and concurrent process models
- Understand the embedded software development tools and RTOS

Course Outcomes: At the end of this course, learners will be able to:

- Describe the design methodology of embedded system
- Describe the characteristics of general and single purpose processor
- Discuss the types of Bus structures
- Describe the methods of state machine and concurrent process models
- Apply and debug using embedded software development tools and RTOS.

Unit I	EMBEDDED SYSTEM OVERVIEW	9

Embedded System Overview, Design Challenges – Optimizing Design Metrics, Design Methodology, RT-Level Combinational and Sequential Components, Optimizing Custom Single-Purpose Processors.

Unit II	GENERAL AND SINGLE PURPOSE PROCESSOR	9

Basic Architecture, Pipelining, Superscalar and VLIW architectures, Programmer's view, Development Environment, Application-Specific Instruction-Set Processors (ASIPs) Microcontrollers, Timers, Counters and watchdog Timer, UART, LCD Controllers and Analog-to-Digital Converters, Memory Concepts.

Unit III	BUS STRUCTURES	9

Basic Protocol Concepts, Microprocessor Interfacing – I/O Addressing, Port and Bus-Based I/O, Arbitration, Serial Protocols, I2C, CAN and USB, Parallel Protocols – PCI and ARM Bus, Wireless Protocols – IrDA, Bluetooth, IEEE 802.11.

Unit IV	STATE MACHINE AND CONCURRENT PROCESS MODELS	9

Basic State Machine Model, Finite-State Machine with Datapath Model, Capturing State Machine in Sequential Programming Language, Program-State Machine Model, Concurrent Process Model, Communication among Processes, Synchronization among processes, Dataflow Model, Real-time Systems, Automation: Synthesis, Verification : Hardware/Software Co-Simulation, Reuse: Intellectual Property Cores, Design Process Models.

Unit V	EMBEDDED SOFTWARE DEVELOPMENT TOOLS AND RTOS	9

Compilation Process – Libraries – Porting kernels – C extensions for embedded systems – emulation and debugging techniques – RTOS – System design using RTOS.

REFERENCE(S):

1. Bruce Powel Douglas,Real time UML, second edition: Developing efficient objects for embedded systems, 3rd Edition 2009, Pearson Education.
2. Daniel W. Lewis, Fundamentals of embedded software where C and assembly meet, Pearson Education, 2002.
3. Frank Vahid and Tony Gwargie, Embedded System Design, John Wiley & sons, 2012.
4. Steve Heath, Embedded System Design, Elsevier, Second Edition, 2014.

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Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	I
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AE105	COMPUTATIONAL INTELLIGENCE TECHNIQUES	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is

- Understand the various learning techniques of artificial neural networks
- Understand the basic concepts of fuzzy logic
- Understand the optimization techniques,
- Classify the types of neuro fuzzy modeling
- Knowledge about Applications of neural network.

Course Outcomes: At the end of this course, learners will be able to:

- Describe the various learning techniques of artificial neural networks
- Discuss the basic concepts of fuzzy logic
- Describe the methods of optimization techniques,
- Describe the types of neuro fuzzy modeling
- Gain Knowledge about applications of neural network.

Unit I	ARTIFICIAL NEURAL NETWORKS	9

Introduction to Soft computing – Neural Networks – Model – activation functions – architecture – Supervised learning – Perceptrons – Adaline and Madaline – Back propagation algorithm – Radial Basis Function Networks – Unsupervised Learning and Other Neural Networks – Competitive Learning Networks – Kohonen Self Organizing Networks – Learning Vector Quantization – Hebbian Learning.

Unit II	FUZZY LOGIC	9

Fuzzy Sets – Basic Definition and Terminology – Set theoretic operations – Membership function formulation and parameterization - Extension principle and Fuzzy Relations- Fuzzy if-then Rules – Fuzzy Reasoning – Fuzzy Inference Systems – Mamdani Fuzzy Models –Sugeno Fuzzy Models –Tsukamoto Fuzzy Models – Input Space Partitioning - Fuzzy Modeling.

Unit III	OPTIMIZATION TECHNIQUES	9

Derivative based Optimization: Descent Methods –The Method of steepest Descent – Classical Newton's Method – Step Size Determination – Derivative free Optimization: Genetic Algorithms – Simulated Annealing – Particle swarm Optimization - Ant colony optimization.

Unit IV	NEURO FUZZY MODELING	9

Adaptive Neuro Fuzzy Inference Systems – Architecture – Hybrid learning Algorithm –learning methods that Cross-fertilize ANFIS and RBFN – Coactive Neuro fuzzy Modeling – Framework – Neuron Functions for Adaptive Networks – Neuro Fuzzy spectrum.

Unit V	APPLICATIONS	9

Printed Character Recognition – Inverse kinematics Problem – Applications of soft computing techniques for power electronics: MPPT, speed control for electrical machines, harmonic elimination techniques in power converters.

REFERENCE(S):

1. J.S.R Jang, C.T.Sun and E.Mizutani, Neuro-Fuzzy and Soft Computing, PHI, Pearson Education, 2014.
2. Laurene V. Fausett, Fundamentals of Neural Networks: Architectures, Algorithms and Applications, Pearson Education, III Edition, 2010.

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3.	Timothy J. Ross, Fuzzy Logic with Engineering Applications Wiley India.
4.	David E.Goldberg, Genetic Algorithms: Search, Optimization and Machine Learning, Addison Wesley, New York, 2008.

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Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	I
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AE106	SYSTEM THEORY	3	1	0	4	60	100	

Course Objective (s): The purpose of learning this course is

- Understand the basics of digital control system
- Understand the methods of z-pane analysis of Discrete- time control systems
- Understand the state space analysis, state feedback control and stability analysis
- Understand the state feedback control
- Understand the stability analysis

Course Outcomes: At the end of this course, learners will be able to:

- Describe the basics of digital control system
- Discuss the various types of fuzzy models
- Analyze state space,
- Analyze state feedback control
- Define the effect of stability

Unit I	INTRODUCTION TO DIGITAL CONTROL SYSTEM	12

Elements of Digital control system- Classifications of discrete time signals – Time domain models for discrete time systems. Sampling and reconstruction of signals –Frequency domain representation of sampling theorem-Nyquist rate, Aliasing. Mathematical model of sample and hold circuits-Practical aspects of choice of sampling rate.

Unit II	Z-PLANE ANALYSIS OF DISCRETE-TIME CONTROL SYSTEMS	12

Review of Z transform- Relationship between s plane and z plane - Difference equation representation of discrete time system-Pulse transfer function -Modified Z transform- Digital PID controllers– Zeigler – Nichols tuning method

Unit III	STATE SPACE ANALYSIS AND ITS SOLUTION	12

Review of state space representation- Conversion of continuous state model to discrete state model – State diagram-Solution of discrete time state model: autonomous, non-autonomous systems – State transition matrix –Controllability and observability – Multi variable discrete systems.

Unit IV	STATE FEEDBACK CONTROL	12

Design of state feedback controller – Design of reduced and full order observers – Steady state error in state space-PI feedback- Digital compensator design– Digital filter properties– Kalman's filter.

Unit V	STABILITY ANALYSIS	12

BIBO stability-Effect of sampling rate on stability-Jury's stability test-Root Locus analysis –Asymptotic stability-Liapunov Stability Analysis of discrete time systems: Linear and Non-linear systems- Direct, Indirect method-Construction of Liapunov energy function.

REFERENCE(S):

1. Gopal, M., Digital Control and State Variable Methods, 4th edition, Tata McGraw-Hill, New Delhi, 2012.
2. Kuo, B.C., Digital Control Systems, 2nd edition Oxford University Press, Oxford, 2007.
3. Ogata, K., Discrete Time Control Systems, second edition Prentice Hall, New Jersey, 2011.
4. M.Sami Fadali, Antonio Visioli, Digital control Engineering Analysis and design Elsevier, 2012.

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Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	I
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AE107	REAL TIME EMBEDDED SYSTEMS LABORATORY	0	0	4	2	45	100	

Course Objective (s): The purpose of learning this course is

- Learn to program in PIC Microcontroller
- Learn to interface with I2C communication
- Study the DSP Processor
- Learn to Interface with PIC Microcontroller
- Learn Stepper Motor Interfacing

Course Outcomes: At the end of this course, learners will be able to:

- Understand the Program logic in PIC
- Understand the Program Logic in Embedded based Communication
- Gain knowledge about the DSP Processors
- Programming to Interface with PIC Microcontroller
- Programming to Interface Stepper Motor

Exp No.	Name of Experiments
1	RS232C Bus Interfacing with PIC Microcontroller
2	LED and Switch Interfacing with Embedded PIC Microcontroller
3	LED interfacing with Embedded PIC Microcontroller
4	LED and Key matrix Interfacing with Embedded PIC Microcontroller
5	EEPROM Interfacing with Embedded PIC Microcontroller (I2C-Communication)
6	LCD Interfacing with Embedded PIC Microcontroller
7	Rolling Display in LCD /LED using Embedded PIC Microcontroller
8	Stepper Motor Interfacing with Embedded PIC Microcontroller
9	ADC Interfacing with Embedded PIC Microcontroller(I2C-Communication)
10	RTC interfacing with Embedded PIC Microcontroller(I2C-Communication)
11	Study of Convolution Algorithm Implementation using DSP Processor
12	Study of Matrix Multiplication using DSP Processor

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Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	I
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AE108	TECHNICAL SEMINAR	0	0	2	0	30	100	

Course Objective: In this course, students will develop their scientific and technical reading and writing skills that they need to understand and construct research articles. A term paper requires a student to obtain information from a variety of sources (i.e. Journals, dictionaries, reference books) and then place it in logically developed ideas.

TECHNICAL SEMINAR **30**

The work involves the following steps:

- Selecting a subject, narrowing the subject into a topic
- Stating an objective.
- Collecting the relevant bibliography (at least 15 journal papers)
- Preparing a working outline.
- Studying the papers and understanding the authors contributions and critically analyzing each paper.
- Preparing a working outline
- Linking the papers and preparing a draft of the paper.
- Preparing conclusions based on the reading of all the papers.
- Writing the Final Paper and giving final Presentation

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SEMESTER-II

Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	II
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AE201	ADVANCED DIGITAL SIGNAL PROCESSING	3	1	0	4	60	100	

Course Objective (s): The purpose of learning this course is to

- Understand the discrete random signal processing
- Update with important filters and algorithms.
- Familiar with digital filter banks.
- Analyze the Uniform and two channel filter banks
- Understand Sparse Signal Processing

Course Outcomes: At the end of this course, learners will be able to:

- Familiar with the stationary process.
- Apply the various filters for signal processing
- Describe with noise cancellation filtering method
- Apply Uniform and two Channel filter banks
- Apply Sparse signal Processing

Unit I	DISCRETE RANDOM SIGNAL PROCESSING	12

Discrete time random process - Random process: Ensemble averages- Gaussian process – Stationary process - The auto covariance and autocorrelation matrices – White noise - power spectrum. Parseval's theorem - Wiener Khintchine relation- Filtering random process - Spectral factorization.

Unit II	FILTERS	12

The FIR Wiener filter - Filtering - Linear prediction - IIR Wiener Filter - Non causal IIR Wiener filter - Causal IIR Wiener filter. Adaptive Filter: Concepts of adaptive filter - FIR adaptive filter - LMS algorithm.

Unit III	MULTIRATE DIGITAL SIGNAL PROCESSING	12

Mathematical description of sampling rate – Interpolation and Decimation by integer factor – Sampling rate conversion by rational factor- Filter design for sampling rate conversion - Direct form FIR structures, Polyphase structures. Multistage implementation of sampling rate conversion.

Unit IV	UNIFORM AND TWO CHANNEL FILTER BANKS AND APPLICATIONS OF DSP	12

Digital Filter Banks – Two -channel Quadrature Mirror Filter Bank – M-Channel QMF Bank. Applications: Noise cancellation using adaptive filtering technique, Sub band coding of speech signals, Design of decimation and interpolation filters.

Unit V	SPARSE SIGNAL PROCESSING	12

Sparse Signal Representation- Introduction-Sparse signals-Compressible signal-Over complete dictionaries-Coherence between the bases-Compressed sensing and signal reconstruction- Sensing in the presence of noise-Restricted isometry property.

REFERENCE(S):

1. Hayes, Monson H. Statistical Digital Signal processing and Modeling, John Wiley and Sons, Inc., 2011
2. Proakis, John G. and Manolakis, Dimitris G. Digital Signal Processing: Principles Algorithms and Applications, PHI, 2008

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Dept.of ECE - ESEC

3.	Ifeachor, Emmanuel C. and Jervis, Barrie N. Digital Signal Processing: A Practical Approach, Addison-Wesley Publishing Company, 2012
4.	Dionitris G. Manolakis, Vinay K. Ingle, Stepen M. Kogon, Statistical & Adaptive signal processing, spectral estimation, signal modeling, Adaptive filtering & Array processing, McGraw-Hill International edition 2000.
5.	K.P.Soman R.Ramanathan, Digital Signal and Image Processing –The Sparse Way, Elseveir Publisher,2012.

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Programme	APPLIED ELECTRONICS					R 2019	Semester	II
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AE202	VLSI SIGNAL PROCESSING	3	1	0	4	60	100	

Course Objective (s): The purpose of learning this course is to

- Introduce techniques for altering the existing DSP structures to suit VLSI implementations
- Introduce efficient design of DSP architectures suitable for VLSI
- Understand the folding and fast Convolution
- Understand Algorithmic Strength Reduction
- Understand the Pipelined and parallel recursive filters

Course Outcomes: At the end of this course, learners will be able to:

- Modify the existing or new DSP structures suitable for VLSI.
- Efficient design of DSP architectures.
- Perform folding and fast Convolution
- Perform Algorithmic Strength Reduction
- Design Pipelined recursive filters

Unit I	INTRODUCTION TO DSP SYSTEMS	12

Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Algorithms For Computing Iteration Bound, Iteration Bound of Multirate Data Flow Graphs. Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power.

Unit II	RETIMING AND UNFOLDING	12

Retiming - definitions and properties Retiming techniques; Solving systems of inequalities, Retiming Techniques. Unfolding – an algorithm for Unfolding, properties of unfolding, Critical path Unfolding and Retiming applications of Unfolding- sample period reduction and parallel processing application.

Unit III	FOLDING AND FAST CONVOLUTION	12

Folding – Folding transformation – Register minimizing techniques –Register minimization in folded architectures-Folding of Multirate systems. Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm – Wino grad Algorithm, Modified Wino grad Algorithm -Design of Fast Convolution algorithm by inspection.

Unit IV	ALGORITHMIC STRENGTH REDUCTION	12

Algorithmic strength reduction in Filters-Parallel FIR Filters, DCT and Inverse DCT, Parallel architectures for rank order Filters.

Unit V	PIPELINED AND PARALLEL RECURSIVE FILTERS ADAPTIVE FILTERS	12

Inefficient/efficient single channel interleaving, Look- Ahead pipelining in first- order IIR filters, Look-Ahead pipelining with power-of-two decomposition parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters-relaxed look-ahead, pipelined LMS adaptive filter.

REFERENCE(S):

1. Parhi, Keshab K., VLSI Digital Signal Processing Systems, Design and Implementation, John Wiley, Inter Science, New York, 2008.
2. Isamail, Mohammed and Fiez, Terri, Analog VLSI Signal and Information Processing, McGraw-Hill, New York, 2009

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3.	www.pdf-search-engine.com/vlsi-signal-processing-pdf.html
4.	Magdy A. Bayoumi, Magdy A. Bayoumi, E. Swartzlander, VLSI Signal Processing Technology, Kluwer Academic Publishers.October 1994
5.	Ray Liu K J, High Performance VLSI Signal Processing, Innovative architectures and Algorithms, IEEE Press,2008

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Dept.of ECE - ESEC

Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	II
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AE203	LOW POWER VLSI DESIGN	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is to

- Identify the power reduction techniques based on technology independent and technology dependent.
- Power dissipation mechanism in various MOS logic style.
- Identify suitable techniques to reduce the power dissipation.
- Gain Knowledge about Power Estimation
- Understand Synthesis and software design for low power

Course Objective (s): The purpose of learning this course is to

- Identify the power reduction techniques based on technology independent.
- Identify the power reduction techniques based on technology dependent.
- Power dissipation mechanism in various MOS logic style.
- Identify suitable techniques to reduce the power dissipation.
- Perform the Synthesis and Software for Low power Circuits

Unit I	POWER DISSIPATION IN CMOS	9

Hierarchy of limits of power – Sources of power consumption – Physics of power dissipation in CMOS FET devices – Long Channel and Submicron Effect-Basic principle of low power design.

Unit II	POWER OPTIMIZATION	9

Logic level power optimization – Circuit level low power design – circuit techniques for reducing power consumption in adders and multipliers.

Unit III	DESIGN OF LOW POWER CMOS CIRCUITS	9

Computer arithmetic techniques for low power system – reducing power consumption in memories – low power clock, Inter connect and layout design – Advanced techniques –Special techniques.

Unit IV	POWER ESTIMATION	9

Power Estimation techniques – logic power estimation –Simulation power analysis–Probabilistic power analysis.

Unit V	SYNTHESIS AND SOFTWARE DESIGN FOR LOW POWER	9

Synthesis for low power – Behavioral level transform – software design for low power.

REFERENCE(S):

1. Kaushik Roy and S.C.Prasad, Low power CMOS VLSI circuit design, Wiley, 2007.
2. Dimitrios Soudris, Chirstian Pignet, Costas Goutis, Designing CMOS Circuits for Low Power, Kluwer, 2010.
3. J.B.Kulo and J.H Lou, Low voltage CMOS VLSI Circuits, Wiley 2001
4. A.P.Chandrasekaran and R.W.Broadersen, Low power digital CMOS design, Kluwer,2010
5. Gary Yeap, Practical low power digital VLSI design, Kluwer, 2008.
6. Abdelatif Belaouar, Mohamed.I.Elmasry, Low power digital VLSI design, Kluwer, 2005.
7. James B.Kulo, Shih-Chia Lin, Low voltage SOI CMOS VLSI devices and Circuits, John Wiley and sons, inc. 2009.

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Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	II
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AE204	VLSI LABORATORY	0	0	2	2	45	100	

Course Objective (s): The purpose of learning this course is to

- Design and simulation of digital circuits VHDL and Verilog
- Design FIR Filters.
- Design Real time clock using VHDL
- Design Neural Network Algorithms using MATLAB
- Design Genetic Algorithms using MATLAB

Course Outcomes: At the end of this course, learners will be able to:

- Simulation of Digital Circuits using Verilog
- Simulation of Digital Circuits using VHDL
- FPGA implementation of ALU and RTC
- FPGA implementation of FIR Filters.
- FPGA implementation of FFT Computation.

Exp No.	Name of Experiments
1	Design and Simulation of Combinational and sequential circuits using VHDL.
2	Design and Simulation of Combinational and sequential circuits using Verilog.
3	FPGA Implementation of FFT Computation
4	FPGA Implementation of FIR Filter (Low, High and Band pass)
5	FPGA Implementation of 4 Bit ALU & Power analysis.
6	FPGA Implementation of Real Time Clock & RTL view.
7	FPGA Implementation of Adaptive Signal Processing Algorithm
8	Implementation of Image Processing Algorithm using MATLAB.
9	Implementation of Neural networks Algorithms using MATLAB.
10	Implementation of Genetic Algorithm and PSO using MATLAB.

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ELECTIVE-I

Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	II
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AEX01	SENSORS, ACTUATORS AND INTERFACE ELECTRONICS	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is to

- Study the concepts of Measurement Systems, Resistive And Reactive Sensors
- Study the concepts of Self-Generating Sensors,
- Study Actuators Drive Characteristics and Applications &
- Study Digital Sensors and Semiconductor Device Sensors

Course Outcomes: At the end of this course, learners will be able to:

- Gain Knowledge of Measurement Systems, Resistive and Reactive Sensors
- Gain Knowledge of Self-Generating Sensors,
- Gain Knowledge of Actuators Drive Characteristics and Applications &
- Gain Knowledge of Digital Sensors and Semiconductor Device Sensors

Unit I	INTRODUCTION TO MEASUREMENT SYSTEMS	9

Introduction to measurement systems: general concepts and terminology, measurement systems, sensor classification, general input-output configuration, methods of correction, performance characteristics: static characteristics of measurement systems, accuracy, precision, sensitivity, other characteristics: linearity, resolution, systematic errors, random errors, dynamic characteristics of measurement systems: zero-order, first-order, and second-order measurement systems and response.

Unit II	RESISTIVE AND REACTIVE SENSORS	9

Resistive sensors: potentiometers, strain gages, resistive temperature detectors, magneto resistors, light-dependent resistors, Signal conditioning for resistive sensors: Wheatstone bridge, sensor bridge calibration and compensation, Instrumentation amplifiers, sources of interference and interference reduction, Reactance variation and electromagnetic sensors, capacitive sensors, differential, inductive sensors, linear variable differential transformers (LVDT), magneto elastic sensors, hall effect sensors, Signal conditioning for reactance-based sensors & application to the LVDT.

Unit III	SELF-GENERATING SENSORS	9

Self-generating sensors: thermoelectric sensors, piezoelectric sensors, pyroelectric sensors, photovoltaic sensors, electrochemical sensors, Signal conditioning for self-generating sensors: chopper and low-drift amplifiers, offset and drifts amplifiers, electrometer amplifiers, charge amplifiers, noise in amplifiers.

Unit IV	ACTUATORS DRIVE CHARACTERISTICS AND APPLICATIONS	9

Relays, Solenoid drive, Stepper Motors, Voice-Coil actuators, Servo Motors, DC motors and motor control, 4-to-20 mA Drive, Hydraulic actuators, variable transformers: synchros, resolvers, Inductosyn, resolver-to-digital and digital-to-resolver converters.

Unit V	DIGITAL SENSORS AND SEMICONDUCTOR DEVICE SENSORS	9

Digital sensors: position encoders, variable frequency sensors – quartz digital thermometer, vibrating wire strain gages, vibrating cylinder sensors, saw sensors, digital flow meters, Sensors based on semiconductor junctions: thermometers based on semiconductor junctions, magneto diodes and magneto transistors,

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photodiodes and phototransistors, sensors based on MOSFET transistors, CCD imaging sensors , ultrasonic sensors, fiber-optic sensors.	
REFERENCE(S):	
1.	Andrzej M. Pawlak Sensors and Actuators in Mechatronics Design and Applications, 2016.
2.	D. Johnson, Process Control Instrumentation Technology, John Wiley and Sons.
3.	D.Patranabis, Sensors and Transducers, TMH 2013.
4.	E.O. Doeblin,Measurement System : Applications and Design, McGraw Hill publications
5.	Graham Brooker, Introduction to Sensors for ranging and imaging, Yesdee, 2009.

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Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	II
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AEX02	COMPUTER ARCHITECTURE AND PARALLEL PROCESSING	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is to

- Concepts of Computer Design And Performance Measures, Parallel Processing, Pipelining and ILP
- Concepts of Memory Hierarchy Design, Multiprocessors & Multi-Core Architectures

Course Outcomes: At the end of this course, learners will be able to:

- Knowledge of Computer Design And Performance Measures, Parallel Processing, Pipelining and ILP
- Gain Knowledge of Memory Hierarchy Design, Multiprocessors & Multi-Core Architectures

Unit I	COMPUTER DESIGN AND PERFORMANCE MEASURES	9

Fundamentals of Computer Design – Parallel and Scalable Architectures – Multiprocessors –Multi-vector and SIMD architectures – Multithreaded architectures – Stanford Dash multiprocessor – KSR1 - Data-flow architectures - Performance Measures.

Unit II	PARALLEL PROCESSING, PIPELINING AND ILP	9

Instruction Level Parallelism and Its Exploitation - Concepts and Challenges - Pipelining processors - Overcoming Data Hazards with Dynamic Scheduling – Dynamic Branch Prediction - Speculation - Multiple Issue Processors - Performance and Efficiency in Advanced Multiple Issue Processors.

Unit III	MEMORY HIERARCHY DESIGN	9

Memory Hierarchy - Memory Technology and Optimizations – Cache memory – Optimizations of Cache Performance – Memory Protection and Virtual Memory - Design of Memory Hierarchies.

Unit IV	MULTIPROCESSORS	9

Symmetric and distributed shared memory architectures – Cache coherence issues – Performance Issues – Synchronization issues – Models of Memory Consistency - Interconnection networks – Buses, crossbar and multi-stage switches.

Unit V	MULTI-CORE ARCHITECTURES	9

Software and hardware multithreading – SMT and CMP architectures – Design issues – Case-studies – Intel Multi-core architecture – SUN CMP architecture – IBM cell architecture – hp architecture.

REFERENCE(S):

1.	David E. Culler, Jaswinder Pal Singh, Parallel Computing Architecture: A hardware/ software approach, Morgan Kaufmann / Elsevier, 2007.
2.	Dimitrios Soudris, Axel Jantsch, Scalable Multi-core Architectures: Design Methodologies and Tools, Springer, 2012.
3.	Hwang Briggs, Computer Architecture and parallel processing, McGraw Hill, 2004.
4.	John L. Hennessey and David A. Patterson, Computer Architecture – A quantitative approach, Morgan Kaufmann / Elsevier, 4th. edition, 2017
5.	John P. Hayes, Computer Architecture and Organization, McGraw Hill
6.	John P. Shen, Modern processor design. Fundamentals of super scalar processors, Tata McGraw Hill 2003

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Dept.of ECE - ESEC

Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	II
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AEX03	HARDWARE - SOFTWARE CO-DESIGN	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is to

- Study the concepts of System Specification And Modelling, Hardware / Software Partitioning
- Study the concepts of Hardware / Software Co-Synthesis, Prototyping And Emulation, Design Specification And Verification

Course Outcomes: At the end of this course, learners will be able to:

- Gain Knowledge of System Specification and Modelling, Hardware / Software Partitioning
- Gain Knowledge of Hardware / Software Co-Synthesis, Prototyping And Emulation, Design Specification and Verification

Unit I	SYSTEM SPECIFICATION AND MODELLING	9

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling , Co-Design for Heterogeneous Implementation - Single-Processor Architectures with one ASIC and many ASICs, Multi-Processor Architectures, Comparison of Co- Design Approaches, Models of Computation, Requirements for Embedded System Specification.

Unit II	HARDWARE / SOFTWARE PARTITIONING	9

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization, HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms.

Unit III	HARDWARE / SOFTWARE CO-SYNTHESIS	9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Co-Synthesis Algorithm for Distributed System- Case Studies with any one application.

Unit IV	PROTOTYPING AND EMULATION	9

Introduction, Prototyping and Emulation Techniques , Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping ,Target Architecture- Architecture Specialization Techniques , System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems ,Mixed Systems and Less Specialized Systems.

Unit V	DESIGN SPECIFICATION AND VERIFICATION	9

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification ,Languages for System-Level Specification and Design System-Level Specification ,Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co-simulation.

REFERENCE(S):

1. Giovanni De Micheli, Rolf Ernst Morgon, Reading in Hardware/Software Co-Design, Kaufmann Publishers,2011.
2. Jorgen Staunstrup, Wayne Wolf,Hardware/Software Co-Design: Principles and Practice, Kluwer Academic Pub,2007.
3. Ralf Nieman, Hardware/Software Co-Design for Data Flow Dominated Embedded Systems, Kluwer Academic Pub, 2008.

Chairman - BoS
Dept.of ECE - ESEC

Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	II
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AEX04	PROGRAMMABLE LOGIC CONTROLLERS	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is to

- Study the concepts of Programmable Logic Controller, Basic PLC Programming
- Study the concepts of Advanced PLC Programming, PLC Installation and Troubleshooting & PLC Communication and its Applications

Course Outcomes: At the end of this course, learners will be able to:

- Gain Knowledge of Programmable Logic Controller, Basic PLC Programming
- Gain Knowledge of Advanced PLC Programming, PLC Installation and Troubleshooting & PLC Communication and its Applications

Unit I	Introduction to Programmable Logic Controller	9

Overview of Programmable Logic Controller - Parts of a PLC – Principles of operation - modifying the operation - PLC vs Computer - PLC Size and applications - I/O Modules: Discrete, Analog, Special – I/O Specifications – CPU – Memory design and types – Programming devices – Recording and Retrieving data – PLC Workstations

Unit II	Basic PLC Programming	9

Fundamentals of Logic – Processor Memory Organization – Program Scan – PLC programming languages – Relay-Type Instructions - Instruction addressing – Branch and Internal relay instructions – Entering the Ladder diagram – Electromagnetic Control relays – Contactors – Motor Starters – Manual operated switches and Mechanically operated switches

Unit III	Advanced PLC Programming	9

Programming Timers – Programming Counters – Program Control Instructions – Data Manipulation Instructions – Math Instructions – Sequencer and Shift Register Instructions.

Unit IV	PLC Installation and Troubleshooting	9

PLC Enclosures – Electrical Noise – Leaky Inputs and Outputs – Grounding – Voltage Variations and Surges – Program Editing – Programming and Monitoring – Preventive Maintenance – Connecting PC and PLC – Process Control: Types of processes – structure of control system – Controllers – Data Acquisition Systems

Unit V	PLC Communication and its Applications	9

Computer Fundamentals – Computer-Integrated Manufacturing – Data Communications – Computer numeric control – Robotics - PLC Applications: Bottle filling system – pneumatic stamping system – material handling system – PLC in Individual process – Continuous process – Container filling system – liquid heating system.

REFERENCE(S):

1. Frank D. Petruzella, Programmable Logic Controllers" Tata McGraw-Hill Edition, New Delhi,2010
2. Webb John W and Reis Ronald A., Programmable Logic Controllers, Prentice Hall Publications, New Delhi, 2015
3. Bolton W, Programmable Logic Controllers, ELSEVIER , New York, 2016
4. Rockwell Automation, Logix 5000 Controllers – system reference

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ELECTIVE-II

Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	II
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AEX05	CAD FOR VLSI	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is to

- Study the concepts of VLSI Design Flow, Layout, Placement And Partitioning
- Study the concepts of Floor Planning And Routing, Simulation And Logic Synthesis & High Level Synthesis

Course Outcomes: At the end of this course, learners will be able to:

- Gain Knowledge of VLSI Design Flow, Layout, Placement And Partitioning
- Gain Knowledge of Floor Planning And Routing, Simulation And Logic Synthesis & High Level Synthesis

Unit I	INTRODUCTION TO VLSI DESIGN FLOW	9

Introduction to VLSI Design methodologies, Basics of VLSI design automation tools, Algorithmic Graph Theory and Computational Complexity, Tractable and Intractable problems, General purpose methods for combinatorial optimization.

Unit II	LAYOUT, PLACEMENT AND PARTITIONING	9

Layout Compaction, Design rules, Problem formulation, Algorithms for constraint graph compaction, Placement and partitioning, Circuit representation, Placement algorithms, Partitioning.

Unit III	FLOOR PLANNING AND ROUTING	9

Floor planning concepts, Shape functions and floorplan sizing, Types of local routing problems, Area routing, Channel routing, Global routing, Algorithms for global routing.

Unit IV	SIMULATION AND LOGIC SYNTHESIS	9

Simulation, Gate-level modeling and simulation, Switch-level modeling and simulation, Combinational Logic Synthesis, Binary Decision Diagrams, Two Level Logic Synthesis.

Unit V	HIGH LEVEL SYNTHESIS	9

Hardware models for high level synthesis, internal representation, allocation, assignment and scheduling, scheduling algorithms, Assignment problem, High level transformations.

REFERENCE(S):

1. N.A. Sherwani,Algorithms for VLSI Physical Design Automation, Kluwer Academic Publishers, 2008.
2. S.H. Gerez, Algorithms for VLSI Design Automation, John Wiley & Sons, 2012.
3. Sadiq M. Sait, Habib Youssef, VLSI Physical Design automation: Theory and Practice, World scientific 2016.
4. Steven M.Rubin, Computer Aids for VLSI Design, Addison Wesley Publishing 2001.

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Dept.of ECE - ESEC

Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	II
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AEX06	ASIC AND FPGA DESIGN	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is to

- Study the concepts of Overview Of ASIC And PID, ASIC Physical Design
- Study the concepts of Logic Synthesis, Simulation And Testing, Field Programmable Gate Arrays & SOC Design

Course Outcomes: At the end of this course, learners will be able to:

- Gain Knowledge of Overview Of ASIC And PID, ASIC Physical Design
- Gain Knowledge of Logic Synthesis, Simulation And Testing, Field Programmable Gate Arrays & SOC Design

Unit I	OVERVIEW OF ASIC AND PLD	9

Types of ASICs - Design flow – CAD tools used in ASIC Design – Programming Technologies: Antifuse – static RAM – EPROM and EEPROM technology, Programmable Logic Devices: ROMs and EPROMs – PLA –PAL. Gate Arrays – CPLDs and FPGAs.

Unit II	ASIC PHYSICAL DESIGN	9

System partition -partitioning - partitioning methods – interconnect delay models and measurement of delay - floor planning - placement – Routing: global routing - detailed routing - special routing - circuit extraction - DRC.

Unit III	LOGIC SYNTHESIS, SIMULATION AND TESTING	9

Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation. Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

Unit IV	FIELD PROGRAMMABLE GATE ARRAYS	9

FPGA Design : FPGA Physical Design Tools -Technology mapping - Placement & routing - Register transfer (RT)/Logic Synthesis - Controller/Data path synthesis - Logic minimization.

Unit V	SOC DESIGN	9

System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures. High performance algorithms for ASICs/ SoCs as case studies: Canonical Signed Digit Arithmetic, Knowledge Crunching Machine, Distributed Arithmetic, High performance digital filters for sigma-delta ADC.

REFERENCE(S):

1.	David A.Hodges, Analysis and Design of Digital Integrated Circuits (3/e), MGH 2014
2.	H.Gerez, Algorithms for VLSI Design Automation, John Wiley, 2001
3.	Jan. M. Rabaey et al, Digital Integrated Circuit Design Perspective (2/e), PHI 2007
4.	M.J.S. Smith : Application Specific Integrated Circuits, Pearson, 2013
5.	J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley& Sons, Newyork.
6.	P.K.Chan& S. Mourad, Digital Design using Field Programmable Gate Array, Prentice Hall.
7.	Sudeep Pasricha and NikilDutt, On-Chip Communication Architectures System on Chip Interconnect, Elsevier, 2008

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Dept.of ECE - ES

Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	II
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AEX07	SYSTEM ON CHIP DESIGN	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is to

- Study the concepts of Introduction to System On Chip Design, System On Chip Design
- Study the concepts of Hardware Software Co-Design, Synthesis & SOC Verification and Testing

Course Outcomes: At the end of this course, learners will be able to:

- Gain Knowledge of System On Chip Design, System On Chip Design
- Gain Knowledge of Hardware Software Co-Design, Synthesis & SOC Verification and Testing

Unit I	INTRODUCTION	9

Introduction to SoC Design, system level design, methodologies and tools, system hardware: IO, communication, processing units, memories; operating systems: prediction of execution, real time scheduling, embedded OS, middle ware; Platform based SoC design, multiprocessor SoC and Network on Chip, Low power SoC Design

Unit II	SYSTEM LEVEL MODELLING	9

SystemC: overview, Data types, modules, notion of time, dynamic process, basic channels, structure communication, ports and interfaces, Design with examples.

Unit III	HARDWARE SOFTWARE CO-DESIGN	9

Analysis, partitioning, high level optimizations, real-time scheduling, hardware acceleration, voltage scaling and power management; Virtual platform models, co-simulation and FPGAs for prototyping of HW/SW systems.

Unit IV	SYNTHESIS	9

System synthesis: Transaction Level Modeling (TLM) based design, automatic TLM generation and mapping, platform synthesis; software synthesis: code generation, multi task synthesis, internal and external communication; Hardware synthesis: RTL architecture, Input models, estimation and optimization, resource sharing and pipelining and scheduling.

Unit V	SOC VERIFICATION AND TESTING	9

SoC and IP integration, Verification: Verification technology options, verification methodology, overview: system level verification, physical verification, hardware/software co-verification; Test requirements and methodologies, SoC design for testability - System modeling, test power dissipation, test access mechanism.

REFERENCE(S):

1.	D. Black, J. Donovan, SystemC: From the Ground Up, Springer, 2014.
2.	D. Gajski, S. Abdi, A. Gerstlauer, G. Schirner, Embedded System Design: Modeling, Synthesis, Verification, Springer, 2009.
3.	Erik Larson, Introduction to advanced system-on-chip test design and optimisation, Springer 2009.
4.	Grotker, T., Liao, S., Martin, G. & Swan, S. System design with System C, Springer, 2011.
5.	Ghenassia, F. Transaction-level modeling with SystemC: TLM concepts and applications for embedded systems, Springer, 2010.
6.	Hoi-junyoo, Kangmin Lee, Jun Kyoungkim,Low power NoC for high performance SoCdesing,CRC press
7.	M. L. Bushnell and V.D. Agrawal, Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits, Springer, 2009.

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Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	II
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AEX08	GENETIC ALGORITHMS	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is to

- Study the concepts of Introduction to Genetic Algorithm, GA Operators
- Study the concepts of Applications Of GA , Introduction To Genetics-Based Machine Learning & Applications Of Genetics-Based Machine Learning

Course Outcomes: At the end of this course, learners will be able to:

- Gain Knowledge of Introduction to Genetic Algorithm, GA Operators
- Gain Knowledge of Applications Of GA , Introduction To Genetics-Based Machine Learning & Applications Of Genetics-Based Machine Learning

Unit I	INTRODUCTION TO GENETIC ALGORITHM	9

Introduction to Genetic Algorithm – Robustness of Traditional Optimization and Search methods – Goals of optimization-GA versus Traditional methods – Simple GA – GA at work –Similarity templates (Schemata) – Learning the lingo - **Mathematical foundations:** The fundamental theorem - Schema processing at work. – The 2-armed & k-armed Bandit problem. –The building Block Hypothesis. – Minimal deceptive problem.

Unit II	GA OPERATORS	9

Data structures – Reproduction- Roulette-wheel Selection – Boltzman Selection – Tournament Selection- Rank Selection – Steady –state selection –Crossover mutation – A time to reproduce, a time to cross. – Get with the Main program. – How well does it work. – Mapping objective functions to fitness forum. – Fitness scaling. Coding – A Multi parameter, Mapped, Fixed – point coding – Discretization – constraints.

Unit III	APPLICATIONS OF GA	9

The rise of GA – GA application of Historical Interaction. – Dejung & Function optimization – Current applications of GA - **Advanced operators & techniques in genetic search** :Dominance, Diploidy & abeyance – Inversion & other reordering operators. – other mine-operators – Niche & Speciation – Multi objective optimization – Knowledge-Based Techniques. – GA & parallel processes – Real life problem

Unit IV	INTRODUCTION TO GENETICS-BASED MACHINE LEARNING	9

Genetics – Based Machine learning – Classifier system – Rule & Message system – Apportionment of credit: The bucket brigade – Genetic Algorithm – A simple classifier system in Pascal. – Results using the simple classifier system

Unit V	APPLICATIONS OF GENETICS-BASED MACHINE LEARNING	9

The Rise of GBMC – Development of CS-1, the first classifier system. – Smitch's Poker player. – Other Early GBMC efforts. –Current Applications.

REFERENCE(S):

1. David E. Gold Berg, Genetic Algorithms in Search, Optimization & Machine Learning, Pearson Education, 2011
2. S.Rajasekaran, G.A.Vijayalakshmi Pai, Neural Networks, Fuzzy Logic and Genetic Algorithms , PHI , 2003 (Chapters 8 and 9)
3. Kalyanmoy Deb, Optimization for Engineering Design, algorithms and examples, PHI 2005

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ELECTIVE-III

Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	II
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AEX09	PATTERN RECOGNITION	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is to

- Study the concepts of Pattern Classifier, Unsupervised Classification
- Study the concepts of Structural Pattern Recognition, Feature Extraction And Selection & Recent Advances

Course Outcomes: At the end of this course, learners will be able to:

- Gain Knowledge of Pattern Classifier, Unsupervised Classification
- Gain Knowledge of Structural Pattern Recognition, Feature Extraction And Selection & Recent Advances

Unit I	PATTERN CLASSIFIER	9

Overview of pattern recognition -Discriminant functions-Supervised learning –Parametric estimation-Maximum likelihood estimation –Bayesian parameter estimation- Perceptron algorithm-LMSE algorithm – Problems with Bayes approach –Pattern classification by distance functions-Minimum distance pattern classifier.

Unit II	UNSUPERVISED CLASSIFICATION	9

Clustering for unsupervised learning and classification - Clustering concept-C-means algorithm-Hierarchical clustering procedures- Graph theoretic approach to pattern clustering - Validity of clustering solutions.

Unit III	STRUCTURAL PATTERN RECOGNITION	9

Elements of formal grammars-String generation as pattern description - recognition of syntactic description-Parsing-Stochastic grammars and applications - Graph based structural representation.

Unit IV	FEATURE EXTRACTION AND SELECTION	9

Entropy minimization – Karhunen - Loeve transformation-feature selection through functions approximation-Binary feature selection.

Unit V	RECENT ADVANCES	9

Neural network structures for Pattern Recognition –Neural network based Pattern associators-Unsupervised learning in neural Pattern Recognition-Self organizing networks-Fuzzy logic-Fuzzy classifiers-Pattern classification using Genetic Algorithms.

REFERENCE(S):

1. R.O Duda, P.E Hart and Stork, Pattern Classification, Wiley, 2012.
2. Robert J. Sehalkoff, Pattern Recognition: Statistical, Structural and Neural Approaches, John Wiley & Sons Inc., 2010.
3. Tou & Gonzales, Pattern Recognition Principles, Wesley Publication Company, 2008.
4. Morton Nadier and P. Eric Smith, Pattern Recognition Engineering, John Wiley & Sons, 2006.
5. IEEE Transaction on Pattern Recognition Technique, 2016.
6. IEEE Engineering Medicine and Biology Magazine, 2006.

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Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	II
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AEX10	ADVANCED DIGITAL IMAGE PROCESSING	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is to

- Study the concepts of Fundamentals Of Digital Image Processing, Color Image Processing
- Study the concepts of Morphological Image Processing, Segmentation, Representation And Description & Object Recognition And Image Processing Applications

Course Outcomes: At the end of this course, learners will be able to:

- Gain Knowledge of Fundamentals Of Digital Image Processing, Color Image Processing
- Gain Knowledge of Morphological Image Processing, Segmentation, Representation And Description & Object Recognition And Image Processing Applications

Unit I	FUNDAMENTALS OF DIGITAL IMAGE PROCESSING	9

Elements of Visual Perception- Image acquisition, digitization- Histogram - Image enhancement – Spatial filters for smoothing and sharpening – Discrete 2D transforms - DFT, DCT, Walsh-Hadamard, Slant, KL, Wavelet Transform – Haar wavelet.

Unit II	COLOR IMAGE PROCESSSING	9

Color Image Fundamentals-Color Models- RGB, CMY, CMYK and HSI Color Models- Pseudocolor Image Processing - Intensity Slicing- Intensity to Color transformations -Basics of Color Image Processing- Color Transformation - Color Image Smoothing and Sharpening- Color Segmentation - Noise in Color Images.

Unit III	MORPHOLOGICAL IMAGE PROCESSING	9

Preliminaries- Basic Concepts from Set Theory-Logic Operations Involving Binary Images -Dilation and Erosion –Opening and Closing - Hit-or-Miss Transformation - Basic Morphological Algorithms -Boundary Extraction- Region Filling- Extraction of Connected Components- Convex Hull- Thinning-Thickening- Skeletons- Pruning- - Gray-Scale Morphology.

Unit IV	SEGMENTATION, REPRESENTATION AND DESCRIPTION	9

Edge Detection - Edge Linking and Boundary Detection -Thresholding- Segmentation by Morphological Watershed Segmentation Algorithm - Use of Markers- Representation and Boundary Descriptors.

Unit V	OBJECT RECOGNITION AND IMAGE PROCESSING APPLICATIONS	9

Patterns and Pattern Classes -Recognition Based on Decision-Theoretic Methods –Matching- Optimum Statistical Classifiers- Neural Networks, Fuzzy Systems - GA. Image compression- JPEG, JPEG2000 JBIG standards - Watermarking - Steganography.

REFERENCE(S):

1. Rafael C. Gonzalez, Digital Image Processing, Pearson Education, Inc., 3rd Edition, 2008.
2. Milman Sonka, Vaclav Hlavac, Roger Boyle, Image Processing, Analysis and Machine Vision, Brooks/Cloe, Vikas Publishing House 2nd Edition, 2001.
3. Khalid Sayood, Data Compression, Morgan Kaufmann Publishers (Elsevier)., 3rd Edition, 2016.
4. Rafael C. Gonzalez, Richards E.Woods, Steven Eddins, Digital Image Processing using MATLAB, Pearson Education, Inc., 2014.

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Programme	ME-APPLIED ELECTRONICS				R 2019	Semester	II
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks
		L	T	P	C		
19AEX11	SOFT COMPUTING AND OPTIMIZATION TECHNIQUES	3	0	0	3	45	100

Course Objective (s): The purpose of learning this course is to

- Study the concepts of Neural Networks, Fuzzy Logic
- Study the concepts of Neuro-Fuzzy Modeling, Conventional Optimization Techniques & Evolutionary Optimization Techniques

Course Outcomes: At the end of this course, learners will be able to:

- Gain Knowledge of Neural Networks, Fuzzy Logic
- Gain Knowledge of Neuro-Fuzzy Modeling, Conventional Optimization Techniques & Evolutionary Optimization Techniques

Unit I	NEURAL NETWORKS	9

Machine Learning using Neural Network, Learning algorithms, Supervised Learning Neural Networks – Feed Forward Networks, Radial Basis Function, Unsupervised Learning Neural Networks – Self Organizing map , Adaptive Resonance Architectures, Hopfield network.

Unit II	FUZZY LOGIC	9

Fuzzy Sets – Operations on Fuzzy Sets – Fuzzy Relations – Membership Functions-Fuzzy Rules and Fuzzy Reasoning – Fuzzy Inference Systems – Fuzzy Expert Systems – Fuzzy Decision Making.

Unit III	NEURO-FUZZY MODELING	9

Adaptive Neuro-Fuzzy Inference Systems – Coactive Neuro-Fuzzy Modeling – Classification and Regression Trees – Data Clustering Algorithms – Rule base Structure Identification –Neuro-Fuzzy Control – Case Studies.

Unit IV	CONVENTIONAL OPTIMIZATION TECHNIQUES	9

Introduction to optimization techniques, Statement of an optimization problem, classification, Unconstrained optimization-gradient search method-Gradient of a function, steepest gradient-conjugate gradient, Newton's Method, Marquardt Method, Constrained optimization –sequential linear programming, Interior penalty function method, external penalty function method.

Unit V	EVOLUTIONARY OPTIMIZATION TECHNIQUES	9

Genetic algorithm - working principle, Basic operators and Terminologies, Building block hypothesis, Travelling Salesman Problem, Particle swam optimization, Ant colony optimization.

REFERENCE(S):

1. David E. Goldberg, Genetic Algorithms in Search, Optimization and Machine Learning, Addison wesley, 2009.
2. George J. Klir and Bo Yuan, Fuzzy Sets and Fuzzy Logic-Theory and Applications,Prentice Hall, 2010.
3. James A. Freeman and David M. Skapura, Neural Networks Algorithms, Applications, and Programming Techniques, Pearson Edn., 2008.
4. Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, Neuro-Fuzzy and Soft Computing, Prentice-Hall of India, 2006.
5. Mitchell Melanie, An Introduction to Genetic Algorithm, Prentice Hall, 2001.

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Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	II
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AEX12	SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is to

- Study the concepts of Circuits And Hardware Modeling, Architectural Level Synthesis And Optimization
- Study the concepts of Scheduling Algorithms And Resource Sharing, Logic-Level Synthesis And Optimization & Sequential Logic Optimization

Course Outcomes: At the end of this course, learners will be able to:

- Gain Knowledge of Circuits And Hardware Modeling, Architectural Level Synthesis And Optimization
- Gain Knowledge of Scheduling Algorithms And Resource Sharing, Logic-Level Synthesis And Optimization & Sequential Logic Optimization

Unit I	CIRCUITS AND HARDWARE MODELING	9

Design of Microelectronic Circuits - Computer Aided Synthesis and optimization-Combinatorial optimization-Boolean Algebra and Application-Hardware Modeling Languages –Compilation and Behavioral optimization.

Unit II	ARCHITECTURAL LEVEL SYNTHESIS AND OPTIMIZATION	9

Fundamental Architectural synthesis Problems- Area and performance Estimation-Control unit synthesis-Synthesis of pipelined circuits.

Unit III	SCHEDULING ALGORITHMS AND RESOURCE SHARING	9

Unconstrained Scheduling-ASAP Algorithm-ALAP Scheduling Algorithm- Scheduling with Resource Constraints- Scheduling pipelined circuits-Sharing and binding for Dominated circuits-Area Binding-Concurrent Binding –Module selection problems-Structural testability.

Unit IV	LOGIC-LEVEL SYNTHESIS AND OPTIMIZATION	9

Logic optimization Principles-Algorithms and Logic Minimization –Encoding problems- Multiple-level optimization of logic networks-Algebraic and Boolean model-Algorithm for delay Evaluation-Rule based logic optimization

Unit V	SEQUENTIAL LOGIC OPTIMIZATION	9

Sequential circuit -State Encoding-Minimization methods-Retiming- Finite state machine-testability for synchronous circuits-Algorithm for library binding- Look-Up table - FPGA- Rule-based library binding.

REFERENCE(S):

1. Giovanni De Micheli, Synthesis and optimization of Digital Circuits, Tata McGraw-Hill, 2007. .
2. John Paul Shen, Mikko H. Lipasti, Modern processor Design, Tata McGraw Hill, 2003
3. Gary D. Hachtel and Fabio Somenzi, Logic Synthesis and Verification Algorithms, Springer
4. Frank Vahid, Digital Design, John Wiley & Sons

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ELECTIVE-IV

Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	III
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AEX13	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is to

- Study the concepts of EMI Environment, EMI Coupling Principles
- Study the concepts of EMI/EMC Standards And Measurements, EMI Control Techniques & EMC Design Of PCBs

Course Outcomes: At the end of this course, learners will be able to:

- Gain Knowledge of EMI Environment, EMI Coupling Principles
- Gain Knowledge of EMI/EMC Standards And Measurements, EMI Control Techniques & EMC Design Of PCBs

Unit I	EMI ENVIRONMENT	9

EMI/EMC concepts and definitions, Sources of EMI, conducted and radiated EMI, Transient EMI, Time domain Vs Frequency domain EMI, Units of measurement parameters, Emission and immunity concepts, ESD.

Unit II	EMI COUPLING PRINCIPLES	9

Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling, Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near Field Cable to Cable Coupling, Power Mains and Power Supply coupling.

Unit III	EMI/EMC STANDARDS AND MEASUREMENTS	9

Civilian standards - FCC, CISPR,I EC, EN, Military standards - MIL STD 461D/462, EMI Test Instruments /Systems, EMI Shielded Chamber, Open Area Test Site, TEM Cell, Sensors/Injectors/Couplers, Test beds for ESD and EFT, Military Test Method and Procedures (462).

Unit IV	EMI CONTROL TECHNIQUES	9

Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting.

Unit V	EMC DESIGN OF PCBS	9

PCB Traces Cross Talk, Impedance Control, Power Distribution Decoupling, Zoning, Motherboard Designs and Propagation Delay Performance Models.

REFERENCE(S):

1. Ott, Henry W., Noise Reduction Techniques in Electronic Systems, John Wiley & Sons, New York, 2002
2. Paul, C.R., Introduction to Electromagnetic Compatibility, John Wiley & Sons, New York, 2010
3. Kodali, V.P., Engineering EMC Principles, Measurements and Technologies, IEEE Press, London, 2006.
4. Keiser, Bernhard., Principles of Electromagnetic Compatibility, Third Edition, Artech House, Dedham, 2000

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Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	III
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AEX14	NANO ELECTRONICS	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is to

- Study the concepts of Introduction to Nanoelectronics, Fabrication And Measurement Techniques
- Study the concepts of Properties of Nanoelectronics, Nano Structure Devices & Logic Devices And Applications

Course Outcomes: At the end of this course, learners will be able to:

- Gain Knowledge of Introduction to Nanoelectronics, Fabrication And Measurement Techniques
- Gain Knowledge of Properties of Nanoelectronics, Nano Structure Devices & Logic Devices And Applications

Unit I	INTRODUCTION TO NANOELECTRONICS	9

Microelectronics towards bio molecule electronics-Particles and waves- Wave-particle duality- Wave mechanics- Schrodinger wave equation- Wave mechanics of particles: - Atoms and atomic orbitals- Materials for nano electronics- Semiconductors- Crystal lattices: Bonding in crystals- Electron energy bands- Semiconductor hetero structures- Lattice-matched and pseudo morphic hetero structures- Inorganic-organic hetero structures- Carbon nano materials: nano tubes and fullerenes.

Unit II	FABRICATION AND MEASUREMENT TECHNIQUES	9

Growth, fabrication, and measurement techniques for nanostructures- Bulk crystal and hetero structure growth- Nanolithography, etching, and other means for fabrication of nanostructures and nano devices- Techniques for characterization of nanostructures- Spontaneous formation and ordering of nanostructures- Clusters and nano crystals- Methods of nano tube growth- Chemical and biological methods for nanoscale fabrication- Fabrication of nano-electromechanical systems.

Unit III	PROPERTIES	9

Dielectrics-Ferroelectrics-Electronic Properties and Quantum Effects-Magneto electronics –Magnetism and Magneto transport in Layered Structures-Organic Molecules – Electronic Structures, Properties, and Reactions-Neurons – The Molecular Basis of their Electrical Excitability-Circuit and System Design- Analysis by Diffraction and Fluorescence Methods-Scanning Probe Techniques

Unit IV	NANO STRUCTURE DEVICES	9

Electron transport in semiconductors and nanostructures- Time and length scales of the electrons in solids- Statistics of the electrons in solids and nanostructures- Density of states of electrons in nanostructures- Electron transport in nanostructures-Electrons in traditional low-dimensional structures- Electrons in quantum wells- Electrons in quantum wires- Electrons in quantum dots- Nanostructure devices- Resonant-tunneling diodes- Field-effect transistors- Single-electron-transfer devices- Potential-effect transistors- Light-emitting diodes and lasers- Nano-electromechanical system devices- Quantum-dot cellular automata.

Unit V	LOGIC DEVICES AND APPLICATIONS	9

Logic Devices-Silicon MOSFETs-Ferroelectric Field Effect Transistors-Quantum Transport Devices Based on Resonant Tunneling-Single-Electron Devices for Logic Applications-Superconductor Digital Electronics-Quantum Computing Using Superconductors-Carbon Nanotubes for Data Processing- Molecular Electronics.

REFERENCE(S):

1. Vladimir V. Mitin, Viatcheslav A. Kochelap, Michael A. Stroscio, Introduction to Nanoelectronics: Science, Nanotechnology, Engineering, and Applications, Cambridge University Press 2011

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2.	Supriyo Datta,Lessons from Nanoelectronics: A New Perspective on Transport, World Scientific 2012
3.	George W. Hanson,Fundamentals of Nanoelectronics, Pearson 2009
4.	Korkin, Anatoli; Rosei, Federico (Eds.), Nanoelectronics and Photonics, Springer 2008
5.	Mircea Dragoman, Daniela Dragoman, Nanoelectronics: principles and devices, CRC Press 2006
6.	Karl Goser, Peter Glosekotter, Jan Dienstuhl,Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices, Springer 2004
7.	W. R. Fahrner, Nanotechnology and Nan electronics: Materials, Devices, Measurement Techniques (SpringerVerlag Berlin Heidelberg 2005)

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Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	III
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AEX15	MEMS AND NEMS	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is to

- Study the concepts of Overview Of MEMS And NEMS, MEMS Fabrication Technologies
- Study the concepts of Micro Sensors, Micro Actuators & Nano systems And Quantum Mechanics

Course Outcomes: At the end of this course, learners will be able to:

- Gain Knowledge of Overview Of MEMS And NEMS, MEMS Fabrication Technologies
- Gain Knowledge of Micro Sensors, Micro Actuators & Nano systems And Quantum Mechanics

Unit I	OVERVIEW	9

New trends in Engineering and Science: Micro and Nanoscale systems, Introduction to Design of MEMS and NEMS, MEMS and NEMS – Applications, Devices and structures. Materials for MEMS: Silicon, silicon compounds, polymers, metals.

Unit II	MEMS FABRICATION TECHNOLOGIES	9

Microsystem fabrication processes: Photolithography, Ion Implantation, Diffusion, Oxidation. Thin film depositions: LPCVD, Sputtering, Evaporation, Electroplating; Etching techniques: Dry and wet etching, electrochemical etching; Micromachining: Bulk Micromachining, Surface Micromachining, High Aspect- Ratio (LIGA and LIGA-like) Technology; Packaging: Microsystems packaging, Essential packaging technologies, Selection of packaging materials.

Unit III	MICRO SENSORS	9

MEMS Sensors: Design of Acoustic wave sensors, resonant sensor, Vibratory gyroscope, Capacitive and Piezo Resistive Pressure sensors-engineering mechanics behind these Microsensors. Case study: Piezo-resistive pressure sensor.

Unit IV	MICRO ACTUATORS	9

Design of Actuators: Actuation using thermal forces, Actuation using shape memory Alloys, Actuation using piezoelectric crystals, Actuation using Electrostatic forces (Parallel plate, Torsion bar, Comb drive actuators), Micromechanical Motors and pumps. Case study: Comb drive actuators.

Unit V	NANOSYSTEMS AND QUANTUM MECHANICS	9

Atomic Structures and Quantum Mechanics, Molecular and Nanostructure Dynamics: Schrodinger Equation and Wave function Theory, Density Functional Theory, Nanostructures and Molecular Dynamics, Electromagnetic Fields and their quantization, Molecular Wires and Molecular Circuits.

REFERENCE(S):

1. Chang Liu, Foundations of MEMS, Pearson education India limited, 2006.
2. Marc Madou, Fundamentals of Microfabrication, CRC press 2004.
3. Stephen D. Senturia, Micro system Design, Kluwer Academic Publishers,2001.
4. Sergey Edward Lyshevski, MEMS and NEMS: Systems, Devices, and Structures CRC Press, 2002.
5. Tai Ran Hsu ,MEMS and Microsystems Design and Manufacture ,Tata McGraw Hill, 2002.

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Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	III
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AEX16	SYSTEM IDENTIFICATION AND ADAPTIVE CONTROL	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is to

- Study the concepts of System Identification, Recursive methods and Closed Loop Identification
- Study the concepts of State Estimation, Adaptive Control Schemes & Applications of Adaptive Control

Course Outcomes: At the end of this course, learners will be able to:

- Gain Knowledge of System Identification, Recursive methods and Closed Loop Identification
- Gain Knowledge of State Estimation, Adaptive Control Schemes & Applications of Adaptive Control

Unit I	System Identification	9

Introduction: Dynamic systems, Models for Linear Time-invariant Systems, Time varying systems and nonlinear systems, The system identification procedure. Non-parametric methods- Transient analysis, Frequency analysis, Correlation analysis and Spectral analysis. Parametric methods: Least Square- Prediction error method -Maximum Likelihood – Instrumental Variable methods

Unit II	Recursive methods and Closed Loop Identification	9

Recursive methods: Recursive least squares method- The recursive prediction error method -Recursive instrumental variable method- Input signal design for identification. Identification of systems operating in closed loop: Identifiability considerations – Direct and indirect identification – Joint input / output identification.

Unit III	State Estimation	9

Linear Optimal State Estimation: Kalman filter - Stability Analysis Non-Linear State Estimation: Extended Kalman filter – Bucy filter Adaptive Strate Estimation: Parameter Identification via Extented Kalman filter

Unit IV	Adaptive Control Schemes	9

Internal Model Control (IMC) schemes: Known parameters -Adaptive Internal Model Control schemes – Stability and robustness analysis. Robust adaptive control: Problem formulation - Ordinary direct adaptive control with dead zone – New robust direct adaptive control - Robust adaptive control with least prior knowledge. Indirect adaptive periodic control: Problem formulation – Adaptive control scheme and control law.

Unit V	Applications of Adaptive Control	9

Optimal adaptive tracking for nonlinear systems: Problem statement – Adaptive tracking – adaptive back stepping – Inverse concepts – Design of strict feedback system. Adaptive inverse for actuator compensation: Plants with actuator non-linearities – Parameterized inverses – State feedback designs– Output feedback inverse control and designs – Designs for multivariable systems and non-linear dynamics. Stable MIMO adaptive fuzzy/ neural control.

REFERENCE(S):

1. Torsten Soderstrom T and Petre Stoica, "System Identification, Prentice Hall International, Second Edition, London, 2001.
2. Gang Feng and Rogelio Lozano, Adaptive Control Systems, Newnes publisher, First Edition, Jordan Hill, 2009.

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3.	Lennart Ljung, System Identification: Theory for the User, Prentice-Hall, Second Edition, New Jersey, USA, 1999.
4.	Karl J.Astrom and Bjorn Wittenmark, Adaptive Control, Pearson Education, Second Edition, New Delhi, 2003.
5.	Eveleigh,V.W. Adaptive Control and optimization Techniques, Tata McGraw Hill Newyork,2007.

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Programme	ME-APPLIED ELECTRONICS				R 2019	Semester	III
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks
		L	T	P	C		
19AEX17	DSP ARCHITECTURES AND PROGRAMMING	3	0	0	3	45	100

Course Objective (s): The purpose of learning this course is to

- Study the concepts of Fundamentals Of Programmable DSPs, Special Functions
- Study the concepts of Linear Programming, Algebraic Equations & Ordinary Differential Equations

Course Outcomes: At the end of this course, learners will be able to:

- Understand of Fundamentals Of Programmable DSPs, Special Functions
- Understand of Linear Programming, Algebraic Equations & Ordinary Differential Equations

Unit I	FUNDAMENTALS OF PROGRAMMABLE DSPs	9

Multiplier and Multiplier accumulator – Modified Bus Structures and Memory access in PDSPs – Multiple access memory – Multi-port memory – VLIW architecture- Pipelining – Special Addressing modes in P-DSPs – On chip Peripherals.

Unit II	SPECIAL FUNCTIONS	9

Architecture – Assembly language syntax - Addressing modes – Assembly language Instructions - Pipeline structure, Operation – Block Diagram of DSP starter kit – Application Programs for processing real time signals.

Unit III	LINEAR PROGRAMMING	9

Architecture of the C6x Processor - Instruction Set - DSP Development System: Introduction – DSP Starter Kit Support Tools- Code Composer Studio - Support Files - Programming Examples to Test the DSK Tools – Application Programs for processing real time signals.

Unit IV	ALGEBRAIC EQUATIONS	9

Architecture of ADSP-21XX and ADSP-210XX series of DSP processors- Addressing modes and assembly language instructions – Application programs –Filter design, FFT calculation.

Unit V	ORDINARY DIFFERENTIAL EQUATIONS	9

Architecture of TMS320C54X: Pipe line operation, Code Composer studio – Architecture of TMS320C6X - Architecture of Motorola DSP563XX – Comparison of the features of DSP family processors.

REFERENCE(S):

1. Avtar Singh and S. Srinivasan, Digital Signal Processing – Implementations using DSP Microprocessors with Examples from TMS320C54xx, cengage Learning India Private Limited, Delhi 2012
2. B.Venkataramani and M.Bhaskar, Digital Signal Processors – Architecture, Programming and Applications – Tata McGraw – Hill Publishing Company Limited. New Delhi, 2003.
3. RulphChassaing, Digital Signal Processing and Applications with the C6713 and C6416 DSK, A JOHN WILEY & SONS, INC., PUBLICATION, 2015
4. User guides Texas Instrumentation, Analog Devices, Motorola.

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Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	III
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AEX18	SPEECH AND AUDIO SIGNAL PROCESSING	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is to

- Study basic concepts of processing speech and audio signals
- Study and analyze various M-band filter-banks for audio coding
- Understand audio coding based on transform coders.
- Study time and frequency domain speech processing methods

Course Outcomes: At the end of this course, learners will be able to:

- Evaluate audio coding and transform coders
- Discuss time and frequency domain methods for speech processing
- Explain predictive analysis of speech

Unit I	MECHANICS OF SPEECH AND AUDIO	9

Introduction - Review of Signal Processing Theory-Speech production mechanism – Nature of Speech signal – Discrete time modelling of Speech production – Classification of Speech sounds – Phones – Phonemes – Phonetic and Phonemic alphabets – Articulatory features. Absolute Threshold of Hearing - Critical Bands-Simultaneous Masking, Masking-Asymmetry, and the Spread of Masking- Non-simultaneous Masking - Perceptual Entropy - Basic measuring philosophy -Subjective versus objective perceptual testing - The perceptual audio quality measure (PAQM) - Cognitive effects in judging audio quality.

Unit II	TIME-FREQUENCY ANALYSIS: FILTER BANKS AND TRANSFORMS	9

Introduction - Analysis-Synthesis Framework for M-band Filter Banks- Filter Banks for Audio Coding: Design Considerations - Quadrature Mirror and Conjugate Quadrature Filters - Tree-Structured QMF and CQF M-band Banks - Cosine Modulated "Pseudo QMF" M-band Banks -Cosine Modulated Perfect Reconstruction (PR) M-band Banks and the Modified Discrete Cosine Transform (MDCT) - Discrete Fourier and Discrete Cosine Transform - Pre-echo Distortion- Pre-echo Control Strategies

Unit III	AUDIO CODING AND TRANSFORM CODERS	9

Lossless Audio Coding – Lossy Audio Coding - ISO-MPEG-1A, 2A, 2A-Advaned, 4A Audio Coding - Optimum Coding in the Frequency Domain - Perceptual Transform Coder –Brandenburg - Johnston Hybrid Coder - CNET Coders - Adaptive Spectral Entropy Coding –Differential Perceptual Audio Coder - DFT Noise Substitution -DCT with Vector Quantization -MDCT with Vector Quantization

Unit IV	TIME AND FREQUENCY DOMAIN METHODS FOR SPEECH PROCESSING	9

Time domain parameters of Speech signal – Methods for extracting the parameters :Energy, Average Magnitude – Zero crossing Rate – Silence Discrimination using ZCR and energy Short Time Fourier analysis – Formant extraction – Pitch Extraction using time and frequency domain methods Homomorphic Speech Analysis: Cepstral analysis of Speech – Formant and Pitch Estimation – Homomorphic Vocoders

Unit V	PREDICTIVE ANALYSIS OF SPEECH	9

Formulation of Linear Prediction problem in Time Domain – Basic Principle – Auto correlation method – Covariance method – Solution of LPC equations – Cholesky method – Durbin"s Recursive algorithm – lattice formation and solutions – Comparison of different methods – Application of LPC parameters – Pitch detection using LPC parameters – Formant analysis – VELP – CELP

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REFERENCE(S):	
1.	B.Gold and N.Morgan, Speech and Audio Signal Processing, Wiley and Sons, 2018.
2.	L.R.Rabiner and R.W.Schaffer, Digital Processing of Speech Signals, Prentice Hall, 2002.
3.	Mark Kahrs, Karlheinz Brandenburg, Kluwer Applications of Digital Signal Processing to Audio And Acoustics, Academic Publishers,
4.	Udo Zölzer, Digital Audio Signal Processing, Second Edition A John Wiley& sons Ltd

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Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	III
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AEX21	MULTIMEDIA COMPRESSION TECHNIQUES	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is to

- To understand the basic ideas of compression algorithms related to multimedia components – Text, speech, audio, image and Video.
- To understand the principles and standards and their applications with an emphasis on underlying technologies, algorithms, and performance.
- To appreciate the use of compression in multimedia processing applications
- To understand and implement compression standards in detail.

Course Outcomes:

- Implement basic compression algorithms with MATLAB and its equivalent open source environments.
- Design and implement some basic compression standards
- Critically analyze different approaches of compression algorithms in multimedia related mini projects.

Unit I	FUNDAMENTALS OF COMPRESSION	9

Introduction To multimedia – Graphics, Image and Video representations – Fundamental concepts of video, digital audio – Storage requirements of multimedia applications – Need for compression – Taxonomy of compression Algorithms - Elements of Information Theory – Error Free Compression – Lossy Compression.

Unit II	TEXT COMPRESSION	9

Huffman coding – Adaptive Huffman coding – Arithmetic coding – Shannon-Fano coding – Dictionary techniques – LZW family algorithms.

Unit III	IMAGE COMPRESSION	9

Image Compression: Fundamentals — Compression Standards – JPEG Standard – Sub-band coding – Wavelet Based compression – Implementation using Filters – EZW, SPIHT coders – JPEG 2000 standards – JBIG and JBIG2 standards.

Unit IV	AUDIO COMPRESSION	9

Audio compression Techniques – law, A-Law companding – Frequency domain and filtering – Basic sub-band coding – Application to speech coding – G.722 – MPEG audio – progressive encoding – Silence compression, Speech compression – Formant and CELP vocoders.

Unit V	VIDEO COMPRESSION	9

Video compression techniques and Standards – MPEG video coding: MPEG-1 and MPEG -2 video coding: MPEG-3 and MPEG-4 – Motion estimation and compensation techniques – H.261 Standard – DVI technology – DVI real time compression – Current Trends in Compression standards.

REFERENCE(S):

1. David Solomon, "Data Compression – The Complete Reference", Fourth Edition, Springer Verlog, New York, 2006.
2. Darrel Hankerson, Greg A Harris, Peter D Johnson, 'Introduction to Information Theory and Data Compression' Second Edition, Chapman and Hall ,CRC press, 2003
3. Khalid Sayood: Introduction to Data Compression", Morgan Kauffman Harcourt India, Third Edition, 2010.
4. Mark S. Drew, Ze-Nian Li, "Fundamentals of Multimedia", PHI, 2009.
5. Peter Symes : Digital Video Compression, McGraw Hill Pub., 2004.
6. Yun Q.Shi, Huifang Sun, "Image and Video Compression for Multimedia Engineering, Algorithms and Fundamentals", CRC Press, 2003

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Programme	ME-APPLIED ELECTRONICS					R 2019	Semester	III
Course Code	Course Name	Hours / Week			Credit	Total Hours	Maximum Marks	
		L	T	P	C			
19AEX20	WAVELET TRANSFORMS AND ITS APPLICATIONS	3	0	0	3	45	100	

Course Objective (s): The purpose of learning this course is to

- Study the basics of signal representation and Fourier theory
- Understand Multi Resolution Analysis and Wavelet concepts
- Study the wavelet transform in both continuous and discrete domain
- Understand the applications of Wavelet transform

Course Outcomes: At the end of this course, learners will be able to:

- Identify the limitations of Fourier transforms and its applications
- Develop wavelet transform based coding
- Analyze signals and images using wavelet transforms

Unit I	Introduction	9

Vector spaces - properties - dot product - basis-dimension, orthogonality and orthonormality-relationship between vectors and signals-signal spaces-concept of convergence-Hilbert spaces for energy signals

Unit II	Fourier Analysis and STFT	9

Fourier Transform-drawbacks of Fourier analysis- window function - Short-time Fourier Transform (STFT) analysis-spectrogram plot-phase-space plot in time-frequency plane. Heisenberg's uncertainty principle-Tilling of the time-frequency plane for STFT.

Unit III	Continuous Wavelet Transform	9

Wavelet transform properties-concept of scale and its relation with frequency-continuous Wavelet Transform (CWT)-scaling function and wavelet functions: Daubechies, Haar, Coiflet, Mexican hat, Sine, Gaussian, Bi-orthogonal wavelets - Tilling of time scale plane for CWT.

Unit IV	Discrete Wavelet Transform and Multi-Resolution Analysis	9

Discrete Wavelet Transform (DWT)-Filter bank and sub-band coding principles. Multi-resolution analysis-Time scale difference equations for wavelets and scaling functions-Wavelet filters-scale variation in discrete domain-Mallet's algorithm for DWT-Inverse DWT computation by filter banks. Introduction to multiwavelet transforms.

Unit V	Wavelet Packet Analysis and Applications	9

Haar wavelet packets – application –best basis selection and cost functions. Sub-band coding of images-Image compression-Image de-noising – image coding using wavelet tree coder – EZW code and SPIHT code. Introduction to second generation wavelets.

REFERENCE(S):

1. Mallat, S. A Tour on Wavelet Signal Processing, Elsevier, New Delhi, December 2005
2. Rao .R. M and Bopardikar. A.S, Wavelet Transforms, Addison Wesley, 2002
3. Soman K.P. and Ramachandran K.I. Insight into Wavelets-From Theory to Practice, Prentice Hall of India, New Delhi, 2010.
4. Strang G and Nguyen T., Wavelets and Filter Banks, Wellesley Cambridge Press, 2006
5. Vetterli M, and Kovacevic J.,Wavelets and Sub- band Coding, Prentice Hall, 2015

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