

ERODE SENGUNTHAR ENGINEERING COLLEGE



(An Autonomous Institution, Affiliated to Anna University) PERUNDURAI, ERODE - 638 057

PG Curriculum and Syllabus

(1 to 4 Semesters)

M.E. APPLIED ELECTRONICS

Choice Based Credit System (CBCS)

REGULATION 2019

			M.E. APPLIED Minimum credi								
FIRST SE	MESTER							2			
		Objective & Outcomes			-		6	M	C .		
Code No	Course	PEOs	POs	L	T	Р	C	CA	ES	Total	Categor
19AE101	Mathematics for Electronic Systems	I,II	1,2,3,4,12	3	1	0	4	40	60	100	BS
19AE102	Advanced Digital System Design	I,II,III	1,2,3,4,5,12	3	1	0	4	40	60	100	PC
19AE103	CMOS VLSI Design	I,II,III	1,3,4,5,12	3	0	0	3	40	60	100	PC
19AE104	Embedded System Design	I,II,III	1,2,4,5,12	3	0	0	3	40	60	100	PC
19AE105	Computational Intelligence Techniques	I,II,III	1,2,12	3	0	0	3	40	60	100	PC
19AE106	System Theory	I,II,III	1,2,3,4,12	3	1	0	4	40	60	100	PC
			PRACTICA	LS							
19AE107	Real Time Embedded System Laboratory	1,11,111	1,2,3,4,5,12	0	0	4	2	60	40	100	PC
19AE108	Technical Seminar	I,IV	1,2,3,4,9,10	0	0	2	0	60	40	100	EEC
			TOTAL	18	3	6	23	360	440	800	-

	SEMESTER	Objective	& Outcomes					М	Marks		
Code No	Course	PEOs	POs	L	T	P	C	CA	ES	Total	- Category
19AE201	Advanced Digital Signal Processing	I,II,III	1,2,3,4,5,12	3	1	0	4	40	60	100	PC
19AE202	VLSI Signal Processing	I,II,III	1,2,3,4,5,12	3	1	0	4	40	60	100	PC
19AE203	Low Power VLSI Design	1,11,111	1,2,3,4,12	3	0	0	3	40	60	100	PC
	Professional Elective-I	-	-	3	0	0	3	40	60	100	PE
	Professional Elective-II	7	-	3	0	0	3	40	60	100	PE
	Professional Elective-III	-		3	0	0	3	40	60	100	PE

Chairman - Bos Dept.of ECE

PRACTICALS											
19AE204	VLSI laboratory	I,II,III	1,2,3,4,5,12	0	0	4	2	60	40	100	PC
			Total	18	2	4	22	300	400	700	-

C. L. NE	C	Objectiv	e & Outcomes		m	D		Maximum Marks		Category	
Code No	Course	PEOs	POs	L	T	Р	C	CA	ES	Total	
	Professional Elective-IV	-	-	3	0	0	3	40	60	100	PE
	Professional Elective-V	-	·	3	0	0	3	40	60	100	PE
		1	PRACTICAL	S					2.11		
19AE301	Project Work Phase-I	I,II,III,IV	1,2,3,4,5,6,7,8, 9,10,11,12	0	0	12	6	60	40	100	EEC
			Total	6	0	12	12	140	160	300	-

Code No	Courses	Objective & Outcomes	e & Outcomes		T	n	С	M	Catagory		
	Course	PEOs	POs		1	P		CA	ES	Total	Category
19AE401	Project Work Phase-II	I,II,III,IV	1,2,3,4,5,6,7,8, 9,10,11,12	0	0	24	12	60	40	100	EEC
			Total	0	0	24	12	60	40	100	-

ELECTIVES

	PROFESS	SIONAL ELE	CTIVES				
Cole No.	0	Objective	& Outcomes		т	D	
Code No	Course	PEOs	POs	L	1	Р	C
	E	LECTIVES-I					
19AEX01	Sensors, Actuators and Interface Electronics	I,II,III	1,2,3,4,12	3	0	0	3
19AEX02	Computer Architecture and Parallel Processing	I,II,III 1,2,3,4,12		3	0	0	3
19AEX03	Hardware – Software Co-design	I,II,III	1,2,3,4,12	3	0	0	3
19AEX04	Programmable Logic Controllers	I,II,III	1,2,3,4,12	3	0	0	3
	El	LECTIVES-II					
19AEX05	CAD for VLSI	I,II,III	1,2,3,4,12	3	0	0	3
19AEX06	AEX06 ASIC and FPGA Design		1,2,3,4,12	3	0	0	3
19AEX07	System on Chip Design	I,II,III	1,2,3,4,12	3	0	0	3

Chairman - BoS Dept.of ECE - ESEC

19AEX08	Genetic Algorithms	I,II,III	1,2,3,4,12	3	0	0	3
	ELI	ECTIVES-II	I				
19AEX09	Pattern Recognition	I,II,III	1,2,3,4,12	3	0	0	3
19AEX10	Advanced Digital Image Processing	I,II,III	1,2,3,4,5, 12	3	0	0	3
19AEX11	Soft Computing and Optimization Techniques	I,II,III	1,2,3,4,12	3	0	0	3
19AEX12	Synthesis and Optimization of Digital Circuits	I,II,III	1,2,3,4,5, 12	3	0	0	3
	ELI	ECTIVES-IV	7				
19AEX13	Electromagnetic Interference and Compatibility	I,II,III	1,2,3,4,12	3	0	0	3
19AEX14	Nano Electronics	I,II,III	1,2,3,4,12	3	0	0	3
19AEX15	MEMS and NEMS	I,II,III	1,2,3,4,12	3	0	0	3
19AEX16	System Identification and Adaptive Control	I,II,III	1,2,3,4,12	3	0	0	3
	EL	ECTIVES-V					
19AEX17	DSP Architectures and Programming	I,II,III	1,2,3,4,5, 12	3	0	0	3
19AEX18	Speech and Audio Signal Processing	I,II,III	1,2,3,4,5, 12	3	0	0	3
19AEX19	Multimedia Compression Techniques	I,II,III	1,2,3,4,5, 12	3	0	0	3
19AEX20	Wavelet Transforms and its Application	I,II,III	1,2,3,4,12	3	0	0	3

S.No.	Category	I	П	ш	IV	Total	Credits in	Range of Total Credits		
5.110.	Category	1	п	m	IV	Credit	%	Min	Max	
1	BS	4	-	-	-	4	5.79	5%	10%	
2	ES	-	-	-	-	-	-	-	1	
3	HS	-	-,	-	-	-	-	-		
4	PC	19	13	_		32	46.37	40%	50%	
5	PE		9	6	-	15	21.73	20%	25%	
6	EEC	-		6	12	18	26.08	25%	30%	
	Total	23	22	12	12	69	100	1.1	19	

BS- Basic Science

PE- Professional Elective

MC - Mandatory course

ES-Engineering Science **EEC**-Employability Enhancement Course

CA – Continuous Assessment

HSS-Humanities and Social Science

PC- Professional Core

ES- End semester Examination

Chairman - BoS Dept.of ECE - ESEC

Programme	ME-APPLIED I	ELECT	RONIC	CS		R 2019	Semester	I
		Ho	urs / W	Veek	Credit	Total	Maximur	n
Course Code	Course Name	L T P C		Hours	Marks			
19AE101	MATHEMATICS FOR ELECTRONIC SYSTEMS	3	1	0	4	60	100	
Course Object	ve (s): The purpose of learning thi	s course	is to					
• Use com	putational techniques and algebra	aic skill	s essen	tial for	r the study	of matrix	theory, Chol	esky
decompo	sition							
 Algebrai 	c skills essential for the study of To	oeplitz n	natrices	s and C	irculant ma	atrices.	a - hult si	
Construct	t mathematical arguments that rela	te to the	study	of Calc	culus of var	iations		
• Construc	t mathematical arguments that rela	te to the	study	of Stoc	hastic proc	ess		
 Compute 	queuing models and graph theory.							
Course Outcon	nes: At the end of this course, lear	ners wil	l be ab	le to:				
 Apply th 	e matrix theory, and calculus of va	riations						
Critically	analyze Calculus of variations							
Critically	analyze Stochastic process							
 Apply th 	e queuing models in Engineering A	pplicati	ions.					
 Apply th 	e graph theory in Engineering App	lications	5.					
Unit I MA	TRIX THEORY							12
Matrix factoriza	ations - LU decomposition - The	Cholesk	y deco	mposit	tion - QR f	factorization	ı – Least squa	ares
method - Gener	ralized inverses - Singular value de	ecompos	sition –	Toepli	itz matrices	and Circula	ant matrices.	
	APH THEORY							1
	graphs – Isomorphism – Subgraph							
Graphs - Hami	Itonian Paths and circuits – Digra							
	there we the formation of the	test nat	h algo	rithms	– Dijkstra	a's algorith	m – Warsha	
matrix and inc	idence matrix of graphs - Shor	-						
matrix and inc algorithm – Tr	ees - Properties of trees - Spann	-			spanning			
matrix and inc algorithm – Tr Kruskal's algor	ees – Properties of trees – Spann thm.	-			spanning			1 –
matrix and inc algorithm – Tr Kruskal's algor Unit III CA	ees – Properties of trees – Spann ithm. LCULUS OF VARIATIONS	ning tree	es – M	inimal		trees – Prin	n's Algorithn	1 -
matrix and inc algorithm – Tr Kruskal's algor Unit III CA Concept of var	ees – Properties of trees – Spann thm. LCULUS OF VARIATIONS ation – Euler equation – Variation	ning tree	es – M blems	inimal with fi	xed bound	trees – Prin aries – Var	n's Algorithm iational probl	n – 1 ems
matrix and inc algorithm – Tr Kruskal's algor Unit III CA Concept of var involving sever	ees – Properties of trees – Spann ithm. LCULUS OF VARIATIONS iation – Euler equation – Variation al unknown functions – Function	onal pro al invol	blems blems	inimal with fi rst and	xed bound second or	trees – Prin aries – Var der derivati	n's Algorithm iational probl ives – Functi	n – 1 ems onal
matrix and inc algorithm – Tr Kruskal's algor Unit III CA Concept of var involving sever involving sever	ees – Properties of trees – Spann thm. LCULUS OF VARIATIONS ation – Euler equation – Variation al unknown functions – Function ral independent variables – Isop	onal pro al invol	blems blems	inimal with fi rst and	xed bound second or	trees – Prin aries – Var der derivati	n's Algorithm iational probl ives – Functi	n – 1 ems onal
matrix and inc algorithm – Tr Kruskal's algor Unit III CA Concept of var involving sever involving sever Kantorowich m	ees – Properties of trees – Spann ithm. LCULUS OF VARIATIONS iation – Euler equation – Variatic al unknown functions – Function ral independent variables – Isoj ethod.	onal pro al invol	blems blems	inimal with fi rst and	xed bound second or	trees – Prin aries – Var der derivati	n's Algorithm iational probl ives – Functi	n – ems ona d –
matrix and inc algorithm – Tr Kruskal's algor Unit III CA Concept of var involving sever involving sever Kantorowich m Unit IV STO	ees – Properties of trees – Spann ithm. LCULUS OF VARIATIONS ation – Euler equation – Variation al unknown functions – Function ral independent variables – Isop ethod. DCHASTIC PROCESS	onal pro al invol	blems ving fi	inimal with fi rst and blems	xed bound second or – Direct	trees – Prin aries – Var der derivati methods –	n's Algorithm iational probl ives – Functi Ritz metho	1 - 1 ems onal d - 1
matrix and inc algorithm – Tr Kruskal's algor Unit III CA Concept of var involving sever involving sever Kantorowich m Unit IV STC Definition – C	ees – Properties of trees – Spann thm. LCULUS OF VARIATIONS fation – Euler equation – Variation al unknown functions – Function ral independent variables – Isop ethod. DCHASTIC PROCESS lassification of Stochastic Proce	onal pro al invol perimetr sses –	blems ving fi ic pro Marko	inimal with fi rst and blems v Chai	xed bound l second or – Direct in -Transit	trees – Prin aries – Var der derivati methods – ion Probab	n's Algorithm iational probl ves – Functi Ritz metho ility Matrice	1 - 1 emsonal d - 1 1 s - 1
matrix and inc algorithm – Tr Kruskal's algor Unit III CA Concept of var involving sever involving sever Kantorowich m Unit IV STO Definition – C Chapman Koln	ees – Properties of trees – Spann thm. LCULUS OF VARIATIONS ation – Euler equation – Variation al unknown functions – Function ral independent variables – Isop ethod. DCHASTIC PROCESS lassification of Stochastic Proce mogorov Equations - Classification	onal pro al invol perimetr sses –	blems ving fi ic pro Marko	inimal with fi rst and blems v Chai	xed bound l second or – Direct in -Transit	trees – Prin aries – Var der derivati methods – ion Probab	n's Algorithm iational probl ves – Functi Ritz metho ility Matrice	n - 1 emsona d - 1 s - 1
matrix and inc algorithm – Tr Kruskal's algor Unit III CA Concept of var involving sever involving sever Kantorowich m Unit IV STC Definition – C Chapman Koln Process - Birth	ees – Properties of trees – Spann thm. LCULUS OF VARIATIONS iation – Euler equation – Variation al unknown functions – Function ral independent variables – Isop ethod. DCHASTIC PROCESS lassification of Stochastic Proce togorov Equations - Classification and Death Processes.	onal pro al invol perimetr sses –	blems ving fi ic pro Marko	inimal with fi rst and blems v Chai	xed bound l second or – Direct in -Transit	trees – Prin aries – Var der derivati methods – ion Probab	n's Algorithm iational probl ves – Functi Ritz metho ility Matrice	1 - 1 emsona d - 1 s - son
matrix and inc algorithm – Tr Kruskal's algor Unit III CA Concept of var involving sever involving sever Kantorowich m Unit IV STO Definition – C Chapman Kolm Process - Birth a Unit V QU	ees – Properties of trees – Spann ithm. LCULUS OF VARIATIONS iation – Euler equation – Variation al unknown functions – Function ral independent variables – Isopethod. DCHASTIC PROCESS lassification of Stochastic Proce nogorov Equations - Classification and Death Processes. EUING MODELS	onal pro al invol perimetr sses – n of Sta	es – M blems ving fi ic pro Marko ates –	inimal with fi rst and blems v Chai Contin	xed bound l second or – Direct in -Transit uous Time	trees – Prin aries – Var der derivati methods – ion Probab Markov C	n's Algorithn iational probl ives – Functi Ritz metho ility Matrice hains – Pois	$1 - \frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$
matrix and inc algorithm – Tr Kruskal's algor Unit III CA Concept of var involving sever involving sever kantorowich m Unit IV STC Definition – C Chapman Koln Process - Birth Unit V QU Markovian que	ees – Properties of trees – Spann thm. LCULUS OF VARIATIONS iation – Euler equation – Variation al unknown functions – Function ral independent variables – Isop ethod. DCHASTIC PROCESS lassification of Stochastic Proce togorov Equations - Classification and Death Processes.	onal pro al invol perimetr sses – n of Sta dels – Li	es – M blems ving fi ic pro Marko ates –	inimal with fi rst and blems v Chai Contin	xed bound l second or – Direct in -Transit uous Time	trees – Prin aries – Var der derivati methods – ion Probab Markov C	n's Algorithn iational probl ives – Functi Ritz metho ility Matrice hains – Pois	$1 - \frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$ $\frac{1}{2}$

Chairman - BoS Dept.of ECE - ESEC

RE	FERENCE(S):
1.	Richard Bronson Matrix Operation, Schaum's outline series, 2nd Edition, McGraw Hill, 2011.
2.	Sheldon M. Ross Introduction To Probability And Statistics For Engineers And Scientists-Elsevier
3.	Roy D.Yates and David J Goodman, Probability and Stochastic Processes – A friendly Introduction for Electrical and Computer Engineers", John Wiley & Sons, 2005.
4.	Lev Elsgot- Differential Equations and the Calculus of Variations

Uboon

Chairman - BoS Dept. of Maths - ESEC

R.l. Chairman - BoS Dept.of ECE - ESEC

Programm	ne ME-APPLIED I	ELECTRO	ONIC	S		R 2019	Semester	I
Course Co	de Course Name		urs / /eek		Credit	Total Hours	Maximun Marks	n
		L	T	Р	С	Hours	WIAT KS	
19AE102	ADVANCED DIGITAL SYSTEM DESIGN	3	1	0	4	60	100	
 Unders Unders Unders Unders Unders Unders Ourse Ou Apply Descrite Discuss Descrite Apply Unit I ASM Char (ASC) - F Design of A Unit II VHDL Des VHDL Co Combination 	jective (s): The purpose of learning this tand the design procedures of sequenti tand the design procedures using VHD tand the various types of Field Program tand the methods of fault modeling and tand the fault diagnosis and testability tcomes: At the end of this course, lear the design procedures of sequential log be the design procedures using VHDL is the various types of Field Programma be the various types of Field Programma the methods of the fault diagnosis and the ADVANCED TOPIC IN SEQUENT t – ASM Realization for Synchronous low Table Reduction – Races in ASC ASC – Static and Dynamic Hazards – E SYSTEM DESIGN USING VHDL cription of Combinational Circuits – de – Modeling using VHDL – Fli mal Logic Circuits – VHDL Code for Systems – Design of a Simple Micropr	al logic de DL nmable Ga d simulatic algorithms rners will b ic design able Gate A ng and sim testability IAL LOG Logic cir C – State Essential H Arrays – 7 p Flops – Serial Ado	sign ate Ar on be able Array ulatio algori IC D cuit – Assig azard VHDI – Reg	e to: thms ESIC Anal nmen s.	SN ysis of Asy t – Proble erators – C s - Count	m and the T Compilation a ers – Seque	ransition Tab	le – 12 n of e –
	FIELD PROGRAMMABLE GATE	1	5			1		12
Input/ Outp Introduction Unit IV Introduction – Fault loc	PGA – XILINX XC3000 series – Log out Blocks (IOB) – Programmable I in to Xilinx SPARTAN, VIRTEX FPGA FAULT MODELING AND SIMULA in to Testing – Faults in digital circuits ation – Fault dominance – Logic Sim- en simulation.	nterconne A – Desigr ATION – Modelin	ction n exan	Poin nples faults	ts (PIP) – - Logical I	XILINX X	C4000 Series	12 tion
Unit V	FAULT DIAGNOSIS AND TESTAI	BILITY A	LGO	RIT	HMS			12
Fault Table Techniques	Method – Path Sensitization Method – The Compact Algorithm – Practical es – Built-in Self Test.	– Boolea	n Dif	feren	ce Method			
REFEREN	CE(S):	Z						
publica	r. Charles H. Lizy Kurian John, "Diation, 2012.							
mixed	el L Bushnell, Vishwani D Agrawal, signal VLSI circuit, Kluwer academic	Publicatio	ns, U	SA, 2	.014.	ing For digi	tal memory a	nd
3. Nripen	dra N Biswas ogic Design Theory Prei	ntice Hall	of Ind	ia, 20)15.			

P.10-

Chairman - BoS Dept.of ECE - ESEC

4.	Parag K.Lala, An Introduction to Logic Circuit Testing Morgan and Claypool publishers, 2011.	
5.	Balabanian, Digital Logic Design Principles, Wiley publication, 2007.	
6.	Stephen D Brown, Fundamentals of Digital Logic, TMH publication, 2007.	

Chairman - BoS Dept.of ECE - ESEC

Juez : Run Inito Juez : Jos iunte d

	ME-APPLIED	ELECTR	ONIC	S		R 2019	Semester	1
Course Code	Course Name		Hours / Week		Credit	Total	Maximum	
4		L	Т	P	С	Hours	Marks	
19AE103	CMOS VLSI DESIGN	3	0	0	3	45	100	
Course Objective	(s): The purpose of learning this	course is					· · · · · · · · · · · · · · · · · · ·	
 Understand t Understand t Understand t Understand t Understand t Understand t Describe the Describe the p Describe the 	he process of VLSI and Basic CM he design procedures of CMOS a he performance estimation of CM he methods of logic synthesis and he methods of system partitioning at the end of this course, learn process of VLSI and Basic CMO MOS circuits performance estimation of CMOS methods of logic synthesis and si methods of system partitioning an DESIGN PROCESS AND BAS - Design flow -VLSI Design P	Ind its cha IOS chara I simulation g and rout ers will be S character mulation nd routing SIC CMO	cteristion ing e able t istics	o:		- Logical F	Design - Phys	ica
Design – Layou	t Styles –Full custom, Semicus fect- Design equations- Second on	tom appr	oaches	. NM	IOS and I	PMOS trans	istors, Thresh	nolo
Unit II INVE	RTERS, CMOS LOGIC AND	CIRCUI	Г СНА	RAC	TERIZA	TION		9
Basic CMOS te	chnology NMOS and CMOS Ir	verters -	Stick	diag	ram, Inver	ter ratio, D	C and transi	ent
characteristics , s Transmission gat estimation.	switching times, Super buffers, tes - Static CMOS design - dyn	Driving la	arge ca	pacita	ance loads	- CMOS I	ogic structure	s -
characteristics , s Transmission gat estimation. Unit III PERI	switching times, Super buffers, tes - Static CMOS design - dyn FORMANCE ESTIMATION	Driving la amic CM	arge ca OS de	pacita sign	ance loads - Résistan	- CMOS lo ce estimatio	ogic structure n - Capacitar	s - nce
characteristics , s Transmission gat estimation. Unit III PERI MOS capacitor of capacitance - Rou Fall time - Dela	switching times, Super buffers, tes - Static CMOS design - dyn	Driving la amic CM ances - D C effects - els - Gate	orge ca OS de Diffusio Induct	pacita sign on caj	ance loads - Résistanc pacitance - Switchin	- CMOS le ce estimatio	ogic structure n - Capacitar odeling of M stics - Rise tir	s - nce 9 1OS ne wei
characteristics , s Transmission gat estimation. Unit III PERI MOS capacitor of capacitance - Rou Fall time - Dela dissipation- Scali	switching times, Super buffers, 1 tes - Static CMOS design - dyn FORMANCE ESTIMATION characteristics - Device capacita ting capacitance - Distributed RC ty time - Empirical delay mode	Driving la amic CM ances - D C effects - els - Gate	orge ca OS de Diffusio Induct	pacita sign on caj	ance loads - Résistanc pacitance - Switchin	- CMOS le ce estimatio	ogic structure n - Capacitar odeling of M stics - Rise tir	s - nce 9 105 ne -
characteristics , s Transmission gat estimation. Unit III PERI MOS capacitor of capacitance - Rou Fall time - Dela dissipation- Scali Unit IV LOG Simulation - Gat	switching times, Super buffers, 1 tes - Static CMOS design - dyn FORMANCE ESTIMATION characteristics - Device capacita iting capacitance - Distributed RC by time - Empirical delay mode ing of MOS transistor dimensions	Driving la amic CM ances - D C effects - els - Gate ATION n - Switc	orge ca OS de Diffusic Induct e delay	pacita sign on caj tance ys - 0	ance loads - Résistance pacitance - Switchin CMOS ga leling and	- CMOS le ce estimatio	ogic structure n - Capacitar odeling of M stics - Rise tin sizing - Po	s - nce (OS ne wei
characteristics , s Transmission gat estimation. Unit III PERI MOS capacitor of capacitance - Rou Fall time - Dela dissipation- Scali Unit IV LOG Simulation - Gat Logic Synthesis -	switching times, Super buffers, 1 tes - Static CMOS design - dyn FORMANCE ESTIMATION characteristics - Device capacita tting capacitance - Distributed RC by time - Empirical delay mode ng of MOS transistor dimensions IC SYNTHESIS AND SIMULA e-level modeling and simulation	Driving la amic CM ances - D C effects - els - Gata	orge ca OS de Diffusic Induct e delay	pacita sign on caj tance ys - 0	ance loads - Résistance pacitance - Switchin CMOS ga leling and	- CMOS le ce estimatio	ogic structure n - Capacitar odeling of M stics - Rise tin sizing - Po	s - nce (OS ne wei
characteristics , s Transmission gat estimation. Unit III PERI MOS capacitor of capacitance - Rou Fall time - Dela dissipation - Scali Unit IV LOG Simulation - Gat Logic Synthesis - Unit V SYST System partition - -global routing -	witching times, Super buffers, 1 tes - Static CMOS design - dyn CORMANCE ESTIMATION characteristics - Device capacita ating capacitance - Distributed RC by time - Empirical delay mode ing of MOS transistor dimensions IC SYNTHESIS AND SIMULA e-level modeling and simulation Binary Decision Diagrams - Two EM PARTITIONING AND RC FPGA partitioning - partitioning detailed routing - special routing	Driving la amic CM ances - D C effects - els - Gata	orge ca OS de Diffusic Induct e delay h-level ogic Sy - floor	on cap tance ys - 0 mod mthes	ance loads - Résistance - Switchin CMOS ga leling and is.	- CMOS le ce estimatio	ogic structure n - Capacitar odeling of M stics - Rise tin sizing - Po - Combinatic	s - nce IOS ne we
characteristics , s Transmission gat estimation. Unit III PERI MOS capacitor of capacitance - Rou Fall time - Dela dissipation - Scali Unit IV LOG Simulation - Gat Logic Synthesis - Unit V SYST System partition - -global routing - REFERENCE(S)	witching times, Super buffers, I tes - Static CMOS design - dyn FORMANCE ESTIMATION characteristics - Device capacita iting capacitance - Distributed RC by time - Empirical delay mode ing of MOS transistor dimensions IC SYNTHESIS AND SIMULA e-level modeling and simulation Binary Decision Diagrams - Two EM PARTITIONING AND RC FPGA partitioning - partitioning detailed routing - special routing	Driving la amic CM ances - D C effects - els - Gate MTION n - Switc D Level Lo DUTING g methods - circuit ex	orge ca OS de Diffusic Induct e delay h-level ogic Sy - floor xtractic	mod mon cap tance ys - f mod mthes plan on - D	ance loads - Résistance - Switchin CMOS ga deling and is. ning - plac PRC.	- CMOS le ce estimatio - SPICE m g characteri te transistor simulation ement - phy	ogic structure n - Capacitar odeling of M stics - Rise tin r sizing - Po - Combination r sical design f	s - nce IOS ne we Dna
characteristics , s Transmission gat estimation. Unit III PERI MOS capacitor of capacitance - Rou Fall time - Dela dissipation- Scali Unit IV LOG Simulation - Gat Logic Synthesis - Unit V SYST System partition - global routing - of REFERENCE(S) 1. Neil H.E. W Education, 2	switching times, Super buffers, 1 tes - Static CMOS design - dyn FORMANCE ESTIMATION characteristics - Device capacita ating capacitance - Distributed RC by time - Empirical delay mode ing of MOS transistor dimensions IC SYNTHESIS AND SIMULA e-level modeling and simulation Binary Decision Diagrams - Two EM PARTITIONING AND RC FPGA partitioning - partitioning detailed routing - special routing E Veste CMOS VLSI Design: A 0 012.	Driving la amic CM ances - D C effects - els - Gate ATION n - Switc b Level Lo DUTING g methods - circuit ex Circuits a	orge ca OS de Diffusio Induct e delay h-level ogic Sy - floor xtractio	mod mod mod mod mod mod mod mod mod mod	ance loads - Résistance - Switchin CMOS ga leling and is. ning - plac DRC. Perspectiv	- CMOS le ce estimatio - SPICE m g characteri te transistor simulation ement - phy ve (For VT	ogic structure n - Capacitar odeling of M stics - Rise tin r sizing - Po - Combination r sical design f	s - nce IO: ne we Dna
characteristics , s Transmission gat estimation. Unit III PERI MOS capacitor of capacitance - Rou Fall time - Dela dissipation - Scali Unit IV LOG Simulation - Gat Logic Synthesis - Unit V SYST System partition - -global routing - O REFERENCE(S) 1. Neil H.E. W Education, 2 2. Gerez S.H., A	witching times, Super buffers, 1 tes - Static CMOS design - dyn CORMANCE ESTIMATION characteristics - Device capacita ating capacitance - Distributed RC by time - Empirical delay mode ing of MOS transistor dimensions IC SYNTHESIS AND SIMULA e-level modeling and simulation Binary Decision Diagrams - Two EM PARTITIONING AND RC FPGA partitioning - partitioning detailed routing - special routing E Veste CMOS VLSI Design: A 0 012.	Driving la amic CM ances - D C effects - els - Gate ATION n - Switc o Level Lo DUTING g methods - circuit ex Circuits a omation, J	orge ca OS de Diffusic Induct e delay h-level ogic Sy - floor xtractic nd Sys	mod mod mod mod mod mod mod mod mod mod	ance loads - Résistance - Switchin CMOS ga leling and is. ning - plac DRC. Perspectiv & Sons, rep	- CMOS le ce estimatio - SPICE m g characteri te transistor simulation ement - phy ve (For VT print 2018.	ogic structure n - Capacitar odeling of M stics - Rise tin r sizing - Po - Combination r sical design f	s - nce IO: ne we Dna
characteristics , a Transmission gat estimation. Unit III PERI MOS capacitor of capacitance - Rou Fall time - Dela dissipation - Scali Unit IV LOG Simulation - Gat Logic Synthesis - Unit V SYST System partition - -global routing - REFERENCE(S) 1. Neil H.E. W Education, 2 2. Gerez S.H., A 3. M.J.S. Smith	switching times, Super buffers, 1 tes - Static CMOS design - dyn FORMANCE ESTIMATION characteristics - Device capacita ating capacitance - Distributed RC by time - Empirical delay mode ing of MOS transistor dimensions IC SYNTHESIS AND SIMULA e-level modeling and simulation Binary Decision Diagrams - Two EM PARTITIONING AND RC FPGA partitioning - partitioning detailed routing - special routing E Veste CMOS VLSI Design: A 0 012.	Driving la amic CM ances - D C effects - els - Gate ATION n - Switc o Level Lo DUTING g methods - circuit ex Circuits a omation, J Circuits,	orge ca OS de Diffusic Induct e dela h-level ogic Sy - floor xtractic nd Sys ohn W Pearso	mod mod mod mod mod mod mod mod mod mod	ance loads - Résistance - Switchin CMOS ga leling and is. ning - plac DRC. Perspectiv & Sons, representation, 20	- CMOS le ce estimatio - SPICE m g characteri te transistor simulation ement - phy ve (For VT print 2018. 16.	ogic structure n - Capacitar odeling of M stics - Rise tin r sizing - Po - Combinatio sical design f	s - nce IOS ne we ona

Chairman - BoS Dept.of ECE - ESEC

Programme	ME-APPLIED EL	ME-APPLIED ELECTRONICS						
			lours /		Credit	Total	Maximum	
Course Code	Course Name	Week Hours M		Marks				
		L	T	P	C		100	_
19AE104	EMBEDDED SYSTEM DESIGN	3	0	0	3	45	100	
Understan Understan Understan Understan Understan Understan Understan Ourse Outcor Describe t Descri	ive (s): The purpose of learning this could the design methodology of embedded d the characteristics of general and sing d the types of Bus structures d the state machine and concurrent product the embedded software development thes: At the end of this course, learners he design methodology of embedded synthe characteristics of general and single e types of Bus structures he methods of state machine and concur debug using embedded software development MBEDDED SYSTEM OVERVIEW stem Overview, Design Challenges – ational and Sequential Components, Open ENERAL AND SINGLE PURPOSE cture, Pipelining, Superscalar and V Application-Specific Instruction-Set Product of the state of the structure of the structure of the structure of the state machine and very the structure of the structur	l syster gle purp cess mo tools a will be ystem purpos rrent p opmen Optim otimizin PROC	odels nd RTC able to able to e process rocess to t tools a izing I ng Cust CESSO architeo	DS b: essor mode and R Design tom S R ctures	ls CTOS. n Metrics, Single-Purp	nmer's view	sors. v, Developm	9 ent
Unit III B Basic Protocol Serial Protoco Bluetooth, IEE	er, UART, LCD Controllers and Analo US STRUCTURES Concepts, Microprocessor Interfacing Is, I2C, CAN and USB, Parallel Proto E 802.11.	g-to-D – I/O pcols –	Addres PCI a	ssing, nd A	rters, Mem Port and RM Bus,	ory Concep Bus-Based	ots. I/O, Arbitrati	9 0n,
Unit IIIBBasic ProtocolSerial ProtocoBluetooth, IEEUnit IVS'	er, UART, LCD Controllers and Analog US STRUCTURES Concepts, Microprocessor Interfacing Is, I2C, CAN and USB, Parallel Proto E 802.11. FATE MACHINE AND CONCURRI	g-to-D – I/O pcols – ENT P	Addres PCI a	ssing, nd A	Port and RM Bus, TODELS	Bus-Based Wireless Pi	ots. I/O, Arbitratio rotocols – IrD	9 on, 0A,
Unit IIIBBasic ProtocolSerial ProtocoBluetooth, IEEUnit IVS'Basic StateMSequentialPCommunicatioAutomation:SDesign Process	er, UART, LCD Controllers and Analog US STRUCTURES Concepts, Microprocessor Interfacing Is, I2C, CAN and USB, Parallel Proto E 802.11. TATE MACHINE AND CONCURRI Machine Model, Finite-State Machine rogramming Language, Program-St n among Processes, Synchronization ynthesis, Verification : Hardware/Soft is Models.	g-to-D – I/O pools – ENT P e with ate M among ware C	Addres PCI a PCI a ROCE Datap Iachine proces	ssing, nd A SSS M bath 1 e M sses, ulatio	rters, Mem Port and RM Bus, 10DELS Model, Ca odel, Co Dataflow n, Reuse:	Bus-Based Wireless Pr apturing St ncurrent F Model, Rea Intellectual	ots. I/O, Arbitration rotocols – IrD ate Machine Process Mod al-time Syster	9 on,)A, in lel, ns, res,
Unit IIIBBasic ProtocolSerial ProtocolBluetooth, IEEUnit IVS'Basic StateMSequentialPrCommunicationAutomation:SDesign ProcessUnit VE	er, UART, LCD Controllers and Analog US STRUCTURES Concepts, Microprocessor Interfacing Is, I2C, CAN and USB, Parallel Proto E 802.11. TATE MACHINE AND CONCURR Machine Model, Finite-State Machine rogramming Language, Program-St n among Processes, Synchronization ynthesis, Verification : Hardware/Soft Models. MBEDDED SOFTWARE DEVELOI	g-to-D - I/O cools – ENT P e with ate M among ware C PMEN	Addres PCI a PCI a PCI a PCI a Datap fachine proces Co-Simu T TOC	ssing, nd A SSS M bath 1 e M sses, ulatio	rters, Mem Port and RM Bus, 10DELS Model, Ca odel, Co Dataflow n, Reuse: AND RTO	Bus-Based Wireless Pr apturing St ncurrent I Model, Rea Intellectual	ots. I/O, Arbitration rotocols – IrD ate Machine Process Moc al-time Syster Property Cor	9 on, 0A, 9 in lel, ns, res, 9
Unit IIIBBasic ProtocolSerial ProtocolBluetooth, IEEUnit IVS'Basic State NSequential ProtocolCommunicationAutomation: SDesign ProcessUnit VECompilation Protocol	er, UART, LCD Controllers and Analog US STRUCTURES Concepts, Microprocessor Interfacing Is, I2C, CAN and USB, Parallel Proto E 802.11. TATE MACHINE AND CONCURRI Machine Model, Finite-State Machine rogramming Language, Program-St n among Processes, Synchronization ynthesis, Verification : Hardware/Soft is Models.	g-to-D – I/O pools – ENT P e with ate M among ware C PMEN – C ex	Addres PCI a PCI a ROCE Datap Iachine proces Co-Simu T TOC	ssing, nd A SSS M bath 1 e M sses, ulatio	rters, Mem Port and RM Bus, 10DELS Model, Ca odel, Co Dataflow n, Reuse: AND RTO	Bus-Based Wireless Pr apturing St ncurrent I Model, Rea Intellectual	ots. I/O, Arbitration rotocols – IrD ate Machine Process Moc al-time Syster Property Cor	9 on, 0A, 9 in lel, ns, res, 9
Unit IIIBBasic ProtocolSerial ProtocolBluetooth, IEEUnit IVS'Basic StateSequentialPhiCommunicationAutomation:SDesign ProcessUnit VECompilationPBebugging tech	er, UART, LCD Controllers and Analog US STRUCTURES Concepts, Microprocessor Interfacing Is, I2C, CAN and USB, Parallel Proto E 802.11. TATE MACHINE AND CONCURR Machine Model, Finite-State Machine rogramming Language, Program-St n among Processes, Synchronization ynthesis, Verification : Hardware/Soft & Models. MBEDDED SOFTWARE DEVELOD rocess – Libraries – Porting kernels – miques – RTOS – System design using	g-to-D – I/O pools – ENT P e with ate M among ware C PMEN – C ex	Addres PCI a PCI a ROCE Datap Iachine proces Co-Simu T TOC	ssing, nd A SSS M bath 1 e M sses, ulatio	rters, Mem Port and RM Bus, 10DELS Model, Ca odel, Co Dataflow n, Reuse: AND RTO	Bus-Based Wireless Pr apturing St ncurrent I Model, Rea Intellectual	ots. I/O, Arbitration rotocols – IrD ate Machine Process Moc al-time Syster Property Cor	on, oA, in lel, ns, res,
Unit IIIBBasic ProtocolSerial ProtocolBluetooth, IEEUnit IVS'Basic State NSequential ProtocolCommunicationAutomation: SDesign ProcessUnit VECompilation Pdebugging techREFERENCE1Bruce Pov	er, UART, LCD Controllers and Analog US STRUCTURES Concepts, Microprocessor Interfacing Is, I2C, CAN and USB, Parallel Proto E 802.11. TATE MACHINE AND CONCURR Machine Model, Finite-State Machine rogramming Language, Program-St n among Processes, Synchronization ynthesis, Verification : Hardware/Soft & Models. MBEDDED SOFTWARE DEVELOD rocess – Libraries – Porting kernels – miques – RTOS – System design using	g-to-Di - I/O pcols - ENT P e with ate M among ware C PMEN - C ex RTOS	Addres PCI a PCI a PCI a PCI a Datap fachine proces Co-Simu T TOC tensior	ssing, nd A SSS N bath 1 e M sses, ulatio DLS A ns for	rters, Mem Port and RM Bus, 10DELS Model, Ca odel, Co Dataflow n, Reuse: AND RTO embedde	Bus-Based Wireless Pr apturing St ncurrent I Model, Rea Intellectual OS d systems -	ots. I/O, Arbitratio rotocols – IrD ate Machine Process Moc al-time Syster Property Cor – emulation a	9 0n, 0A, 10 10 10 10 10 10 10 10 10 10 10 10 10
Unit IIIBBasic ProtocolSerial ProtocolSerial ProtocolBluetooth, IEEUnit IVS'Basic StateSequentialProtommunicationAutomation:SDesign ProcessUnit VECompilationBebugging techREFERENCE1.Bruce Pov 3rd Editio	er, UART, LCD Controllers and Analog US STRUCTURES Concepts, Microprocessor Interfacing Is, I2C, CAN and USB, Parallel Proto E 802.11. TATE MACHINE AND CONCURRI Machine Model, Finite-State Machine rogramming Language, Program-St n among Processes, Synchronization ynthesis, Verification : Hardware/Soft & Models. MBEDDED SOFTWARE DEVELOI rocess – Libraries – Porting kernels – miques – RTOS – System design using (S): wel Douglas,Real time UML, second ed	g-to-D - I/O cols - ENT P e with ate M among ware C PMEN - C ex RTOS lition:	Addres PCI a PCI a PCI a PCI a PCI a Datap fachine proces Co-Simu T TOC tensior	ssing, nd A SSS N bath 1 e M sses, ulatio DLS A ns for ping o	rters, Mem Port and RM Bus, 10DELS Model, Ca odel, Co Dataflow n, Reuse: AND RTO embedde	Bus-Based Wireless Pr apturing St ncurrent H Model, Rea Intellectual OS d systems -	ots. I/O, Arbitration otocols – IrD ate Machine Process Moo al-time Syster Property Cor - emulation a nbedded syste	9 on, OA, 9 in lel, ns, res, 9 and ems
Unit IIIBBasic ProtocolSerial ProtocolSerial ProtocolBluetooth, IEEUnit IVS'Basic State NSequential ProtocolCommunicationAutomation: SDesign ProcessUnit VECompilation PBebugging techREFERENCE1.Bruce Pov3rd Edition2.Daniel W2002.3.Frank Val	er, UART, LCD Controllers and Analog US STRUCTURES Concepts, Microprocessor Interfacing Is, I2C, CAN and USB, Parallel Proto E 802.11. TATE MACHINE AND CONCURR Machine Model, Finite-State Machine rogramming Language, Program-St n among Processes, Synchronization ynthesis, Verification : Hardware/Soft Models. MBEDDED SOFTWARE DEVELOP rocess – Libraries – Porting kernels – miques – RTOS – System design using (S): wel Douglas,Real time UML, second econ n 2009, Pearson Education.	g-to-Di - I/O cols - ENT P e with ate M among ware C PMEN - C ex RTOS lition: I oftware em Des	Addres PCI a PCI a PCI a PCI a PCI a PCI a Datap fachine proces Co-Simu T TOC tensior Develo e where sign, Jc	ssing, nd A SSS N bath 1 SSES, ulatio DLS 2 ns for ping o e C a	rters, Mem Port and RM Bus, 1ODELS Model, Ca odel, Co Dataflow n, Reuse: AND RTO embedde efficient ol nd assemb	Bus-Based Wireless Pr apturing St ncurrent I Model, Rea Intellectual OS d systems -	ots. I/O, Arbitration otocols – IrD ate Machine Process Moo al-time Syster Property Cor - emulation a nbedded syste	on, oA, in lel, ns, res, gund

Chairman - BoS Dept.of ECE - ESEC

	TY I I I I I I I I I I I I I I I I I I I					R 2019	Semester	r
Course Code	Course Name		rs / We	eek	Credit	Total	Maximu	
	COMPUTATION	L	Т	Р	С	Hours	Marks	
19AE105	COMPUTATIONAL INTELLICENCE TECHNIQUES	3	0	0	3			
Course Object	INTELLIGENCE TECHNIQUES tive (s): The purpose of learning this co			U	3	45	100	
Understa	and the various loss of learning this co	ourse is						-
• Underste	and the various learning techniques of a	rtificial	neural	netwo	orks			
- Understa	nd the basic concepts of fuzzy logic							
• Understa	nd the optimization techniques,							
• Classify	the types of neuro fuzzy modeling							
Knowled	ge about Applications of neural network	k.						
Course Outcon	nes: At the end of this course, learners	will be	able to):				_
Describe	the various learning techniques of artif	icial ne	ural ne	twork	6			
Discuss L	ne basic concepts of fuzzy logic		and ne	WUIK	5			
 Describe 	the methods of optimization techniques							
 Describe 	the types of neuro fuzzy modeling	,						
 Gain Kno 	wledge about applications of neural net	u cali						
Unit I ART	TIFICIAL NEURAL NETWORKS	WOFK.						
ntroduction to S	oft computing – Neural Networks – M eptrons – Adaline and Madaline – P	la da t						9
earning - Perce	eptrons - Adaline and Madali	odel –	activat	ion fu	nctions – a	rchitecture	- Supervis	e
Networks - Unsu	eptrons – Adaline and Madaline – B pervised Learning and Other Neural N	Back pr	opagat	ion al	gorithm -	Radial Ba	sis Functi	-
onse	ipervised Learning and Other Neural N	aturial	- 0					or
elf Organizing N	Jetworks Lease: W	etwork	s - Cor	mpetit	ive Learni	ng Network	s – Kohon	0I er
	pervised Learning and Other Neural N Vetworks – Learning Vector Quantization	on – He	s – Coi ebbian I	mpetit Learni	ive Learni ng.	ng Network	s – Kohon	or er
Jnit II FUZ	ZY LOGIC	on – He	bolan	Learn	ive Learni ng.	ng Network	s – Kohon	en
Jnit II FUZ uzzy Sets - Basi	ZY LOGIC	on – He	oblan i	Learn	ng.	ng Network	s – Kohon	en 9
Jnit II FUZ uzzy Sets – Basing Basing nd parameterization Basing	ZY LOGIC ic Definition and Terminology – Set th tion - Extension principle and Eugen	eoretic	operati	ions –	ng. Membersl	ng Network	s – Kohon formulatic	9 01
Jnit II FUZ uzzy Sets – Basind Fuzzy Sets – Basind uzzy Inference State	ZY LOGIC ic Definition and Terminology – Set th tion - Extension principle and Fuzzy 1 Systems – Mamdani Fuzzy Models	eoretic	operati	ions –	ng. Membersl	ng Network	s – Kohon formulatic	9 00
Jnit II FUZ uzzy Sets – Basing Basing and parameterization Basing uzzy Inference Basing uput Space Partition Basing	ZY LOGIC ic Definition and Terminology – Set th tion - Extension principle and Fuzzy 1 Systems – Mamdani Fuzzy Models – ioning - Fuzzy Modeling.	eoretic	operati	ions –	ng. Membersl	ng Network	s – Kohon formulatic	9 0
Jnit II FUZ uzzy Sets – Basing Basing uzzy Inference Basing uzzy Inference Basing uput Space Partition nit III OPT	ZY LOGIC ic Definition and Terminology – Set th tion - Extension principle and Fuzzy 1 Systems – Mamdani Fuzzy Models – ioning - Fuzzy Modeling.	eoretic Relatio Sugeno	operati ns- Fuz Fuzzy	ions – zzy if ⁄ Mod	Membersh then Rule els –Tsuka	ng Network nip function s – Fuzzy amoto Fuzz	formulatic Reasoning cy Models	9 0n
Jnit IIFUZuzzy Sets – Basiud parameterizatiuzzy Inferenceuput Space Partitinit IIIOPTerivativebased	ZY LOGIC ic Definition and Terminology – Set th tion - Extension principle and Fuzzy 1 Systems – Mamdani Fuzzy Models – ioning - Fuzzy Modeling. IMIZATION TECHNIQUES Optimization: Descent Methods The	eoretic Relatio Sugeno	operati ns- Fuz Fuzzy	ions – zzy if ⁄ Mod	Membersh then Rule els –Tsuka	ng Network nip function s – Fuzzy amoto Fuzz	s – Kohon formulatic Reasoning ty Models	9 0n -
Jnit II FUZ uzzy Sets – Basing Basing uzzy Inference Basing uzzy Inference Basing uput Space Partition nit III OPT erivative based ethod – Step Siz	ZY LOGIC ic Definition and Terminology – Set th tion - Extension principle and Fuzzy 1 Systems – Mamdani Fuzzy Models – ioning - Fuzzy Modeling. IMIZATION TECHNIQUES Optimization: Descent Methods –The e Determination – Derivative free Opti	on – He eoretic Relatio Sugeno	operati ns- Fuz Fuzzy	ions – zzy if ⁄ Mod	Membersh then Rule els –Tsuka	ng Network nip function s – Fuzzy amoto Fuzz	s – Kohon formulatic Reasoning ty Models	9 0n
Jnit II FUZ uzzy Sets – Basing Basing ud parameterization Basing uzzy Inference State uput Space Partition nit III OPT erivative based ethod Step Siz Particle swarm Comparison Step Siz	ZY LOGIC ic Definition and Terminology – Set th tion - Extension principle and Fuzzy 1 Systems – Mamdani Fuzzy Models – ioning - Fuzzy Modeling. IMIZATION TECHNIQUES Optimization: Descent Methods –The e Determination – Derivative free Opti	on – He eoretic Relatio Sugeno	operati ns- Fuz Fuzzy	ions – zzy if ⁄ Mod	Membersh then Rule els –Tsuka	ng Network nip function s – Fuzzy amoto Fuzz	s – Kohon formulatic Reasoning ty Models	9 0n
Jnit II FUZ Suzzy Sets – Basing Basing Suzzy Inference Suzzy Inference Suzzy Inference Suzzy Inference Suput Space Partitit Suzzy Inference Suzzy Suzzy Suzy </td <td>ZY LOGIC ic Definition and Terminology – Set th tion - Extension principle and Fuzzy 1 Systems – Mamdani Fuzzy Models – ioning - Fuzzy Modeling. IMIZATION TECHNIQUES Optimization: Descent Methods –The the Determination – Derivative free Opti Optimization - Ant colony optimization.</td> <td>on – He eoretic Relatio Sugeno</td> <td>operati ns- Fuz Fuzzy</td> <td>ions – zzy if ⁄ Mod</td> <td>Membersh then Rule els –Tsuka</td> <td>ng Network nip function s – Fuzzy amoto Fuzz</td> <td>s – Kohon formulatic Reasoning ty Models</td> <td>9 0n -</td>	ZY LOGIC ic Definition and Terminology – Set th tion - Extension principle and Fuzzy 1 Systems – Mamdani Fuzzy Models – ioning - Fuzzy Modeling. IMIZATION TECHNIQUES Optimization: Descent Methods –The the Determination – Derivative free Opti Optimization - Ant colony optimization.	on – He eoretic Relatio Sugeno	operati ns- Fuz Fuzzy	ions – zzy if ⁄ Mod	Membersh then Rule els –Tsuka	ng Network nip function s – Fuzzy amoto Fuzz	s – Kohon formulatic Reasoning ty Models	9 0n -
Jnit IIFUZJuzzy Sets – BasindFuzzy Sets – BasindJuzzy InferenceStateJuzzy InferenceStateJuzzy InferenceStateJuzzy InferenceStateJuzzy InferenceState <td>ZY LOGIC ic Definition and Terminology – Set th tion - Extension principle and Fuzzy 1 Systems – Mamdani Fuzzy Models – ioning - Fuzzy Modeling. IMIZATION TECHNIQUES Optimization: Descent Methods –The the Determination – Derivative free Opti Optimization - Ant colony optimization. RO FUZZY MODELING</td> <td>eoretic Relatio Sugeno</td> <td>operati ns- Fuz Fuzzy od of s on: Gen</td> <td>ions – zzy if v Mod</td> <td>Membersh then Rule els –Tsuka st Descent lgorithms</td> <td>ng Network nip function s – Fuzzy amoto Fuzz – Classica – Simulated</td> <td>s – Kohon formulatic Reasoning y Models y Models</td> <td>9 9 9 5 9</td>	ZY LOGIC ic Definition and Terminology – Set th tion - Extension principle and Fuzzy 1 Systems – Mamdani Fuzzy Models – ioning - Fuzzy Modeling. IMIZATION TECHNIQUES Optimization: Descent Methods –The the Determination – Derivative free Opti Optimization - Ant colony optimization. RO FUZZY MODELING	eoretic Relatio Sugeno	operati ns- Fuz Fuzzy od of s on: Gen	ions – zzy if v Mod	Membersh then Rule els –Tsuka st Descent lgorithms	ng Network nip function s – Fuzzy amoto Fuzz – Classica – Simulated	s – Kohon formulatic Reasoning y Models y Models	9 9 9 5 9
Jnit IIFUZJuzzy Sets – BasindFuzzy Sets – BasindJuzzy InferenceStateJuzzy InferenceStateJuzzy InferenceStateStatePartitionInit IIIOPTParticle swarm ControlStep SizeParticle swarm ContNEUIIdaptive Neuro Fu	ZY LOGIC ic Definition and Terminology – Set th tion - Extension principle and Fuzzy 1 Systems – Mamdani Fuzzy Models – ioning - Fuzzy Modeling. IMIZATION TECHNIQUES Optimization: Descent Methods –The e Determination – Derivative free Opti Optimization - Ant colony optimization. RO FUZZY MODELING	eoretic Relatio Sugeno	operati ns- Fuz Fuzzy od of s on: Gen	ions – zzy if Mod steepe	Membersh Membersh then Rule lels –Tsuka st Descent lgorithms	ng Network nip function s – Fuzzy amoto Fuzz – Classica – Simulated	s – Kohon formulatic Reasoning ty Models I Newton' d Annealing	9 9 9 5 9
Jnit II FUZ uzzy Sets – Basing Fuzzy Sets – Basing uzzy Inference Fuzzy Inference uzzy Inference Fuzzy Inference uput Space Partition uput Space Partition uput Space Partition erivative based ethod – Step Siz Particle swarm Control Particle swarm Control NEUI laptive Neuro Fuzzy	ZY LOGIC ic Definition and Terminology – Set th tion - Extension principle and Fuzzy 1 Systems – Mamdani Fuzzy Models – ioning - Fuzzy Modeling. IMIZATION TECHNIQUES Optimization: Descent Methods –The e Determination – Derivative free Opti Optimization - Ant colony optimization. RO FUZZY MODELING Izzy Inference Systems – Architecture FIS and RBFN – Coactive Neuro fiz	eoretic Relatio Sugeno	operati ns- Fuz Fuzzy od of s on: Gen	ions – zzy if Mod steepe	Membersh Membersh then Rule lels –Tsuka st Descent lgorithms	ng Network nip function s – Fuzzy amoto Fuzz – Classica – Simulated	s – Kohon formulatic Reasoning ty Models I Newton' d Annealing	9 9 9 9
Jnit II FUZ uzzy Sets – Basind parameterization Fuzzy Sets – Basind parameterization uzzy Inference State uzzy Inference State uput Space Partition nit III OPT erivative based ethod – Step Siz Particle swarm Control nit IV NEUI laptive Neuro Fu oss-fertilize aptive Networks	ZY LOGIC ic Definition and Terminology – Set th tion - Extension principle and Fuzzy I Systems – Mamdani Fuzzy Models – ioning - Fuzzy Modeling. IMIZATION TECHNIQUES Optimization: Descent Methods –The e Determination – Derivative free Opti optimization - Ant colony optimization. RO FUZZY MODELING Izzy Inference Systems – Architecture FIS and RBFN – Coactive Neuro fuz – Neuro Fuzzy spectrum.	eoretic Relatio Sugeno	operati ns- Fuz Fuzzy od of s	ions – zzy if Mod steepe	Membersh Membersh then Rule lels –Tsuka st Descent lgorithms	ng Network nip function s – Fuzzy amoto Fuzz – Classica – Simulated	s – Kohon formulatic Reasoning ty Models I Newton' d Annealing	er 9 n - 9 s g
Jnit II FUZ Juzzy Sets – Basind Fuzzy Sets – Basind Juzzy Inference State State State Particle swarm State Justice Neuro Justice Networks Justice APPL	ZY LOGIC ic Definition and Terminology – Set th tion - Extension principle and Fuzzy 1 Systems – Mamdani Fuzzy Models – ioning - Fuzzy Modeling. IMIZATION TECHNIQUES Optimization: Descent Methods –The e Determination – Derivative free Opti Optimization - Ant colony optimization. RO FUZZY MODELING Izzy Inference Systems – Architecture FIS and RBFN – Coactive Neuro fuz – Neuro Fuzzy spectrum. ICATIONS	on – He eoretic Relatio Sugeno Metho mizatic – Hybr zy Mod	operati ns- Fuz Fuzzy od of s on: Gen id lean deling	ions – zzy if / Mod steepe netic A ning / – Fra	Membersh Membersh then Rule lels –Tsuka st Descent lgorithms Algorithm – mework –	ng Network nip function s – Fuzzy amoto Fuzz – Classica – Simulated –learning m Neuron Fu	s – Kohon formulatic Reasoning cy Models l Newton' d Annealing d Annealing gethods that nctions for	9 9 9 s g t
Jnit II FUZ Juzzy Sets – Basind Fuzzy Sets – Basind Juzzy Inference State Particle State Particle Swarm Or Juzzy NEUI Juzzy NEUI Juzzy Neuro Juzy Neuro Juzy Neuro <	ZY LOGIC ic Definition and Terminology – Set th tion - Extension principle and Fuzzy 1 Systems – Mamdani Fuzzy Models – ioning - Fuzzy Modeling. IMIZATION TECHNIQUES Optimization: Descent Methods –The te Determination – Derivative free Opti Optimization - Ant colony optimization. RO FUZZY MODELING UZZY Inference Systems – Architecture FIS and RBFN – Coactive Neuro fuz – Neuro Fuzzy spectrum. ICATIONS	on – He eoretic Relatio Sugeno Metho mizatic – Hybr zy Mod	operati ns- Fuz Fuzzy od of s on: Gen rid lear deling	ions – zzy if / Mod steepe netic A ning A – Fra	Membersh Membersh then Rule lels –Tsuka st Descent lgorithms Algorithm – mework –	ng Network nip function s – Fuzzy f amoto Fuzz – Classica – Simulated –learning m Neuron Fu	s – Kohon formulatic Reasoning y Models y Models l Newton' d Annealing d Annealing gethods that inctions for 9	9 9 s g t
Jnit II FUZ Juzzy Sets – Basind Fuzzy Sets – Basind Juzzy Inference State Particle State Particle Swarm Or Juzzy NEUI Juzzy NEUI Juzzy Neuro Juzy Neuro Juzy Neuro <	ZY LOGIC ic Definition and Terminology – Set th tion - Extension principle and Fuzzy 1 Systems – Mamdani Fuzzy Models – ioning - Fuzzy Modeling. IMIZATION TECHNIQUES Optimization: Descent Methods –The te Determination – Derivative free Opti Optimization - Ant colony optimization. RO FUZZY MODELING UZZY Inference Systems – Architecture FIS and RBFN – Coactive Neuro fuz – Neuro Fuzzy spectrum. ICATIONS	on – He eoretic Relatio Sugeno Metho mizatic – Hybr zy Mod	operati ns- Fuz Fuzzy od of s on: Gen rid lear deling	ions – zzy if / Mod steepe netic A ning A – Fra	Membersh Membersh then Rule lels –Tsuka st Descent lgorithms Algorithm – mework –	ng Network nip function s – Fuzzy f amoto Fuzz – Classica – Simulated –learning m Neuron Fu	s – Kohon formulatic Reasoning y Models y Models l Newton' d Annealing d Annealing gethods that inctions for 9	9 9 s g t
Jnit II FUZ Juzzy Sets – Basind parameterization Fuzzy Sets – Basind Juzzy Inference Standard Set	ZY LOGIC ic Definition and Terminology – Set th tion - Extension principle and Fuzzy 1 Systems – Mamdani Fuzzy Models – ioning - Fuzzy Modeling. IMIZATION TECHNIQUES Optimization: Descent Methods –The e Determination – Derivative free Opti Optimization - Ant colony optimization. RO FUZZY MODELING Izzy Inference Systems – Architecture FIS and RBFN – Coactive Neuro fuz – Neuro Fuzzy spectrum. ICATIONS	on – He eoretic Relatio Sugeno Metho mizatic – Hybr zy Mod	operati ns- Fuz Fuzzy od of s on: Gen rid lear deling	ions – zzy if / Mod steepe netic A ning A – Fra	Membersh Membersh then Rule lels –Tsuka st Descent lgorithms Algorithm – mework –	ng Network nip function s – Fuzzy f amoto Fuzz – Classica – Simulated –learning m Neuron Fu	s – Kohon formulatic Reasoning y Models y Models l Newton' d Annealing d Annealing gethods that inctions for 9	9 9 s g t
Jnit II FUZ Juzzy Sets – Basind parameterization Fuzzy Sets – Basind parameterization Juzzy Inference Standard Set (Set (Set (Set (Set (Set (Set (Set	ZY LOGIC ic Definition and Terminology – Set th tion - Extension principle and Fuzzy I Systems – Mamdani Fuzzy Models – ioning - Fuzzy Modeling. IMIZATION TECHNIQUES Optimization: Descent Methods –The e Determination – Derivative free Opti Optimization - Ant colony optimization. RO FUZZY MODELING Izzy Inference Systems – Architecture FIS and RBFN – Coactive Neuro fuz – Neuro Fuzzy spectrum. ICATIONS Recognition – Inverse kinematics Probl MPPT, speed control for electrical m	eoretic Relatio Sugeno Metho mizatic – Hybr zy Mod lem – A achines	operati ns- Fuz Fuzzy od of s on: Gen id lean deling	ions – zzy if / Mod steepe netic A – Fran tions of	Membersh then Rule els –Tsuka st Descent lgorithms Algorithm- mework – of soft con	ng Network	s – Kohon formulatic Reasoning y Models y Models y Models g al Newton' d Annealing g hethods that inctions for g nniques for s in power	9 9 s g t
Jnit II FUZ Juzzy Sets – Basind parameterization Fuzzy Sets – Basind parameterization Juzzy Inference State Ind parameterization Fuzzy Inference Input Space Partition Init III OPT erivative based ethod – Step Siz Particle swarm Conti IV NEUI laptive Neuro Fu oss-fertilize ANI aptive Networks it V APPL nted Character R ver electronics: verters. ERENCE(S): J.S.R Jang, C.	ZY LOGIC ic Definition and Terminology – Set th tion - Extension principle and Fuzzy I Systems – Mamdani Fuzzy Models – ioning - Fuzzy Modeling. IMIZATION TECHNIQUES Optimization: Descent Methods –The e Determination – Derivative free Opti optimization - Ant colony optimization. RO FUZZY MODELING Izzy Inference Systems – Architecture FIS and RBFN – Coactive Neuro fuz – Neuro Fuzzy spectrum. ICATIONS Recognition – Inverse kinematics Probl MPPT, speed control for electrical m	e Metho mizatio - Hybr zy Mod em – A achines	operati ns- Fuzzy od of s on: Gen rid lear deling Applica s, harm	ions – zzy if Mod steepe netic A – Fran tions o	Membersh Membersh then Rule lels –Tsuka st Descent lgorithms Algorithm- mework – of soft con elimination	ng Network	s – Kohon formulation Reasoning cy Models y Models y Models g al Newton' d Annealing g nethods that inctions for g nniques for s in power	9 9 5 9 1 5 9
Jnit II FUZ Juzzy Sets – Basind parameterization Juzzy Inference State State State Particle State Particle Swarm Or Juzzy NEUI Japtive Neuro Fu Juzzy Networks It V APPL Inted Character R Ner electronics: Ver electronics: Verters. ERENCE(S): J.S.R Jang, C. Jaurene V. F	ZY LOGIC ic Definition and Terminology – Set th tion - Extension principle and Fuzzy 1 Systems – Mamdani Fuzzy Models – ioning - Fuzzy Modeling. IMIZATION TECHNIQUES Optimization: Descent Methods –The te Determination – Derivative free Opti Optimization - Ant colony optimization. RO FUZZY MODELING UZZY Inference Systems – Architecture FIS and RBFN – Coactive Neuro fuz – Neuro Fuzzy spectrum. ICATIONS	e Metho mizatio - Hybr zy Mod em – A achines	operati ns- Fuzzy od of s on: Gen rid lear deling Applica s, harm	ions – zzy if Mod steepe netic A – Fran tions o	Membersh Membersh then Rule lels –Tsuka st Descent lgorithms Algorithm- mework – of soft con elimination	ng Network	s – Kohon formulation Reasoning cy Models y Models y Models g al Newton' d Annealing g nethods that inctions for g nniques for s in power	9 9 5 9 1 5 9

Chairman - BoS Dept.of ECE - ESEC

3.	Timothy J. Ross, Fuzzy Logic with Engineering Applications Wiley India.
1	David E.Goldberg, Genetic Algorithms: Search, Optimization and Machine Learning, Addison Wesley, New York, 2008.

Chairman - BoS Dept.of ECE - ESEC

Program	me	ME-APPLIE	D ELECT	RONI	ICS		R 2019	Semester	I
		6 N	Hours	s / We	ek	Credit	Total	Maximum	1
Course C	ode	Course Name	L	Т	Р	С	Hours	Marks	
19AE1	06	SYSTEM THEORY	3	1	0	4	60	100	
Course O	bjective	(s): The purpose of learning	this course	e is					
 Unde Unde Unde Unde Ourse O Descr Discu Analy Defin Unit I Elements 	rstand th rstand th rstand th rstand th outcomes ribe the b rss the va vze state vze state e the effe of Digit	feedback control ect of stability DUCTION TO DIGITAL al control system- Classificat	of Discret eedback co earners wil n CONTRO	Il be al DL SY screte	ble to: STEM	bility analy	me domain 1		
		pling and reconstruction of							
rate. Unit II	Z-PLA	NE ANALYSIS OF DISCH	RETE-TIN	ME CO	ONTR	OL SYST	EMS		12
rate. Unit II Review o	Z-PL A of Z tran me syste		RETE-TIN	ME CO and z	ONTR plane	OL SYST	EMS nce equatior	n representatio	12 on of
rate. Unit II Review o discrete ti	Z-PL A of Z tran me syste	NE ANALYSIS OF DISCH sform- Relationship betwee	RETE-TIN n s plane 10dified Z	ME CO and z transf	ONTR plane form- I	OL SYST	EMS nce equatior	n representatio	12 on of chols
rate. Unit II Review o discrete ti tuning me Unit III Review o diagram-S	Z-PLA of Z tran me syste thod STAT f state s Solution	NE ANALYSIS OF DISCH sform- Relationship between m-Pulse transfer function -M	RETE-TIN n s plane fodified Z D ITS SOL sion of cor autonomou	ME CO and z transf UTIO ntinuou us, nor	DNTR plane form- I DN us state n-autor	OL SYST - Differen Digital PID e model to	EMS nce equation controllers-	n representatio - Zeigler – Ni nte model – S	12 on of chols 12 tate
rate. Unit II Review o discrete ti tuning me Unit III Review o diagram-S –Controlla	Z-PLA of Z tran me syste thod STAT f state sp Solution ability ar	NE ANALYSIS OF DISCH sform- Relationship between em-Pulse transfer function -M E SPACE ANALYSIS AND pace representation- Converse of discrete time state model:	RETE-TIM n s plane Aodified Z D ITS SOL sion of con autonomou ble discret	ME CO and z transf UTIO ntinuou us, nor	DNTR plane form- I DN us state n-autor	OL SYST - Differen Digital PID e model to	EMS nce equation controllers-	n representatio - Zeigler – Ni nte model – S	12 on of chols 12 tate
rate. Unit II Review o discrete ti tuning me Unit III Review o diagram-S –Controlla Unit IV Design of	Z-PLA of Z tran me syste thod STAT f state s Solution ability ar STAT	ANE ANALYSIS OF DISCH sform- Relationship between em-Pulse transfer function -M E SPACE ANALYSIS AND pace representation- Converse of discrete time state model: ad observability – Multi varia	RETE-TIM n s plane Aodified Z D ITS SOL sion of con autonomou ble discrete L	ME CO and z transf UTIO ntinuou as, nor e syste and fi	ONTR plane form- I ON us statu n-autor ems.	OL SYST - Differen Digital PID e model to nomous sys er observe	EMS nce equation controllers- o discrete sta tems – State	a representatio - Zeigler – Ni ate model – S e transition ma	12 on of chols tate trix
rate. Unit II Review o discrete ti tuning me Unit III Review o diagram-S –Controlla Unit IV Design of	Z-PLA of Z tran me syste thod STAT f state s Solution ability ar STAT state fee eedback	ANE ANALYSIS OF DISCH sform- Relationship between em-Pulse transfer function -M E SPACE ANALYSIS AND pace representation- Converse of discrete time state model: ad observability – Multi varia E FEEDBACK CONTROL edback controller – Design of	RETE-TIM n s plane Aodified Z D ITS SOL sion of con autonomou ble discrete L	ME CO and z transf UTIO ntinuou as, nor e syste and fi	ONTR plane form- I ON us statu n-autor ems.	OL SYST - Differen Digital PID e model to nomous sys er observe	EMS nce equation controllers- o discrete sta tems – State	a representatio - Zeigler – Ni ate model – S e transition ma	12 on of chols 12 tate ttrix 12
rate. Unit II Review o discrete ti tuning me Unit III Review o diagram-S –Controlla Unit IV Design of space-PI fi Unit V BIBO sta stability-L	Z-PLA of Z tran me syste thod STAT f state s Solution ability ar State fee beedback STAB bility-Ef	ANE ANALYSIS OF DISCH sform- Relationship between em-Pulse transfer function -M E SPACE ANALYSIS AND bace representation- Converse of discrete time state model: ad observability – Multi varia E FEEDBACK CONTROL edback controller – Design of Digital compensator design-	RETE-TIN n s plane Aodified Z D ITS SOL sion of cor autonomou ble discret L Dof reduced – Digital fi tability-Jun e time syst	ATE CO and z transf UTIO ntinuou is, nor e syste and fi lter pr	ONTR plane form- I ON us statu n-autor ems. ull ord opertie ability	OL SYST - Differen Digital PID e model to nomous sys er observe es– Kalmar test-Root	EMS nce equation controllers- o discrete sta tems – State rs – Steady i's filter.	n representatio - Zeigler – Ni ate model – S e transition ma state error in	12on ofchols12tatettrix12state12totic
rate. Unit II Review o discrete ti tuning me Unit III Review o diagram-S –Controlla Unit IV Design of space-PI fi Unit V BIBO sta stability-L	Z-PLA of Z tran me syste thod STAT f state sp Solution of ability ar STAT state fee bedback STAB bility-Ef iapunov onstructi	ANE ANALYSIS OF DISCH sform- Relationship between m-Pulse transfer function -M E SPACE ANALYSIS AND pace representation- Converse of discrete time state model: ad observability – Multi varia E FEEDBACK CONTRO edback controller – Design of Digital compensator design- ILITY ANALYSIS fect of sampling rate on s Stability Analysis of discret	RETE-TIN n s plane Aodified Z D ITS SOL sion of cor autonomou ble discret L Dof reduced – Digital fi tability-Jun e time syst	ATE CO and z transf UTIO ntinuou is, nor e syste and fi lter pr	ONTR plane form- I ON us statu n-autor ems. ull ord opertie ability	OL SYST - Differen Digital PID e model to nomous sys er observe es– Kalmar test-Root	EMS nce equation controllers- o discrete sta tems – State rs – Steady i's filter.	n representatio - Zeigler – Ni ate model – S e transition ma state error in	12on ofchols12tatettrix12state12totic
rate. Unit II Review o discrete ti tuning me Unit III Review o diagram-S -Controlla Unit IV Design of space-PI f Unit V BIBO sta stability-L method-Co EFEREN	Z-PLA of Z tran me syste thod STAT f state sp Solution ability ar State fee bedback STAB bility-Ef iapunov onstructi CE(S):	ANE ANALYSIS OF DISCH sform- Relationship between m-Pulse transfer function -M E SPACE ANALYSIS AND pace representation- Converse of discrete time state model: ad observability – Multi varia E FEEDBACK CONTRO edback controller – Design of Digital compensator design- ILITY ANALYSIS fect of sampling rate on s Stability Analysis of discret	RETE-TIN n s plane Aodified Z D ITS SOL sion of con autonomou ble discrete L of reduced – Digital fi tability-Jun e time systee ion.	ATE CO and z transf UTIO ntinuou is, nor e syste and fi lter pro- ry's st tems: 1	DNTR plane form- I DN us statu n-autor ems. ull ord opertie ability Linear	OL SYST - Differen Digital PID e model to nomous sys er observe es- Kalmar test-Root and Non-I	EMS nce equation controllers- o discrete sta tems – State rs – Steady d's filter. Locus anal inear system	n representatio - Zeigler – Ni ate model – S e transition ma state error in lysis –Asymp ns- Direct, Ind	12 on of chols tate trix 12 state 12 totic irect
rate. Unit II Review o discrete ti tuning me Unit III Review o diagram-S -Controlla Unit IV Design of space-PI ff Unit V BIBO sta stability-L method-Co EFEREN 1. Gopal, I 2. Kuo, B.	Z-PLA of Z transing thod STAT f state sp Solution of ability ar STAT state feedback STAB bility-Eff iapunov onstruction CE(S): M., Digin C., Digin	ANE ANALYSIS OF DISCH sform- Relationship betweet m-Pulse transfer function -M E SPACE ANALYSIS AND bace representation- Converse of discrete time state model: ad observability – Multi varia E FEEDBACK CONTRO edback controller – Design of Digital compensator design- LITY ANALYSIS fect of sampling rate on s Stability Analysis of discret on of Liapunov energy function tal Control and State Variable and Control Systems, 2nd edit	RETE-TIN n s plane Aodified Z D ITS SOL sion of con autonomou ble discrete L of reduced – Digital fi tability-Jun e time syst ion.	ATE CO and z transf UTIO ntinuou is, nor e syste and fi lter pro- ry's st tems: 1 4th eo Unive	DNTR plane form- I DN us statu n-autor ems. ull ord opertic ability Linear dition, ersity I	OL SYST - Differen Digital PID e model to nomous sys er observe es- Kalmar test-Root and Non-l Tata McGi Press, Oxfo	EMS nce equation controllers- o discrete sta tems – State rs – Steady d's filter. Locus anal inear system raw-Hill, Ne ord, 2007.	n representatio - Zeigler – Ni ate model – S e transition ma state error in lysis –Asymp ns- Direct, Ind w Delhi, 2012	12 on of chols tate trix 12 state 12 totic irect
rate. Unit II Review o discrete ti tuning me Unit III Review o diagram-S -Controlla Unit IV Design of space-Pl f Unit V BIBO sta stability-L method-Co EFEREN . Gopal, I 2. Kuo, B. 3. Ogata, I	Z-PLA of Z tran me syste thod STAT f state sy Solution of ability ar State fee beedback STAB bility-Ef iapunov onstructi CE(S): M., Digit K., Discr	ANE ANALYSIS OF DISCH sform- Relationship between m-Pulse transfer function -M E SPACE ANALYSIS AND bace representation- Converse of discrete time state model: ad observability – Multi varia E FEEDBACK CONTRO edback controller – Design of Digital compensator design- ILITY ANALYSIS fect of sampling rate on s Stability Analysis of discret on of Liapunov energy function tal Control and State Variable	RETE-TIN n s plane Aodified Z D ITS SOL sion of cor autonomou ble discrete L Dof reduced – Digital fi tability-Jun e time syst ion. e Methods, ion Oxford econd editi	AIE CO and z transf UTIO ntinuou is, nor e syste and fu lter pro- ry's st tems: 1 4th eco I Unive on Pre	DNTR plane form- I ON us statu- n-autor ems. ull ord opertie ability Linear dition, ersity I entice I	OL SYST - Differen Digital PID e model to nomous sys er observe es- Kalmar test-Root and Non-l Tata McGu Press, Oxfo Hall, New J	EMS nce equation controllers- o discrete sta tems – State rs – Steady l's filter. Locus anal inear system raw-Hill, Ne ord, 2007. Jersey, 2011.	n representatio - Zeigler – Ni ate model – S e transition ma state error in lysis –Asymp ns- Direct, Ind w Delhi, 2012	12 on of chols tate trix 12 state 12 totic lirect

Rilo Chairman - BoS Dept.of ECE - ESEC

Programme	ME-APPLIED E	LECTH	RONIC	CS		R 2019	Semester	1	
Course Code	Course Name		lours . Week		Credit	Total		Maximum	
104 5107	REAL TIME EMBEDDED	L	T	Р	C	Hours	Marks		
19AE107	SYSTEMS LABORATORY	0	0	4	2	45	100		

Course Objective (s): The purpose of learning this course is

- · Learn to program in PIC Microcontroller
- · Learn to interface with I2C communication
- Study the DSP Processor
- · Learn to Interface with PIC Microcontroller
- Learn Stepper Motor Interfacing

Course Outcomes: At the end of this course, learners will be able to:

- Understand the Program logic in PIC
- Understand the Program Logic in Embedded based Communication
- Gain knowledge about the DSP Processors
- · Programming to Interface with PIC Microcontroller
- Programming to Interface Stepper Motor

Exp No.	Name of Experiments
1	RS232C Bus Interfacing with PIC Microcontroller
2	LED and Switch Interfacing with Embedded PIC Microcontroller
3	LED interfacing with Embedded PIC Microcontroller
4	LED and Key matrix Interfacing with Embedded PIC Microcontroller
5	EEPROM Interfacing with Embedded PIC Microcontroller (I2C-Communication)
6	LCD Interfacing with Embedded PIC Microcontroller
7	Rolling Display in LCD /LED using Embedded PIC Microcontroller
8	Stepper Motor Interfacing with Embedded PIC Microcontroller
9	ADC Interfacing with Embedded PIC Microcontroller(I2C-Communication)
10	RTC interfacing with Embedded PIC Microcontroller(I2C-Communication)
11	Study of Convolution Algorithm Implementation using DSP Processor
12	Study of Matrix Multiplication using DSP Processor

R.L.



Programme	ME-APPLIED	ELECI	RONI	CS		R 2019	Semester	I
Course Code	Course Name	1	Hours . Week		Credit	Total	Maximum	
		L	Т	P	С	Hours	Marks	
19AE108	TECHNICAL SEMINAR	0	0	2	0	30	100	

Course Objective: In this course, students will develop their scientific and technical reading and writing skills that they need to understand and construct research articles. A term paper requires a student to obtain information from a variety of sources (i.e. Journals, dictionaries, reference books) and then place it in logically developed ideas.

TECHNICAL SEMINAR

The work involves the following steps:

- Selecting a subject, narrowing the subject into a topic
- Stating an objective.
- Collecting the relevant bibliography (at least 15 journal papers)
- Preparing a working outline.
- Studying the papers and understanding the authors contributions and critically analyzing each paper.
- Preparing a working outline
- Linking the papers and preparing a draft of the paper.
- Preparing conclusions based on the reading of all the papers.
- Writing the Final Paper and giving final Presentation

Chairman - BoS Dept.of ECE - ESEC

30

Bod - matulid 3, cara - ital et mod

SEMESTER-II

Programme	ME-APPLIED E	LECT	RON	CS		R 2019	Semester	Π
Course Code	Course Name	I	lours Week		Credit	Total	Maxim	
		L	Т	Р	С	Hours	Mark	S
19AE201	ADVANCED DIGITAL SIGNAL PROCESSING	3	1	0	4	60	100	
Course Obje	ctive (s): The purpose of learning this of	course	is to			P. P. P.		
• Unders	stand the discrete random signal proces	sing						
• Update	with important filters and algorithms.							
• Familia	ar with digital filter banks.							
 Analyz 	te the Uniform and two channel filter b	anks						
	stand Sparse Signal Processing							
	omes: At the end of this course, learne	rs will	be ab	le to:				
	ar with the stationary process.							
	the various filters for signal processing							
	be with noise cancellation filtering met							
	Uniform and two Channel filter banks							
	Sparse signal Processing							
	SCRETE RANDOM SIGNAL PRO	CESSI	INC					12
	e random process - Random process: E	Contraction and and and and and and and and and an	and the second s	rages- (Gaussian pr	ocess - Stat	ionary proce	1. <u>1</u>
	variance and autocorrelation matrices							
	tchine relation- Filtering random proce				a series and the series of the	u unit i urbe	i and and one	
	LTERS							12
	ener filter - Filtering - Linear prediction	- IIR	Wiene	r Filter	- Non caus	al IIR Wier	er filter - Ca	
	ilter. Adaptive Filter: Concepts of adaptive							
	ULTIRATE DIGITAL SIGNAL PR				F			12
	description of sampling rate - Interp			2	tion by int	eger factor	- Sampling	1.15372
	rational factor- Filter design for sampl					-		
	ltistage implementation of sampling ra	-						
	NIFORM AND TWO CHANNEL FI	A CONTRACT OF	A CONTRACTOR OF A CONTRACTOR		D APPLIC	CATIONS	OF DSP	12
	Banks – Two -channel Quadrature M			1				
	ation using adaptive filtering technique					al Contra Traine Inc.		
and interpolati				Ũ	- 4-			
	PARSE SIGNAL PROCESSING				1 1 1 1			12
Sparse Signal	Representation- Introduction-Sparse	signal	s-Con	pressil	ole signal-(Over compl	ete dictiona	ries-
	ween the bases-Compressed sensing a				and the second			
	netry property.							
	2/02		-					5
REFERENCE						<i>P</i> 1	1242	_
	Monson H. Statistical Digital Signal pro	ocessii	ng and	Model	ing, John W	mey and Sc	ons,	
Inc., 201		D'	4 1 C'	1.0		n.:	A 1	
2. Proakis,	John G. and Manolakis, Dimitris G	. Digi	ital Si	gnal P	rocessing:	Principles /	Algorithms	and

P.les

Chairman - BoS Dept.of ECE - ESEC

3.	Ifeachor, Emmanuel C. and Jervis, Barrie N. Digital Signal Processing: A Practical Approach, Addison- Wesley Publishing Company, 2012
4.	Dionitris G. Manolakis, Vinay K. Ingle, Stepen M. Kogon, Statistical & Adaptive signal processing, spectral estimation, signal modeling, Adaptive filtering & Array processing, McGraw-Hill International edition 2000.
5	K.P.Soman R.Ramanathan, Digital Signal and Image Processing –The Sparse Way, Elseveir Publisher, 2012.

R.L. Chairman - BoS Dept.of ECE - ESEC

	APPLIED E	LECTRO	ONICS	5		R 2019	Semester	II
C C 1	Come Name	Hours	/ Wee	k	Credit	Total	Maximum	
Course Code	Course Name	L	Т	Р	С	Hours	Marks	
19AE202	VLSI SIGNAL PROCESSING	3	1	0	4	60	100	
Course Object	tive (s): The purpose of learning this	course i	s to					
 Introduction 	e techniques for altering the existing	g DSP str	ucture	s to si	uit VLSI in	nplementati	ions	
 Introduction 	e efficient design of DSP architectu	res suital	ole for	VLSI				
• Underst	and the folding and fast Convolution	n i						
• Underst	and Algorithmic Strength Reduction	(1				
• Understa	and the Pipelined and parallel recurs	ive filter	S					
Course Outcon	mes: At the end of this course, learn	ners will	be able	e to:				
Modify	the existing or new DSP structures s	uitable fo	or VLS	SI.				
	t design of DSP architectures.							
	folding and fast Convolution							
	Algorithmic Strength Reduction							
	Pipelined recursive filters							
	RODUCTION TO DSP SYSTEM	IS						12
Contraction and the second	o DSP Systems -Typical DSP algo		teratio	n Boi	ınd – data	flow graph	h representatio	100
	d iteration bound, Algorithms For	12 million 13 million 14					and the second states of the second	
	phs. Pipelining and parallel process		-					
	parallel processing for low power.							1
Unit II RE	TIMING AND UNFOLDING							12
	TIMING AND UNFOLDING efinitions and properties Retiming	g technic	ques;	Solvi	ng system	ns of inequ	ualities, Retir	
Retiming - de								ning
Retiming - de Techniques. U	efinitions and properties Retiming	ding, pro	opertie	s of	unfolding,	Critical pa	th Unfolding	ning
Retiming - de Techniques. U Retiming applie	efinitions and properties Retiming nfolding – an algorithm for Unfol	ding, pro reductio	opertie	s of	unfolding,	Critical pa	th Unfolding	ning
Retiming - de Techniques. U Retiming applie Unit III FO	efinitions and properties Retiming nfolding – an algorithm for Unfol cations of Unfolding- sample period	ding, pro reductio	opertie n and j	s of a paralle	unfolding, el processi	Critical pa ng applicati	th Unfolding	ning and 12
Retiming - de Techniques. U Retiming applie Unit III FO Folding – Fol	efinitions and properties Retiming nfolding – an algorithm for Unfol cations of Unfolding- sample period LDING AND FAST CONVOLUT	ding, pro reductio ION ninimizir	n and partie	s of paralle	unfolding, el processi es –Regis	Critical pa ng applicati ter minimi	ath Unfolding ion. zation in fol	ming and 12 ded
Retiming - de Techniques. U Retiming applie Unit III FO Folding – Fol architectures-Fe	efinitions and properties Retiming nfolding – an algorithm for Unfol cations of Unfolding- sample period LDING AND FAST CONVOLUT ding transformation – Register n	ding, pro reductio TON ninimizir onvolutio	n and p ng tecl on – C	s of a paralle hnique Cook-7	unfolding, el processi es –Regis Foom algo	Critical pa ng applicati ter minimi prithm, mod	ath Unfolding ion. zation in fol- lified Cook-To	ning and 12 ded ook
Retiming - de Techniques. U Retiming applie Unit III FO Folding – Fol architectures-Fe algorithm – Wi inspection.	efinitions and properties Retiming nfolding – an algorithm for Unfol cations of Unfolding- sample period LDING AND FAST CONVOLUT ding transformation – Register n olding of Multirate systems. Fast c no grad Algorithm, Modified Wino	ding, pro reductio ION ninimizir onvolutio grad Al	n and p ng tecl on – C gorithr	s of a paralle hnique Cook-7	unfolding, el processi es –Regis Foom algo	Critical pa ng applicati ter minimi prithm, mod	ath Unfolding ion. zation in fol- lified Cook-To	ning and 12 ded ook
Retiming-deTechniques.URetiming applieUnit IIIFOFolding-Folding-architectures-Fealgorithm-winspection.Unit IVAL	efinitions and properties Retiming nfolding – an algorithm for Unfol cations of Unfolding- sample period LDING AND FAST CONVOLUT ding transformation – Register n olding of Multirate systems. Fast c no grad Algorithm, Modified Wino GORITHMIC STRENGTH RED	ding, pro reductio TON ninimizir onvolutio grad Al	n and j ng tech on – C gorithr	s of paralle hnique Cook-T n -De	unfolding, el processi es –Regis Foom algo sign of Fa	Critical pa ng applicati ter minimit prithm, mod st Convolut	ath Unfolding ion. zation in fol- lified Cook-To tion algorithm	ning and 12 ded ook by 12
Retiming-deTechniques.URetiming applieUnit IIIFOFolding-Folding-architectures-Fealgorithm-Wiinspection.Unit IVALAlgorithmic str	efinitions and properties Retiming nfolding – an algorithm for Unfol cations of Unfolding- sample period LDING AND FAST CONVOLUT ding transformation – Register n olding of Multirate systems. Fast c no grad Algorithm, Modified Wino GORITHMIC STRENGTH RED ength reduction in Filters-Parallel F	ding, pro reductio TON ninimizir onvolutio grad Al	n and j ng tech on – C gorithr	s of paralle hnique Cook-T n -De	unfolding, el processi es –Regis Foom algo sign of Fa	Critical pa ng applicati ter minimit prithm, mod st Convolut	ath Unfolding ion. zation in fol- lified Cook-To tion algorithm	ning and 12 ded ook by 12
Retiming - de Techniques. U Retiming applie Unit III FO Folding - Fol architectures-Fe algorithm - Wi inspection. Unit IV AL Algorithmic str rank order Filte	efinitions and properties Retiming nfolding – an algorithm for Unfol cations of Unfolding- sample period LDING AND FAST CONVOLUT ding transformation – Register n olding of Multirate systems. Fast c no grad Algorithm, Modified Wino GORITHMIC STRENGTH RED ength reduction in Filters-Parallel F rs.	ding, pro reductio TON ninimizir onvolutio grad Al UCTION FIR Filter	n and p ng tecl on – C gorithr V rs, DC	s of paralle hnique Cook-T m -De T and	unfolding, el processi es –Regis Foom algo sign of Fa Inverse D	Critical pa ng applicati ter minimit orithm, mod st Convolut	ath Unfolding ion. zation in fol- lified Cook-To tion algorithm el architecture:	ning and 12 ded ook by 12
Retiming-deTechniques.URetiming applieUnit IIIFOFolding-Folding-architectures-Fealgorithm-wiinspection.UUnit IVALeAlgorithmic strrank order FilteUnit VPIP	efinitions and properties Retiming nfolding – an algorithm for Unfol cations of Unfolding- sample period LDING AND FAST CONVOLUT ding transformation – Register n olding of Multirate systems. Fast c no grad Algorithm, Modified Wino GORITHMIC STRENGTH RED ength reduction in Filters-Parallel F rs. ELINED AND PARALLEL REC	ding, pro reductio TON ninimizir onvolutio grad Al UCTION TR Filter URSIVE	n and p ng tech on – C gorithr V S, DC	s of paralle hnique cook-7 n -De T and	unfolding, el processi es –Regis Foom algo sign of Fa Inverse D ADAPTI	Critical pa ng applicati ter minimi orithm, mod st Convolut PCT, Paralle VE FILTE	ath Unfolding ion. zation in fol- lified Cook-To tion algorithm el architecture: RS	ming and 12 ded ook by 12 s for 12
Retiming-deTechniques.URetiming applidUnit IIIFOFolding-Folding-architectures-Fealgorithm-wiinspection.Unit IVALAAlgorithmic strrank order FilteUnit VPIPInefficient/effic	efinitions and properties Retiming nfolding – an algorithm for Unfol cations of Unfolding- sample period LDING AND FAST CONVOLUT ding transformation – Register n olding of Multirate systems. Fast c no grad Algorithm, Modified Wino GORITHMIC STRENGTH RED ength reduction in Filters-Parallel F rs. ELINED AND PARALLEL REC ient single channel interleaving, Lo	ding, pro reductio ION ninimizir onvolutio grad Al UCTION FIR Filter URSIVE ok- Ahea	n and p ng tecl on – C gorithr S, DC C FILT ad pipe	s of paralle hnique Cook-T n -De T and TERS elining	unfolding, el processi es –Regis Foom algo sign of Fa Inverse D ADAPTI g in first-	Critical pa ng applicati ter minimi orithm, mod st Convolut PCT, Paralle VE FILTE order IIR fi	ath Unfolding ion. zation in fol- lified Cook-To tion algorithm el architecture: RS Iters, Look-Al	ming and 12 ded ook by 12 s for 12 head
Retiming-deTechniques.URetiming applieUnit IIIFOFolding-Folding-architectures-Fealgorithm-winspection.Unit IVALeAlgorithmic strrank order FilteUnit VPIPInefficient/efficpipelining with	efinitions and properties Retiming nfolding – an algorithm for Unfol cations of Unfolding- sample period LDING AND FAST CONVOLUT ding transformation – Register n olding of Multirate systems. Fast c no grad Algorithm, Modified Wino GORITHMIC STRENGTH RED ength reduction in Filters-Parallel F rs. ELINED AND PARALLEL REC ient single channel interleaving, Lo power-of-two decomposition parall	ding, pro reductio TON ninimizir onvolutio grad Al UCTION FIR Filter URSIVE ok- Ahea el proces	ng tech on – C gorithr S, DC C FILT ad pipe sing o	s of paralle paralle hnique cook-7 m -De T and T and T ERS elining f IIR	unfolding, el processi es –Regis Foom algo sign of Fa Inverse D ADAPTI g in first-o filters, con	Critical pa ng applicati ter minimi orithm, mod st Convolut OCT, Paralle VE FILTE order IIR fi nbined pipe	ath Unfolding ion. zation in fol- lified Cook-To- tion algorithm el architecture: RS lters, Look-Al- lining and par	ming and 12 ded ook by 12 s for 12 head allel
Retiming-deTechniques.URetiming applidUnit IIIFOFolding-Folding-architectures-Fealgorithm-winspection.Unit IVALAlgorithmic strrank order FilteUnit VPIPInefficient/efficpipelining with	efinitions and properties Retiming nfolding – an algorithm for Unfol cations of Unfolding- sample period LDING AND FAST CONVOLUT ding transformation – Register n olding of Multirate systems. Fast c no grad Algorithm, Modified Wino GORITHMIC STRENGTH RED ength reduction in Filters-Parallel F rs. ELINED AND PARALLEL REC ient single channel interleaving, Lo	ding, pro reductio TON ninimizir onvolutio grad Al UCTION FIR Filter URSIVE ok- Ahea el proces	ng tech on – C gorithr S, DC C FILT ad pipe sing o	s of paralle paralle hnique cook-7 m -De T and T and T ERS elining f IIR	unfolding, el processi es –Regis Foom algo sign of Fa Inverse D ADAPTI g in first-o filters, con	Critical pa ng applicati ter minimi orithm, mod st Convolut OCT, Paralle VE FILTE order IIR fi nbined pipe	ath Unfolding ion. zation in fol- lified Cook-To- tion algorithm el architecture: RS lters, Look-Al- lining and par	ming and 12 ded ook by 12 s for 12 head allel
Retiming-deTechniques.URetiming applidUnit IIIFOFolding-Folding-architectures-Fealgorithm-winspection.Unit IVALAlgorithmic strrank order FilteUnit VPIPInefficient/efficpipelining with	efinitions and properties Retiming nfolding – an algorithm for Unfol cations of Unfolding- sample period LDING AND FAST CONVOLUT ding transformation – Register n olding of Multirate systems. Fast c no grad Algorithm, Modified Wino GORITHMIC STRENGTH RED ength reduction in Filters-Parallel F rs. ELINED AND PARALLEL REC ient single channel interleaving, Lo power-of-two decomposition parall	ding, pro reductio TON ninimizir onvolutio grad Al UCTION FIR Filter URSIVE ok- Ahea el proces	ng tech on – C gorithr S, DC C FILT ad pipe sing o	s of paralle paralle hnique cook-7 m -De T and T and T ERS elining f IIR	unfolding, el processi es –Regis Foom algo sign of Fa Inverse D ADAPTI g in first-o filters, con	Critical pa ng applicati ter minimi orithm, mod st Convolut OCT, Paralle VE FILTE order IIR fi nbined pipe	ath Unfolding ion. zation in fol- lified Cook-To- tion algorithm el architecture: RS lters, Look-Al- lining and par	ming and 12 ded ook by 12 s for 12 head allel
Retiming - de Techniques. U Retiming applie Unit III FO Folding – Fol architectures-Fe algorithm – Wi inspection. Unit IV AL Algorithmic str rank order Filte Unit V PIP Inefficient/effic pipelining with processing of II	efinitions and properties Retiming nfolding – an algorithm for Unfol cations of Unfolding- sample period LDING AND FAST CONVOLUT ding transformation – Register n olding of Multirate systems. Fast c no grad Algorithm, Modified Wino GORITHMIC STRENGTH RED ength reduction in Filters-Parallel F rs. ELINED AND PARALLEL REC ient single channel interleaving, Lo power-of-two decomposition parall R filters, pipelined adaptive digital t	ding, pro reductio TON ninimizir onvolutio grad Al UCTION FIR Filter URSIVE ok- Ahea el proces	ng tech on – C gorithr S, DC C FILT ad pipe sing o	s of paralle paralle hnique cook-7 m -De T and T and T ERS elining f IIR	unfolding, el processi es –Regis Foom algo sign of Fa Inverse D ADAPTI g in first-o filters, con	Critical pa ng applicati ter minimi orithm, mod st Convolut OCT, Paralle VE FILTE order IIR fi nbined pipe	ath Unfolding ion. zation in fol- lified Cook-To- tion algorithm el architecture: RS lters, Look-Al- lining and par	ming and 12 ded ook by 12 s for 12 head allel
Retiming - detection Techniques. U Retiming applie Unit III FO Folding - Folding - architectures-Fe algorithm Wi inspection. Mathematical Str Unit IV AL Algorithmic str rank order Filte Unit V PIP Inefficient/effic pipelining with processing of II REFERENCE(Parhi	efinitions and properties Retiming nfolding – an algorithm for Unfol cations of Unfolding- sample period LDING AND FAST CONVOLUT ding transformation – Register n olding of Multirate systems. Fast c no grad Algorithm, Modified Wino GORITHMIC STRENGTH RED ength reduction in Filters-Parallel F rs. ELINED AND PARALLEL REC ient single channel interleaving, Lo power-of-two decomposition parall R filters, pipelined adaptive digital t	ding, pro reductio ION ninimizir onvolutio grad Al UCTION TR Filter URSIVE ok- Ahea el proces filters-rel	n and p ng tech on – C gorithr V C FILT ad pipe sing o axed le	s of paralle paralle cook-7 m -De T and TERS elining f IIR	unfolding, el processi es –Regis Foom algo sign of Fa Inverse D ADAPTI g in first- filters, con head, pipe	Critical pa ng applicati ter minimi orithm, mod st Convolut OCT, Paralle OCT, Paralle VE FILTE order IIR fin bined pipe lined LMS a	ath Unfolding ion. zation in fol- lified Cook-To- tion algorithm el architecture: RS liters, Look-Al- lining and par adaptive filter.	ming and 12 ded ook by 12 s for 12 head callel
Retiming - de Techniques. U Retiming applie Unit III FO Folding - Folding - Folding - Folding - algorithm - algorithm - Unit IV AL Algorithmic str - rank order Filte - Unit V PIP Inefficient/effic - pipelining with - processing of II - REFERENCE(- 1 Parhi, Ke	efinitions and properties Retiming nfolding – an algorithm for Unfol cations of Unfolding- sample period LDING AND FAST CONVOLUT ding transformation – Register n olding of Multirate systems. Fast c no grad Algorithm, Modified Wino GORITHMIC STRENGTH RED ength reduction in Filters-Parallel F rs. ELINED AND PARALLEL REC ient single channel interleaving, Lo power-of-two decomposition parall R filters, pipelined adaptive digital f	ding, pro reductio ION ninimizir onvolutio grad Al UCTION TR Filter URSIVE ok- Ahea el proces filters-rel	n and p ng tech on – C gorithr V C FILT ad pipe sing o axed le	s of paralle paralle cook-7 m -De T and TERS elining f IIR	unfolding, el processi es –Regis Foom algo sign of Fa Inverse D ADAPTI g in first- filters, con head, pipe	Critical pa ng applicati ter minimi orithm, mod st Convolut OCT, Paralle OCT, Paralle VE FILTE order IIR fin bined pipe lined LMS a	ath Unfolding ion. zation in fol- lified Cook-To- tion algorithm el architecture: RS liters, Look-Al- lining and par adaptive filter.	ming and 12 ded ook by 12 s for 12 head callel
Retiming - detection Techniques. U Retiming applie Unit III FO Folding - Folding - architectures-Fe algorithm Wi inspection. Mathematical Unit IV AL Algorithmic str rank order Filte Unit V PIP Inefficient/effic pipelining with processing of II REFERENCE(1. Parhi, Ke Inter Sciel Sciel	efinitions and properties Retiming nfolding – an algorithm for Unfol cations of Unfolding- sample period LDING AND FAST CONVOLUT ding transformation – Register n olding of Multirate systems. Fast c no grad Algorithm, Modified Wino GORITHMIC STRENGTH RED ength reduction in Filters-Parallel F rs. ELINED AND PARALLEL REC ient single channel interleaving, Lo power-of-two decomposition parall R filters, pipelined adaptive digital f (S): eshab K., VLSI Digital Signal Proc	ding, pro reductio ION ninimizir onvolutio grad Al UCTION TR Filter URSIVE ok- Ahea el proces filters-rel	ng tech on – C gorithr V S, DC C FILT ad pipe sing o axed le	s of paralle paralle cook-T n -De T and T ERS elining f IIR f IIR s, Des	unfolding, el processi es –Regis Foom algo sign of Fa Inverse D ADAPTI g in first- filters, con head, pipe	Critical pa ng applicati ter minimi orithm, mod st Convolut OCT, Paralle OCT, Paralle VE FILTE order IIR fi nbined pipe lined LMS a mplementat	ath Unfolding ion. zation in fol lified Cook-To tion algorithm el architecture: RS liters, Look-Al lining and par adaptive filter.	ming and 12 ded ook i by 12 s for 12 head rallel

P.I. Chairman - BoS Dept.of ECE - ESEC

3.	www.pdf-search-engine.com/vlsi-signal-processing-pdf.html
4.	Magdy A. Bayoumi, Magdy A. Bayoumi, E. Swartzlander, VLSI Signal Processing Technology, Kluwer Academic Publishers.October 1994
5.	Ray Liu K J, High Performance VLSI Signal Processing, Innovative architectures and Algorithms, IEEE Press,2008

R.L.

Chairman - BoS Dept.of ECE - ESEC

Programme	ME-APPLIED I	ME-APPLIED ELECTRONICS						I
Course Code	Course Name	Course Name Hours / Cred		Credit	Total	Maximu		
		L	Т	Р	С	Hours	Marks	5
19AE203	LOW POWER VLSI DESIGN	3	0	0	3	45	100	
 Identify Power Identify Gain K 	etive (s): The purpose of learning this the power reduction techniques base dissipation mechanism in various May suitable techniques to reduce the po- nowledge about Power Estimation	sed on t OS logi ower di	echnol ic style ssipati	on.	ndependent	and technolo	gy dependent	t.
	tand Synthesis and software design f tive (s): The purpose of learning thi							
 Identif Power Identify Perform 	the power reduction techniques bas y the power reduction techniques bas dissipation mechanism in various Mo y suitable techniques to reduce the po the Synthesis and Software for Low	sed on t OS logi ower dis	techno ic style ssipati	logy d on.				
	WER DISSIPATION IN CMOS							9
Hierarchy of	limits of power - Sources of power	r consu	mptior	n – Ph	ysics of po	wer dissipati	ion in CMOS	FE
devices - Lon	g Channel and Submicron Effect-Ba	sic prin	nciple of	of low	power desi	gn.		
Unit II PO	OWER OPTIMIZATION							9
Logic level p	ower optimization - Circuit level	low pc	ower d	lesign	- circuit te	echniques fo	or reducing p	owe
consumption i	n adders and multipliers.							
Unit III DI	ESIGN OF LOW POWER CMOS	CIRC	UITS				2.1	9
Computer arit	hmetic techniques for low power sys	stem – r	reducin	ng pov	ver consum	ption in men	nories – low p	owe
clock, Inter co	nnect and layout design - Advanced	l techni	ques –	Specia	al technique	s.		
Unit IV PO	OWER ESTIMATION							9
Power Estima	tion techniques - logic power e	estimati	on -S	imulat	tion power	analysis-Pr	robabilistic p	owe
analysis.								
Unit V SY	NTHESIS AND SOFTWARE DE	SIGN	FOR I	LOW	POWER		1	9
Synthesis for l	ow power - Behavioral level transfo	orm – so	oftware	e desig	gn for low p	ower.		
			-					-
REFERENCE				6		1 I I I I I I I I I I I I I I I I I I I		
	k Roy and S.C.Prasad, Low power C			a subject to a sub	0.			
2. 2010.	os Soudris, Chirstian Pignet, Costas		-			cuits for Low	v Power, Kluv	wer,
3. J.B.Kul	o and J.H Lou, Low voltage CMOS	VLSI (Circuit	s, Wil	ey 2001			
4. A.P.Ch	andrasekaran and R.W.Broadersen,	Low po	wer di	igital (CMOS desig	gn, Kluwer,2	.010	
5. Gary Y	eap, Practical low power digital VLS	SI desig	gn, Klu	iwer, 2	2008.		T,	
	740 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7		200					
6. Abdelat	tif Belaouar, Mohamed.I.Elmasry, L	ow nov	ver die	rital V	LSI design	Kluwer, 200)5.	

Chairman - BoS Dept.of ECE - ESEC

Programme	ME-APPLIED	ELECTRONICS				R 2019	Semester	П
Course Code	Course Name	Hou	rs / We	eek	Credit	Total Maximum		
104 5204	WELL ADODATODY	L	L T	T P	С	Hours	Marks	
19AE204	VLSI LABORATORY	0	0	2	2	45	100	

Course Objective (s): The purpose of learning this course is to

- Design and simulation of digital circuits VHDL and Verilog
- •= Design FIR Filters.
- Design Real time clock using VHDL
- Design Neural Network Algorithms using MATLAB
- Design Genetic Algorithms using MATLAB

Course Outcomes: At the end of this course, learners will be able to:

- Simulation of Digital Circuits using Verilog
- Simulation of Digital Circuits using VHDL
- FPGA implementation of ALU and RTC
- FPGA implementation of FIR Filters.
- FPGA implementation of FFT Computation.

Exp No.	Name of Experiments
1	Design and Simulation of Combinational and sequential circuits using VHDL.
2	Design and Simulation of Combinational and sequential circuits using Verilog.
3	FPGA Implementation of FFT Computation
4	FPGA Implementation of FIR Filter (Low, High and Band pass)
5	FPGA Implementation of 4 Bit ALU & Power analysis.
6	FPGA Implementation of Real Time Clock & RTL view.
7	FPGA Implementation of Adaptive Signal Processing Algorithm
8	Implementation of Image Processing Algorithm using MATLAB.
9	Implementation of Neural networks Algorithms using MATLAB.
10	Implementation of Genetic Algorithm and PSO using MATLAB.

P.L. Chairman - BoS Dept.of ECE - ESEC

ELECTIVE-I

Programme	ME-APPLIED ELI	ME-APPLIED ELECTRONICS		ME-APPLIED ELECTRONICS R 2019 Semes			Semester	II
Course Code	Course Name	Hours / Week Credit				Total	Maximum	1
Course Code		L	T	Р	С	Hours	Marks	
19AEX01	SENSORS, ACTUATORS AND INTERFACE ELECTRONICS	3	0	0	3	45	100	
 Study th Study th Study A Study D Course Outcor Gain Kn 	ive (s): The purpose of learning this co e concepts of Measurement Systems, F e concepts of Self-Generating Sensors ctuators Drive Characteristics and App igital Sensors and Semiconductor Devi nes: At the end of this course, learners owledge of Measurement Systems, Re owledge of Self-Generating Sensors,	Resisti 3, olicatio ice Se 5 will b	ve And ons & nsors be able	to:		"S		
• Gain Kn	owledge of Actuators Drive Characteri owledge of Digital Sensors and Semico			State of the second				
	RODUCTION TO MEASUREMEN							9
resolution, system order, and second Unit II RE	of measurement systems, accuracy ematic errors, random errors, dynamic nd-order measurement systems and res SISTIVE AND REACTIVE SENSO	chara sponse RS	acteristi 2.	cs of i	measureme	ent systems:	eristics: linea : zero-order, t	first-
resolution, syster order, and secon Unit II RES Resistive senser dependent resiss compensation, variation and differential tra	ematic errors, random errors, dynamic ind-order measurement systems and res SISTIVE AND REACTIVE SENSO ors: potentiometers, strain gages, re tors, Signal conditioning for resistive Instrumentation amplifiers, sources electromagnetic sensors, capacitive insformers (LVDT), magneto elastic	chara sponse RS sistive senso of ir senso	e temp rs: Whe nterfere rs, diff	erature erature eatstor nce a ferenti	e detector ne bridge, s nd interfe al, inducti	ent systems: s, magneto sensor bridg rence redu ve sensors	eristics: linea : zero-order, f o resistors, li ge calibration action, React s, linear vari	ight- ance able
resolution, syste order, and secon Unit II RES Resistive sense dependent resis compensation, variation and differential trans reactance-based	ematic errors, random errors, dynamic ind-order measurement systems and res SISTIVE AND REACTIVE SENSO ors: potentiometers, strain gages, re- tors, Signal conditioning for resistive Instrumentation amplifiers, sources electromagnetic sensors, capacitive insformers (LVDT), magneto elastic I sensors & application to the LVDT.	chara sponse RS sistive senso of ir senso	e temp rs: Whe nterfere rs, diff	erature erature eatstor nce a ferenti	e detector ne bridge, s nd interfe al, inducti	ent systems: s, magneto sensor bridg rence redu ve sensors	eristics: linea : zero-order, f o resistors, li ge calibration action, React s, linear vari	arity first- ight- ance able for
resolution, syste order, and secon Unit II RES Resistive sense dependent resis compensation, variation and differential trais reactance-based Unit III SEI Self-generating sensors, electro	ematic errors, random errors, dynamic ind-order measurement systems and res SISTIVE AND REACTIVE SENSO ors: potentiometers, strain gages, re tors, Signal conditioning for resistive Instrumentation amplifiers, sources electromagnetic sensors, capacitive insformers (LVDT), magneto elastic	chara sponse RS sistive senso of ir senso senso iezoel	e temp rs: Who nterfere rs, diff sors, ha ectric or self-	erature eatstor nce a ferenti all eff sensor	e detector ne bridge, s nd interfe al, inducti fect sensor rs, pyroeld ating sens	ent systems: s, magneto sensor bridg rence redu ve sensors rs, Signal ectric sense ors: chopp	eristics: linea : zero-order, f o resistors, li ge calibration action, React s, linear vari conditioning ors, photovo per and low-	first- gight- and ance able for 9 Itaic
resolution, syster order, and second Unit II RES Resistive senser dependent resis compensation, variation and differential transferential transferential reactance-based Unit III SEI Self-generating sensors, electro amplifiers, offser	ematic errors, random errors, dynamic ind-order measurement systems and res SISTIVE AND REACTIVE SENSO ors: potentiometers, strain gages, re- tors, Signal conditioning for resistive Instrumentation amplifiers, sources electromagnetic sensors, capacitive insformers (LVDT), magneto elastic sensors & application to the LVDT. LF-GENERATING SENSORS sensors: thermoelectric sensors, pro- chemical sensors, Signal conditioni	chara sponse RS esistive senso of ir senso senso iezoel ing for mplifie	e temp rs: Whe nterfere rs, diff cors, ha ectric or self- ers, cha	erature eatstor nce a ferenti all eff sensor genera	e detector ne bridge, s nd interfe al, inducti fect sensor rs, pyroele ating sens nplifiers, n	ent systems: s, magneto sensor bridg rence redu ve sensors rs, Signal ectric senso ors: chopp oise in amp	eristics: linea : zero-order, f o resistors, li ge calibration action, React s, linear vari conditioning ors, photovo per and low-	arity first- first- and ance able for ltaic drift
resolution, syste order, and secon Unit II RES Resistive sense dependent resis compensation, variation and differential transformed variation and differential transformed unit III SEI Self-generating sensors, electro amplifiers, offse Unit IV AC Relays, Solenoi to-20 mA Drive	ematic errors, random errors, dynamic ind-order measurement systems and res SISTIVE AND REACTIVE SENSO ors: potentiometers, strain gages, re- tors, Signal conditioning for resistive Instrumentation amplifiers, sources electromagnetic sensors, capacitive insformers (LVDT), magneto elastic sensors & application to the LVDT. LF-GENERATING SENSORS sensors: thermoelectric sensors, pro- chemical sensors, Signal conditioning et and drifts amplifiers, electrometer ar	chara sponse RS esistive senso of ir senso senso senso iezoel ing for mplific STIC	e temp rs: Whe nterfere rs, diff cors, ha ectric or self- ers, cha S AND ors, Ser	erature eatstor nce a ferenti all eff sensor genera rge an APPI vo Mo	e detector ne bridge, s nd interfe al, inducti fect sensor rs, pyroele ating sens nplifiers, n LICATIO	ent systems: s, magneto sensor bridg rence redu ve sensors rs, Signal ectric sense ors: chopp oise in amp NS notors and	eristics: linea : zero-order, f o resistors, li ge calibration action, React s, linear vari conditioning ors, photovo per and low- olifiers.	rity, first- first- and ance able for ltaic drift 9 1, 4-
resolution, syster order, and secon Unit II RES Resistive sense dependent resis compensation, variation and differential trais reactance-based Unit III SEI Self-generating sensors, electro amplifiers, offse Unit IV AC Relays, Solenoi to-20 mA Drive and digital-to-res	ematic errors, random errors, dynamic ind-order measurement systems and ress SISTIVE AND REACTIVE SENSO ors: potentiometers, strain gages, re- tors, Signal conditioning for resistive Instrumentation amplifiers, sources electromagnetic sensors, capacitive insformers (LVDT), magneto elastic sensors & application to the LVDT. IF-GENERATING SENSORS sensors: thermoelectric sensors, pro- chemical sensors, Signal conditioning et and drifts amplifiers, electrometer and TUATORS DRIVE CHARACTERIS d drive, Stepper Motors, Voice-Coil a e, Hydraulic actuators, variable transformers	chara sponse RS esistive senso of ir senso senso senso iezoel ing for mplific STIC	e temp rs: When terfere rs, diff cors, ha ectric or self- ers, cha S AND ors, Ser : synch	eratur eatstor nce a ferenti all eff sensor genera rrge an APPI vo Mo ros, re	e detector ne bridge, s nd interfe al, inducti fect sensor rs, pyroele ating sens nplifiers, n LICATIO ptors, DC r esolvers, In	ent systems: s, magneto sensor bridg rence redu ve sensors rs, Signal ectric senso ors: chopp oise in amp NS notors and ductosyn, r	eristics: linea : zero-order, f o resistors, li ge calibration action, React s, linear vari conditioning ors, photovo per and low- olifiers.	rity first ght ance able for ltaic driff 9 1, 4-

Chairman - BoS of ECE - ESEC

	odiodes and phototransistors, sensors based on MOSFET transistors, CCD imaging sensors , ultrasonic ors, fiber-optic sensors.
REF	ERENCE(S):
1.	Andrzej M. Pawlak Sensors and Actuators in Mechatronics Design and Applications, 2016.
2.	D. Johnson, Process Control Instrumentation Technology, John Wiley and Sons.
3.	D.Patranabis, Sensors and Transducers, TMH 2013.
4.	E.O. Doeblin, Measurement System : Applications and Design, McGraw Hill publications
5.	Graham Brooker, Introduction to Sensors for ranging and imaging, Yesdee, 2009.

R.Lo

Chairman - BoS Dept.of ECE - ESEC

Pr	ogramme	ME-APPLIED	ELECTI	RONIC	CS		R 2019	Semester	II
Course Code		Course Name	Hours / Week Credi		Credit	Total	Maxim	um	
Co	urse Code	Course Name	L	Т	Р	С	Hours	Mar	ks
		COMPUTER							
1	9AEX02	ARCHITECTURE AND	3	0	0	3	45	100	
		PARALLEL PROCESSING							
Co	urse Objec	tive (s): The purpose of learning this	s course i	is to					
	 Concept 	ts of Computer Design And Perform	ance Me	asures,	Parall	el Processi	ng, Pipelini	ng and ILP	
	• Concep	ts of Memory Hierarchy Design, M	ultiproce	ssors &	z Multi	-Core Arch	nitectures		
Co	urse Outco	mes: At the end of this course, learn	ners will l	be able	to:				
	Knowle	dge of Computer Design And Perfo	ormance I	Measur	es, Par	allel Proce	ssing, Pipel	ining and IL	Р
		nowledge of Memory Hierarchy De	-				ore Archited	ctures	
Un		MPUTER DESIGN AND PERFO	Contraction of the State Sta	an erb i wowers	and menorities and				9
		of Computer Design - Parallel and							
		ctures - Multithreaded architectur	res – Sta	anford	Dash	multiproc	essor – Ks	SR1 - Data	-flov
arc	hitectures -	Performance Measures.					1		
Uni	it II PA	RALLEL PROCESSING, PIPEL	INING A	AND II	LP				9
Ins	truction Le	vel Parallelism and Its Exploitation	on - Cor	ncepts	and C	hallenges	- Pipelinin	g processors	s -
0									
UV	ercoming D	ata Hazards with Dynamic Schedul	ling – Dy	namic		h Predictio			ple
		ata Hazards with Dynamic Schedul rs - Performance and Efficiency in A			Branc		n - Specula		ple
Issi	le Processo				Branc		n - Specula		
lssı Uni	ie Processo t III MI	rs - Performance and Efficiency in A	Advanced	l Multij	Branc ple Issi	le Processo	n - Specula ors.	ition - Multij	9
Issi Uni Me	t III MI mory Hiera	rs - Performance and Efficiency in A EMORY HIERARCHY DESIGN	Advanced	l Multij tions –	Branc ple Issu Cache	e memory	n - Specula ors. – Optimiza	ition - Multij	9
Issu Uni Me Per	t III MI mory Hiera formance –	rs - Performance and Efficiency in A EMORY HIERARCHY DESIGN archy - Memory Technology and C	Advanced	l Multij tions –	Branc ple Issu Cache	e memory	n - Specula ors. – Optimiza	ition - Multij	9 che
Issi Uni Me Per Uni	t III MI mory Hiera formance – t IV MU	rs - Performance and Efficiency in A EMORY HIERARCHY DESIGN archy - Memory Technology and O Memory Protection and Virtual Me	Advanced Optimizat mory - D	l Multij tions – Design c	Branc ple Issu Cacho of Mem	e memory hory Hierar	n - Specula ors. – Optimiza chies.	ation - Multip	9 iche 9
Issu Uni Me Per Uni Syr	t III MI mory Hiera formance – t IV MU nmetric and	rs - Performance and Efficiency in A EMORY HIERARCHY DESIGN archy - Memory Technology and C Memory Protection and Virtual Me JLTIPROCESSORS	Advanced Optimizat mory - D tectures -	tions – Design c – Cach	Branc ple Issu Cacho of Men e cohe	e Processo e memory hory Hierar	n - Specula ors. – Optimiza chies. es – Perfor	ation - Multip ations of Ca rmance Issue	9 che 9 es –
Issu Uni Me Per Uni Syr Syr	t III MI mory Hiera formance – t IV MU nmetric and	rs - Performance and Efficiency in A EMORY HIERARCHY DESIGN Irchy - Memory Technology and O Memory Protection and Virtual Me ULTIPROCESSORS I distributed shared memory architen issues – Models of Memory Con	Advanced Optimizat mory - D tectures -	tions – Design c – Cach	Branc ple Issu Cacho of Men e cohe	e Processo e memory hory Hierar	n - Specula ors. – Optimiza chies. es – Perfor	ation - Multip ations of Ca rmance Issue	9 che 9 es –
Issu Uni Per Uni Syr Syr	t III MI mory Hiera formance – t IV MI nmetric and achronizatio lti-stage swi	rs - Performance and Efficiency in A EMORY HIERARCHY DESIGN Irchy - Memory Technology and O Memory Protection and Virtual Me ULTIPROCESSORS I distributed shared memory architen issues – Models of Memory Con	Advanced Optimizat mory - D tectures -	tions – Design c – Cach	Branc ple Issu Cacho of Men e cohe	e Processo e memory hory Hierar	n - Specula ors. – Optimiza chies. es – Perfor	ation - Multip ations of Ca rmance Issue	9 che 9 es –
Issi Uni Per Uni Syr Syr mu	Image: Processot IIIMImoryHieraformance –t IVMImmetricandand thromizatiolti-stageswitt VMI	rs - Performance and Efficiency in A EMORY HIERARCHY DESIGN archy - Memory Technology and C Memory Protection and Virtual Me ULTIPROCESSORS d distributed shared memory archit in issues – Models of Memory Con itches.	Advanced Dptimizat mory - D tectures - nsistency	i Multij tions – Design c – Cach - Inter	Branc ple Issu Cacho of Men e cohe rconne	e memory hory Hierar erence issu	n - Specula ors. – Optimiza chies. es – Perfor orks – Bus	ations of Ca rmance Issue es, crossbar	9 iche 9 es – and 9
Issu Uni Me Per Uni Syr Syr Mu Uni Sof	Image: Processot IIIMImoryHieraformancet IVMInmetricandachronizatiolti-stageswitt VMIttwareandlti-corearch	rs - Performance and Efficiency in A EMORY HIERARCHY DESIGN Irchy - Memory Technology and O Memory Protection and Virtual Me ULTIPROCESSORS Id distributed shared memory architen issues – Models of Memory Con itches. ULTI-CORE ARCHITECTURES hardware multithreading – SMT an hitecture – SUN CMP architecture –	Advanced Dptimiza mory - D tectures - nsistency d CMP a	i Multij tions – Design c – Cach - Inter architec	Branc ple Issu Cacho of Mem e cohe rconne	e memory hory Hierar erence issu ction netwo	n - Specula ors. – Optimiza chies. es – Perfor orks – Bus	ations of Ca rmance Issue es, crossbar	9 iche 9 es – and 9
Issu Uni Me Per Uni Syr Syr Mu Uni Sof	ue Processo t III MI mory Hiera formance – t t IV MI nmetric and achronization tion iti-stage switter t V MI tware and	rs - Performance and Efficiency in A EMORY HIERARCHY DESIGN Irchy - Memory Technology and O Memory Protection and Virtual Me ULTIPROCESSORS Id distributed shared memory architen issues – Models of Memory Con itches. ULTI-CORE ARCHITECTURES hardware multithreading – SMT an hitecture – SUN CMP architecture –	Advanced Dptimiza mory - D tectures - nsistency d CMP a	i Multij tions – Design c – Cach - Inter architec	Branc ple Issu Cacho of Mem e cohe rconne	e memory hory Hierar erence issu ction netwo	n - Specula ors. – Optimiza chies. es – Perfor orks – Bus	ations of Ca rmance Issue es, crossbar	9 iche 9 es – and 9
Issu Uni Me Per Uni Syr Syr Mu Uni Sof	t III MI mory Hiera formance – t IV MI nmetric and hchronizatio ti-stage swi t V MI tware and h lti-core arch FERENCE	rs - Performance and Efficiency in A EMORY HIERARCHY DESIGN archy - Memory Technology and C Memory Protection and Virtual Me ULTIPROCESSORS d distributed shared memory architen issues – Models of Memory Con itches. ULTI-CORE ARCHITECTURES hardware multithreading – SMT an hitecture – SUN CMP architecture – (S):	Advanced Dptimiza mory - D tectures - nsistency d CMP a IBM cel	1 Multij tions – Design c – Cach - Inter architec 1 archit	Branc ple Issu Cacho of Men e cohe rconne ctures - ectures	e memory hory Hierar erence issu ction netwo – Design is – hp archit	n - Specula ors. – Optimiza chies. es – Perfor orks – Bus ssues – Cas ecture.	ations of Ca rmance Issue es, crossbar se-studies –	9 che 9 es – and 9 Intel
Issu Uni Me Per Uni Syr Syr Mu Uni Soff Mu RE	t III MI mory Hiera formance – t IV MI nmetric and ti-stage swi t V MI tware and I lti-core arch FERENCE	rs - Performance and Efficiency in A EMORY HIERARCHY DESIGN archy - Memory Technology and C Memory Protection and Virtual Me JLTIPROCESSORS d distributed shared memory architen issues – Models of Memory Con itches. JLTI-CORE ARCHITECTURES hardware multithreading – SMT an hitecture – SUN CMP architecture – (S): Culler, Jaswinder Pal Singh, Paralle	Advanced Dptimiza mory - D tectures - nsistency d CMP a IBM cel	1 Multij tions – Design c – Cach - Inter architec 1 archit	Branc ple Issu Cacho of Men e cohe rconne ctures - ectures	e memory hory Hierar erence issu ction netwo – Design is – hp archit	n - Specula ors. – Optimiza chies. es – Perfor orks – Bus ssues – Cas ecture.	ations of Ca rmance Issue es, crossbar se-studies –	9 che 9 es – and 9 Intel
Issu Uni Me Per Uni Syr Syr Mu Uni Soff Mu RE	ae Processo t III MI mory Hiera formance – t t IV MI nmetric and achronization achronization hti-stage switter t V MI tware and I lti-core arch FERENCE David E. Morgan I Morgan I	rs - Performance and Efficiency in A EMORY HIERARCHY DESIGN archy - Memory Technology and C Memory Protection and Virtual Me JLTIPROCESSORS d distributed shared memory architent in issues – Models of Memory Con- itches. JLTI-CORE ARCHITECTURES hardware multithreading – SMT and hitecture – SUN CMP architecture – (S): Culler, Jaswinder Pal Singh, Paralle Kaufmann / Elsevier, 2007.	Advanced Dptimizat mory - D tectures - nsistency d CMP a IBM cel el Compu	tions – Design c – Cach – Cach – Inter architec I architec	Branc ple Issu Cacho of Men e cohe rconne ctures - ecture rchitec	e memory hory Hierar erence issu ction netwo – Design is – hp archit ture: A har	n - Specula ors. – Optimiza chies. es – Perfor orks – Bus ssues – Cas ecture. dware/ soft	ations of Ca rmance Issue es, crossbar se-studies – ware approa	9 cche 9 es – and 9 Intel
Issu Uni Me Per Uni Syr Syr Mu Soff Mu RE	t III MI mory Hiera formance – t IV MI nmetric and achronizatio ti-stage swi t V MI tware and I lti-core arch FERENCE David E. Morgan I Dimitrios	rs - Performance and Efficiency in A EMORY HIERARCHY DESIGN archy - Memory Technology and C Memory Protection and Virtual Me JLTIPROCESSORS I distributed shared memory architention issues – Models of Memory Con- itches. JLTI-CORE ARCHITECTURES hardware multithreading – SMT an- hitecture – SUN CMP architecture – (S): Culler, Jaswinder Pal Singh, Parallec Kaufmann / Elsevier, 2007. S Soudris, Axel Jantsch, Scalable Mu	Advanced Dptimizat mory - D tectures - nsistency d CMP a IBM cel el Compu	tions – Design c – Cach – Cach – Inter architec I architec	Branc ple Issu Cacho of Men e cohe rconne ctures - ecture rchitec	e memory hory Hierar erence issu ction netwo – Design is – hp archit ture: A har	n - Specula ors. – Optimiza chies. es – Perfor orks – Bus ssues – Cas ecture. dware/ soft	ations of Ca rmance Issue es, crossbar se-studies – ware approa	9 cche 9 es – and 9 Intel
Issu Uni Me Per Uni Syr Syr Mu Sof Mu RE 1.	ae Processo t III MI mory Hiera formance – t IV MI nmetric and achronization achronization tticted achronization tticted metric and achronization tticted tticted <td>rs - Performance and Efficiency in A EMORY HIERARCHY DESIGN archy - Memory Technology and C Memory Protection and Virtual Me JLTIPROCESSORS d distributed shared memory architent issues – Models of Memory Con- itches. JLTI-CORE ARCHITECTURES hardware multithreading – SMT and hitecture – SUN CMP architecture – (S): Culler, Jaswinder Pal Singh, Paralle Kaufmann / Elsevier, 2007. S Soudris, Axel Jantsch, Scalable Ma 2012.</td> <td>Advanced Dptimizat mory - D tectures - nsistency d CMP a IBM cel el Compu</td> <td>d Multij tions – Design c – Cach - Cach - Inter architec l architec duting At</td> <td>Branc ple Issu Cacho of Men e cohe rconne ectures rchitec</td> <td>e memory hory Hierar erence issu ction netwo - Design is - hp archit ture: A har : Design M</td> <td>n - Specula ors. – Optimiza chies. es – Perfor orks – Bus ssues – Cas ecture. dware/ soft</td> <td>ations of Ca rmance Issue es, crossbar se-studies – ware approa</td> <td>9 cche 9 es – and 9 Intel</td>	rs - Performance and Efficiency in A EMORY HIERARCHY DESIGN archy - Memory Technology and C Memory Protection and Virtual Me JLTIPROCESSORS d distributed shared memory architent issues – Models of Memory Con- itches. JLTI-CORE ARCHITECTURES hardware multithreading – SMT and hitecture – SUN CMP architecture – (S): Culler, Jaswinder Pal Singh, Paralle Kaufmann / Elsevier, 2007. S Soudris, Axel Jantsch, Scalable Ma 2012.	Advanced Dptimizat mory - D tectures - nsistency d CMP a IBM cel el Compu	d Multij tions – Design c – Cach - Cach - Inter architec l architec duting At	Branc ple Issu Cacho of Men e cohe rconne ectures rchitec	e memory hory Hierar erence issu ction netwo - Design is - hp archit ture: A har : Design M	n - Specula ors. – Optimiza chies. es – Perfor orks – Bus ssues – Cas ecture. dware/ soft	ations of Ca rmance Issue es, crossbar se-studies – ware approa	9 cche 9 es – and 9 Intel
Issu Uni Me Per Uni Syr Syr Mu Sof Mu RE 1.	Ile Processot IIIMImoryHieraformance–t IVMInmetricandachronizationachronizationachronizationachronizationachronizationachronizationachronizationachronizationachronizationachronizationachronizationachronizationachronizationachronizationbailbailbailbailbailbailbailbailbailbailbailbailbailbailbailachronizationbailbailachronizationachronizationbail <td>rs - Performance and Efficiency in A EMORY HIERARCHY DESIGN archy - Memory Technology and C Memory Protection and Virtual Me JLTIPROCESSORS d distributed shared memory architen in issues – Models of Memory Con- itches. JLTI-CORE ARCHITECTURES hardware multithreading – SMT an- hitecture – SUN CMP architecture – G(S): Culler, Jaswinder Pal Singh, Parallec Kaufmann / Elsevier, 2007. S Soudris, Axel Jantsch, Scalable Ma 2012. Briggs, Computer Architecture and p</td> <td>Advanced Dptimiza mory - D tectures - nsistency d CMP a IBM cel el Compu ulti-core arallel pr</td> <td>d Multij tions – Design o – Cach - Inter architec l archite uting Al Archite</td> <td>Branc ple Issu Cacho of Men e cohe rconne ctures - ectures rchitec</td> <td>e memory hory Hierar erence issu ction netwo - Design is - hp archit ture: A har : Design M Graw Hill,</td> <td>n - Specula ors. – Optimiza chies. es – Perfor orks – Bus ssues – Cas ecture. dware/ soft ethodologie 2004.</td> <td>ations of Ca rmance Issue es, crossbar se-studies – ware approad</td> <td>9 che 9 es – and 9 Intel</td>	rs - Performance and Efficiency in A EMORY HIERARCHY DESIGN archy - Memory Technology and C Memory Protection and Virtual Me JLTIPROCESSORS d distributed shared memory architen in issues – Models of Memory Con- itches. JLTI-CORE ARCHITECTURES hardware multithreading – SMT an- hitecture – SUN CMP architecture – G(S): Culler, Jaswinder Pal Singh, Parallec Kaufmann / Elsevier, 2007. S Soudris, Axel Jantsch, Scalable Ma 2012. Briggs, Computer Architecture and p	Advanced Dptimiza mory - D tectures - nsistency d CMP a IBM cel el Compu ulti-core arallel pr	d Multij tions – Design o – Cach - Inter architec l archite uting Al Archite	Branc ple Issu Cacho of Men e cohe rconne ctures - ectures rchitec	e memory hory Hierar erence issu ction netwo - Design is - hp archit ture: A har : Design M Graw Hill,	n - Specula ors. – Optimiza chies. es – Perfor orks – Bus ssues – Cas ecture. dware/ soft ethodologie 2004.	ations of Ca rmance Issue es, crossbar se-studies – ware approad	9 che 9 es – and 9 Intel
Issu Uni Me Per Uni Syr Syr Mu Uni Sof Mu RE 1. 2. 3.	t III MI mory Hiera formance – t IV MI nmetric and ti-stage swi t V MI tware and h lti-core arch FERENCE David E. Morgan h Dimitrios Springer, Hwang B John L. H	rs - Performance and Efficiency in A EMORY HIERARCHY DESIGN archy - Memory Technology and C Memory Protection and Virtual Me JLTIPROCESSORS I distributed shared memory architention issues – Models of Memory Con- itches. JLTI-CORE ARCHITECTURES hardware multithreading – SMT an- hitecture – SUN CMP architecture – (S): Culler, Jaswinder Pal Singh, Paralle Kaufmann / Elsevier, 2007. I Soudris, Axel Jantsch, Scalable Ma 2012. Briggs, Computer Architecture and p- Hennessey and David A. Patterson, C	Advanced Dptimiza mory - D tectures - nsistency d CMP a IBM cel el Compu ulti-core arallel pr	d Multij tions – Design o – Cach - Inter architec l archite uting Al Archite	Branc ple Issu Cacho of Men e cohe rconne ctures - ectures rchitec	e memory hory Hierar erence issu ction netwo – Design is – hp archit ture: A har : Design M Graw Hill,	n - Specula ors. – Optimiza chies. es – Perfor orks – Bus ssues – Cas ecture. dware/ soft ethodologie 2004.	ations of Ca rmance Issue es, crossbar se-studies – ware approad	9 che 9 es – and 9 Intel
Issu Uni Me Per Uni Syr Syr Mu Uni Sof Mu RE	ae Processo t III MI mory Hiera formance – t IV MI nmetric and achronization – achronization – achronization – achronization – bti-stage switted tware and I lti-core arch FERENCE – David E. Morgan I Dimitrios Springer, Hwang B John L. F Kaufman –	rs - Performance and Efficiency in A EMORY HIERARCHY DESIGN archy - Memory Technology and C Memory Protection and Virtual Me JLTIPROCESSORS d distributed shared memory architen in issues – Models of Memory Con- itches. JLTI-CORE ARCHITECTURES hardware multithreading – SMT an- hitecture – SUN CMP architecture – G(S): Culler, Jaswinder Pal Singh, Parallec Kaufmann / Elsevier, 2007. S Soudris, Axel Jantsch, Scalable Ma 2012. Briggs, Computer Architecture and p	Advanced Dptimiza mory - D tectures - nsistency d CMP a IBM cel el Compu ulti-core - arallel pr Computer	d Multij tions – Design c – Cach – Cach – Inter architec l architec l archite viting Archite rocessir r Archite	Branc ple Issu Cacho of Men e cohe rconne ctures - ectures rchitec ectures ng, Mc tecture	e memory hory Hierar erence issu ction netwo – Design is – hp archit ture: A har : Design M Graw Hill, – A quanti	n - Specula ors. – Optimiza chies. es – Perfor orks – Bus ssues – Cas ecture. dware/ soft ethodologie 2004.	ations of Ca rmance Issue es, crossbar se-studies – ware approad	9 che 9 es – and 9 Intel

le Chairman - BoS Dept.of ECE - ESEC *

CodeCourse NameK03HARDWARE - SOFTWARE CO-DESIGNDbjective (s): The purpose of learning this udy the concepts of System Specification A udy the concepts of Hardware / Software C	Hou	ME-APPLIED ELECTRONICS							
HARDWARE - SOFTWARE CO-DESIGN Dbjective (s): The purpose of learning this udy the concepts of System Specification A	L	irs / W	eek	Credit	Total	Maximu			
CO-DESIGN Dbjective (s): The purpose of learning this udy the concepts of System Specification A	~	Т	Р	C	Hours	Marks			
udy the concepts of System Specification A	3	0	0	3	45	100			
	course	is to							
Decification And Verification Dutcomes: At the end of this course, learne	Co-Synt	hesis,	Prototy				-		
ain Knowledge of System Specification an ain Knowledge of Hardware / Software Co d Verification						and the second se	catio		
SYSTEM SPECIFICATION AND MO	ODELI	LING				2010	9		
ed Systems, Hardware/Software Co-Design for Heterogeneous Implementation - Single processor Architectures, Comparison of Co-1 edded System Specification.	-Proces	ssor Ai	chitect	ures with	one ASIC a	nd many AS	Cs,		
HARDWARE / SOFTWARE PARTI	ΓΙΟΝΙ	NG					9		
ng Graph, Formulation of the HW/SW Par stic Scheduling, HW/SW Partitioning based HARDWARE / SOFTWARE CO-SYI	d on Ge NTHES	enetic A	Algorit	hms.			9		
Synthesis Problem, State-Transition Gra n for Distributed System- Case Studies wit					er Generati	on, Co-Synt			
PROTOTYPING AND EMULATION	1						9		
ion, Prototyping and Emulation Technic nents in Emulation and Prototyping ,Targ communication Infrastructure, Target Arch	get Arc itecture	hitectures and a	ire- Ar Applica	chitecture ation Syste	Specializati m Classes,	ion Techniqu Architectures	es , for		
Dominated Systems, Architectures for Data	DIFIC	ATIO	N	1					
Dominated Systems, Architectures for Data					V:6:	1	9		
Design Specification Languages Note: Specification Languages Design System Level Specification Languages Design System Specification Languages Design System Specification Languages Design System Specification Languages Design Specification Specification Languages Design Specification Specification Languages Design Specification Specification Specification Languages Design Specification	ons, Int vel Spe	terfacii cificat	ng Con ion ,De	esign Repr	esentation f	or System Le	9 for evel		
Design Specification and Design System-Level system Level Specification Languages n. NCE(S):	ons, Int vel Spe s, Hete	terfacin cificat rogene	ng Con ion ,De cous Sj	esign Reproduction	esentation f n and Mult	for System Le ti-Language	9 for evel Co-		
Design Specification and Design System-Level New System Level Specification Languages NCE(S): vanni De Micheli, Rolf Ernst Morgon, lishers,2011.	ons, Int vel Spe s, Hete Readi	terfacin ecificat rogene ng in	ng Con ion ,De cous Sj Hardv	esign Repr pecification ware/Softw	esentation f n and Mult are Co-Des	for System La ti-Language sign, Kaufma	9 for evel Co-		
Design Specification And Ver ney, Coordinating Concurrent Computation evel Specification and Design System-Level system Level Specification Languages n. NCE(S): vanni De Micheli, Rolf Ernst Morgon,	ons, Int vel Spe s, Hete Readi	terfacin ecificat rogene ng in	ng Con ion ,De cous Sj Hardv	esign Repr pecification ware/Softw	esentation f n and Mult are Co-Des	for System La ti-Language sign, Kaufma	9 for evel Co-		
Domin DE ncy, (evel S , Syst	Coordinating Concurrent Computation Specification and Design System-Leven	Coordinating Concurrent Computations, Int Specification and Design System-Level Spe	Coordinating Concurrent Computations, Interfacin Specification and Design System-Level Specificat	Specification and Design System-Level Specification ,De	Coordinating Concurrent Computations, Interfacing Components, Specification and Design System-Level Specification, Design Repr	Coordinating Concurrent Computations, Interfacing Components, Verification Specification and Design System-Level Specification, Design Representation f			

Chairman - BoS Dept.of ECE - ESEC

Programme	ME-APPLIED E	LECTR	RONIC	S		R 2019	Semester	П
Course Code 19AEX04	Course Name	Hours / Week Credit				Total	Maximu	ım
	Course Name	L T P		С	Hours	Mark	s	
	PROGRAMMABLE LOGIC CONTROLLERS	3	0	0	3	45	100	
Course Object	ive (s): The purpose of learning this	course i	is to					
Study the	e concepts of Programmable Logic	Controll	er, Bas	ic PLO	C Programi	ning		
Study the	e concepts of Advanced PLC Progra	amming,	PLC I	nstalla	tion and T	roubleshoot	ing & PLC	
Commu	nication and its Applications			43				
	nes: At the end of this course, learn							
Gain Kn	owledge of Programmable Logic C	ontroller	r, Basic	PLC	Programm	ing		
	owledge of Advanced PLC Program	nming, I	PLC In	stallat	ion and Tro	oubleshootir	ng & PLC	
Commu	nication and its Applications							
	oduction to Programmable Logic		11162-2					9
	Programmable Logic Controller - 1							-
	C vs Computer - PLC Size and a							
•	- CPU - Memory design and types	– Progi	rammir	ng dev	ices – Rec	ording and	Retrieving of	data -
PLC Workstatio	ons			1.1				1 -
Unit II Basic	PLC Programming							9
Relay-Type Ins diagram – Eleo	of Logic – Processor Memory Orga tructions - Instruction addressing – ctromagnetic Control relays – Cor perated switches	Branch	and Int	ernal	relay instru	uctions - En	tering the L	adder
Relay-Type Ins diagram – Elec Mechanically o U nit III Adv a	of Logic – Processor Memory Orga tructions - Instruction addressing – ctromagnetic Control relays – Cor perated switches	Branch ntactors	and Int – Mot	ernal or Sta	relay instru rters – Ma	uctions – En anual opera	ntering the L ted switche	adder s and
Relay-Type Ins diagram – Elec Mechanically o Unit III Adva Programming	of Logic – Processor Memory Orga tructions - Instruction addressing – ctromagnetic Control relays – Cor perated switches	Branch ntactors	and Int – Mot	ternal or Sta	relay instru rters – Ma ol Instruc	uctions – En anual opera	ntering the L ted switche	adder s and
Relay-Type Ins diagram – Elec Mechanically o Unit III Adva Programming Instructions – N	of Logic – Processor Memory Orga tructions - Instruction addressing – ctromagnetic Control relays – Cor perated switches Inced PLC Programming Timers – Programming Counters	Branch ntactors s – Pro hift Regi	and Int – Mot	ternal or Sta	relay instru rters – Ma ol Instruc	uctions – En anual opera	ntering the L ted switche	adden s and 9 lation
Relay-Type Ins diagram – Elec Mechanically o Unit III Adva Programming Instructions – M Unit IV PLC PLC Enclosure – Program Ed	of Logic – Processor Memory Orga tructions - Instruction addressing – etromagnetic Control relays – Cor perated switches Inced PLC Programming Timers – Programming Counters fath Instructions – Sequencer and S Installation and Troubleshooting es – Electrical Noise – Leaky Inputs iting – Programming and Monitori	Branch ntactors s – Pro hift Regi s and Ou ng – Pro	and Int – Mot ogram ister In utputs - eventiv	Contr structi - Grou e Mai	relay instru rters – Ma ol Instruc ons. unding – V ntenance –	ictions – En anual opera tions – Da oltage Varia - Connectin	ations and S pPC and P	adder s and 9 latior 9 urges LC -
Relay-Type Ins diagram – Elec Mechanically o Unit III Adva Programming Instructions – M Unit IV PLC PLC Enclosure – Program Ed Process Contro	of Logic – Processor Memory Orga tructions - Instruction addressing – ctromagnetic Control relays – Cor perated switches Inced PLC Programming Timers – Programming Counters Math Instructions – Sequencer and S Installation and Troubleshooting es – Electrical Noise – Leaky Input	Branch ntactors s – Pro hift Regi s and Ou ng – Pro control	and Int – Mot ogram ister In utputs - eventiv	Contr structi - Grou e Mai	relay instru rters – Ma ol Instruc ons. unding – V ntenance –	ictions – En anual opera tions – Da oltage Varia - Connectin	ations and S pPC and P	adden s and 9 lation 9 urges LC –
Relay-Type Ins diagram – Election Mechanically of Unit III Adva Programming Instructions – M Unit IV PLC Enclosure – Program Ed Process Contro Unit V PLC	of Logic – Processor Memory Orga tructions - Instruction addressing – ctromagnetic Control relays – Cor perated switches Inced PLC Programming Timers – Programming Counters Math Instructions – Sequencer and Si Installation and Troubleshooting es – Electrical Noise – Leaky Input iting – Programming and Monitori ol: Types of processes – structure of	Branch ntactors s – Pro hift Regi s and Ou ng – Pro control ons	and Int – Mot ogram ister In utputs - eventiv system	Contr structi - Grou e Mai – Con	relay instru rters – Ma ol Instruc ons. Inding – V ntenance – ntrollers – I	ictions – En anual opera tions – Da oltage Varia - Connectin Data Acquis	ations and S g PC and P sition Systen	adden s and 9 lation 9 urges LC – ns 9
Relay-Type Ins diagram – Elec Mechanically o Unit III Adva Programming Instructions – M Unit IV PLC PLC Enclosure Process Contro Unit V PLC Computer Fund	of Logic – Processor Memory Orga tructions - Instruction addressing – etromagnetic Control relays – Cor perated switches Inced PLC Programming Timers – Programming Counters Math Instructions – Sequencer and Si Installation and Troubleshooting es – Electrical Noise – Leaky Inputs iting – Programming and Monitori ol: Types of processes – structure of Communication and its Applicati	Branch ntactors s – Pro hift Regi s and Ou ng – Pro control ons anufactu	and Int – Mot ogram ister In utputs - eventiv system uring –	Contr structi - Grou e Mai – Con	relay instru rters – Ma ol Instruc ons. Inding – V ntenance – ntrollers – I Communic	ictions – En anual opera tions – Da oltage Varia - Connectin Data Acquis cations – Co	ations and S g PC and P sition Systen	adder s and 9 latior 9 urges LC - ns 9 neric
Relay-Type Ins diagram – Elect Mechanically of Unit III Adva Programming Instructions – M Unit IV PLC PLC Enclosure – Program Ed Process Contro Unit V PLC Computer Fund control – Robot	of Logic – Processor Memory Orga tructions - Instruction addressing – ctromagnetic Control relays – Cor perated switches Inced PLC Programming Timers – Programming Counters Math Instructions – Sequencer and Si Installation and Troubleshooting es – Electrical Noise – Leaky Inputs iting – Programming and Monitori ol: Types of processes – structure of Communication and its Applicati amentals – Computer-Integrated M	Branch ntactors s – Pro hift Regi s and Ou ng – Pro control ons anufactu ng system	and Int – Mot ogram ister In utputs - eventiv system uring – n – pne	Contr structi - Grou e Mai - Con Data cumati	relay instru rters – Ma ol Instruc ons. unding – V ntenance – ntrollers – 1 Communic c stamping	tions – En anual opera tions – Da oltage Varia - Connectin Data Acquis cations – Co system – n	ations and S ations and S og PC and P sition System omputer num naterial hand	adden s and 9 lation 9 urges LC – ns 9 neric Iling
Relay-Type Ins diagram – Elect Mechanically of Unit III Adva Programming Instructions – M Unit IV PLC PLC Enclosure – Program Ed Process Contro Unit V PLC Computer Fund control – Robot	of Logic – Processor Memory Orga tructions - Instruction addressing – etromagnetic Control relays – Cor perated switches inced PLC Programming Timers – Programming Counters fath Instructions – Sequencer and S Installation and Troubleshooting es – Electrical Noise – Leaky Inputs iting – Programming and Monitori ol: Types of processes – structure of Communication and its Applicati amentals – Computer-Integrated M ics - PLC Applications: Bottle fillin	Branch ntactors s – Pro hift Regi s and Ou ng – Pro control ons anufactu ng system	and Int – Mot ogram ister In utputs - eventiv system uring – n – pne	Contr structi - Grou e Mai - Con Data cumati	relay instru rters – Ma ol Instruc ons. unding – V ntenance – ntrollers – 1 Communic c stamping	tions – En anual opera tions – Da oltage Varia - Connectin Data Acquis cations – Co system – n	ations and S ations and S og PC and P sition System omputer num naterial hand	adde s and 9 latior 9 urges LC - ns 9 neric Iling
Relay-Type Ins diagram – Elect Mechanically of Unit III Adva Programming Instructions – M Unit IV PLC PLC Enclosure – Program Ed Process Contro Unit V PLC Computer Fund control – Robot system – PLC in	of Logic – Processor Memory Orga tructions - Instruction addressing – etromagnetic Control relays – Cor perated switches Inced PLC Programming Timers – Programming Counters fath Instructions – Sequencer and S Installation and Troubleshooting es – Electrical Noise – Leaky Inputs iting – Programming and Monitori ol: Types of processes – structure of Communication and its Applicati amentals – Computer-Integrated M ics - PLC Applications: Bottle filling in Individual process – Continuous p	Branch ntactors s – Pro hift Regi s and Ou ng – Pro control ons anufactu ng system	and Int – Mot ogram ister In utputs - eventiv system uring – n – pne	Contr structi - Grou e Mai - Con Data cumati	relay instru rters – Ma ol Instruc ons. unding – V ntenance – ntrollers – 1 Communic c stamping	tions – En anual opera tions – Da oltage Varia - Connectin Data Acquis cations – Co system – n	ations and S ations and S og PC and P sition System omputer num naterial hand	adder s and 9 latior 9 urges LC - ns 9 neric Iling
Relay-Type Ins diagram – Elec Mechanically o Unit III Adva Programming Instructions – M Unit IV PLC PLC Enclosure – Program Ed Process Contro Unit V PLC Computer Fund control – Robot system – PLC in REFERENCE(1. Frank D. P	of Logic – Processor Memory Orga tructions - Instruction addressing – ctromagnetic Control relays – Cor perated switches Inced PLC Programming Timers – Programming Counters Math Instructions – Sequencer and Si Installation and Troubleshooting es – Electrical Noise – Leaky Inputs iting – Programming and Monitori ol: Types of processes – structure of Communication and its Applicati amentals – Computer-Integrated M ics - PLC Applications: Bottle filling in Individual process – Continuous p	Branch ntactors s – Pro hift Regi s and Ou ng – Pre control ons anufactu ng system rocess –	and Int – Mot ogram ister In utputs - eventiv system uring – n – pne Conta	Contr structi - Grou e Mai - Con Data eumati iner fi	relay instru rters – Ma ol Instruc ons. Inding – V ntenance – ntrollers – I Communic c stamping Iling syster	ictions – En anual opera tions – Da oltage Varia - Connectin Data Acquis cations – Co system – n n – liquid he tion, New I	ations and S ations and S g PC and P sition System omputer num naterial hance eating system Delhi,2010	adden s and g lation urges LC - ns 9 neric lling n.
Relay-Type Ins diagram – Elect Mechanically o Unit III Adva Programming Instructions – M Unit IV PLC PLC Enclosure Program Ed Process Control Unit V PLC Computer Fund control – Robot system – PLC in REFERENCE(1. Frank D. P	of Logic – Processor Memory Orga tructions - Instruction addressing – ctromagnetic Control relays – Cor perated switches Inced PLC Programming Timers – Programming Counters fath Instructions – Sequencer and Si Installation and Troubleshooting es – Electrical Noise – Leaky Inputs iting – Programming and Monitori of: Types of processes – structure of Communication and its Applicati amentals – Computer-Integrated M ics - PLC Applications: Bottle filling in Individual process – Continuous p S): retruzella, Programmable Logic Com- n W and Reis Ronald A., Program	Branch ntactors s – Pro hift Regi s and Ou ng – Pre control ons anufactu ng system rocess –	and Int – Mot ogram ister In utputs - eventiv system uring – n – pne Conta	Contr structi - Grou e Mai - Con Data eumati iner fi	relay instru rters – Ma ol Instruc ons. Inding – V ntenance – ntrollers – I Communic c stamping Iling syster	ictions – En anual opera tions – Da oltage Varia - Connectin Data Acquis cations – Co system – n n – liquid he tion, New I	ations and S ations and S g PC and P sition System omputer num naterial hance eating system Delhi,2010	adder s and g latior g urges LC - ns g heric lling n.
Relay-Type Insdiagram – ElectMechanically oUnit IIIAdvaProgrammingInstructions – MUnit IVPLCPLC EnclosureProcess ControUnit VPLCComputer Fundcontrol – Robotsystem – PLC inREFERENCE(1.Frank D. P2.Webb JohDelhi, 201	of Logic – Processor Memory Orga tructions - Instruction addressing – ctromagnetic Control relays – Cor perated switches Inced PLC Programming Timers – Programming Counters fath Instructions – Sequencer and Si Installation and Troubleshooting es – Electrical Noise – Leaky Inputs iting – Programming and Monitori of: Types of processes – structure of Communication and its Applicati amentals – Computer-Integrated M ics - PLC Applications: Bottle filling in Individual process – Continuous p S): retruzella, Programmable Logic Com- n W and Reis Ronald A., Program	Branch ntactors s – Pro hift Regi s and Ou ng – Pro control ons anufactu ng system rocess – ntrollers" mmable	and Int – Mot ogram ister In utputs - eventiv system uring – n – pne Contai	Contr structi - Grou e Mai - Con Data eumati iner fi	relay instru rters – Ma ol Instruc ons. Inding – V ntenance – ntrollers – I Communic c stamping Iling syster	ictions – En anual opera tions – Da oltage Varia - Connectin Data Acquis cations – Co system – n n – liquid he tion, New I	ations and S ations and S g PC and P sition System omputer num naterial hance eating system Delhi,2010	adder s and g latior g urges LC - ns g heric lling n.

P.C Chairman - BoS Dept.of ECE - ESEC

ELECTIVE-II

Programm	e ME-	APPLIED I	ELECT	RONI	CS		R 2019	Semester	Π
0 0	C N		Hou	rs / W	eek	Credit	Total	Maximum	1
Course Co	e Course Nan	ne	LT		Р	С	Hours	Marks	
19AEX05	CAD FOR V	LSI	3	0	0	3	45	100	
Course Obj	ective (s): The purpose of	f learning th	is course	e is to					
•= Study	the concepts of VLSI De	sign Flow, I	Layout,	Placem	nent A	nd Partition	ning		
 Study Synth 	the concepts of Floor Pla esis	Inning And	Routing,	, Simul	ation	And Logic	Synthesis	& High Level	
Course Out	comes: At the end of this	course, lear	mers wil	l be ab	le to:			1. S. 1. S.	
• Gain	Knowledge of VLSI Des	ign Flow, La	ayout, P	laceme	ent An	d Partitioni	ing		
🖛 Gain	Knowledge.of Floor Plan	ning And R	outing, S	Simula	tion A	nd Logic S	Synthesis &	High Level	
Synth	esis								
Unit I I	NTRODUCTION TO V	LSI DESIG	SN FLO	W		8 I O 1	1.6	21-1-1	9
	to VLSI Design method				-				
Theory and	Computational Complex	city, Tractab	ole and	Intract	able p	problems, (General put	rpose methods	for
combinatori	al optimization.								
Unit II I	AYOUT, PLACEMEN	T AND PA	RTITIC	ONING	5				9
Layout Cor	npaction, Design rules,	Problem	formulat	tion, A	Algorit	hms for	constraint	graph compac	ction
And the second sec	nd partitioning, Circuit rep				-				
Unit III I	LOOR PLANNING AN	D ROUTI	NG	12			1		9
Floor planni	ng concepts, Shape funct	ions and flo	orplan s	sizing.	Types	of local re	outing prob	lems. Area rou	iting
the crossestory descent and tooling	ing, Global routing, Algo		and the second of the		- 7 F				
Unit IV S	IMULATION AND LO	GIC SYNT	THESIS				2002		9
Simulation,	Gate-level modeling and	simulation,	Switch-	level n	nodelin	ng and sim	ulation, Co	mbinational L	ogic
	nary Decision Diagrams,					Ŭ.			U
Unit V I	IIGH LEVEL SYNTHE	SIS					1	10 × 11	9
	adala for high laval an	mthasis int	1			11			1.
Hardware m	odels for mon level sv	nunesis. Ini	ernal re	presen	tation	allocation	n. assignme	ent and sched	ulin
	odels for high level sy gorithms, Assignment pro						n, assignme	ent and sched	uling

RE	FERENCE(S):
1.	N.A. Sherwani, Algorithms for VLSI Physical Design Automation, Kluwer Academic Publishers, 2008.
2.	S.H. Gerez, Algorithms for VLSI Design Automation, John Wiley & Sons, 2012.
3.	Sadiq M. Sait, Habib Youssef, VLSI Physical Design automation: Theory and Practice, World scientific 2016.
4.	Steven M.Rubin, Computer Aids for VLSI Design, Addison Wesley Publishing 2001.

Chairman - Bos Dept.of ECE - ESEC

Programme	ME-APPLIED F	LECTRONICS				R 2019	Semester	I	
<u> </u>	Course Norma	Hou	rs / W	eek	Credit	Total	Maximum	Maximum	
Course Code	Course Name	L	Т	Р	C	Hours	Marks		
19AEX06	ASIC AND FPGA DESIGN	3	0	0	3	45	100		

• Study the concents of Overview Of ASIC And PID ASIC Physical

- Study the concepts of Overview Of ASIC And PID, ASIC Physical Design
- Study the concepts of Logic Synthesis, Simulation And Testing, Field Programmable Gate Arrays & SOC Design

Course Outcomes: At the end of this course, learners will be able to:

- Gain Knowledge of Overview Of ASIC And PID, ASIC Physical Design
- Gain Knowledge of Logic Synthesis, Simulation And Testing, Field Programmable Gate Arrays & SOC Design

9

9

0

9

9

airman - Bos

Dept.of ECE - ES

Unit I OVERVIEW OF ASIC AND PLD

Types of ASICs - Design flow – CAD tools used in ASIC Design – Programming Technologies: Antifuse – static RAM – EPROM and EEPROM technology, Programmable Logic Devices: ROMs and EPROMs – PLA –PAL. Gate Arrays – CPLDs and FPGAs.

Unit II ASIC PHYSICAL DESIGN

System partition -partitioning - partitioning methods – interconnect delay models and measurement of delay floor planning - placement – Routing: global routing - detailed routing - special routing - circuit extraction -DRC.

Unit III LOGIC SYNTHESIS, SIMULATION AND TESTING

Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation. Verilog and logic synthesis -VHDL and logic synthesis - types of simulation -boundary scan test - fault simulation - automatic test pattern generation.

Unit IV FIELD PROGRAMMABLE GATE ARRAYS

FPGA Design : FPGA Physical Design Tools -Technology mapping - Placement & routing - Register transfer (RT)/Logic Synthesis - Controller/Data path synthesis - Logic minimization.

Unit V SOC DESIGN

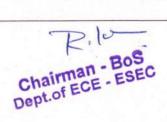
System-On-Chip Design - SoC Design Flow, Platform-based and IP based SoC Designs, Basic Concepts of Bus-Based Communication Architectures. High performance algorithms for ASICs/ SoCs as case studies: Canonical Signed Digit Arithmetic, Knowledge Crunching Machine, Distributed Arithmetic, High performance digital filters for sigma-delta ADC.

REFERENCE(S):

1.	David A.Hodges, Analysis and Design of Digital Integrated Circuits (3/e), MGH 2014
2.	H.Gerez, Algorithms for VLSI Design Automation, John Wiley, 2001
3.	Jan. M. Rabaey et al, Digital Integrated Circuit Design Perspective (2/e), PHI 2007
4.	M.J.S. Smith : Application Specific Integrated Circuits, Pearson, 2013
5.	J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley& Sons, Newyork.
6.	P.K.Chan& S. Mourad, Digital Design using Field Programmable Gate Array, Prentice Hall.
7.	Sudeep Pasricha and NikilDutt, On-Chip Communication Architectures System on Chip Interconnect, Elsevier, 2008

Programme	ME-APPLIED F	ELECT	RONI	CS		R 2019	Semester	Π
0 01	C N	Hou	urs / W	/eek	Credit	Total	Maximun	n
Course Code	Course Name	L	Т	Р	C	Hours	Marks	
19AEX07	SYSTEM ON CHIP DESIGN	3	0	0	3	45	100	
Course Obje	tive (s): The purpose of learning this	s course	e is to					
 Study t 	he concepts of Introduction to System	n On C	hip De	sign, S	ystem On C	Chip Design		
 Study t 	he concepts of Hardware Software C	o-Desig	gn, Syr	nthesis	& SOC Ve	rification an	nd Testing	
Course Outco	mes: At the end of this course, learn	ners wil	l be ab	le to:				
• Gain K	nowledge of System On Chip Desig	n, Syste	em On	Chip I	Design			
🔹 Gain K	nowledge of Hardware Software Co	-Design	n, Synt	hesis &	SOC Veri	fication and	l Testing	
Unit I IN	TRODUCTION					1		9
Introduction	to SoC Design, system level d	lesign,	metho	odologi	es and to	ools, syster	n hardware:	Ю
communicatio	n, processing units, memories; oper	ating s	ystems	: predi	ction of ex	ecution, rea	I time schedu	ling
embedded OS	, middle ware; Platform based SoC d	lesign,	multip	rocesso	r SoC and	Network on	Chip, Low p	owe
SoC Design								
Unit II S	STEM LEVEL MODELLING							9
SystemC: ov	erview, Data types, modules, not	ion of	time,	dynai	nic proces	s, basic cl	hannels, stru	cture
communicatio	n, ports and interfaces, Design with	exampl	es.					
Unit III H	ARDWARE SOFTWARE CO-DES	SIGN						9
Analysis, par	itioning, high level optimizations, r	eal-tim	e sche	duling.	hardware	acceleration	, voltage sca	ling
	anagement; Virtual platform mode							
systems.	anagement, i unan printerni inter					1 .		
and the second se	NTHESIS							9
System synthe	esis: Transaction Level Modeling (T	LM) ba	ased de	esign, a	utomatic T	LM genera	tion and map	oing
	thesis; software synthesis: code			-				
	n; Hardware synthesis: RTL archite							
	pelining and scheduling.							
Unit V SC	C VERIFICATION AND TESTIN	NG	_					9
SoC and IP i	ntegration, Verification: Verification	n techn	ology	option	s, verificati	ion method	ology, overvi	ew:
system level	verification, physical verification,	hardwa	are/soft	ware of	co-verificat	ion; Test r	equirements	
the second se	s, SoC design for testability - System							
	. Soc design for testability - System	model	ing, tes	st powe	r dissipatio	n, test acces	ss mechanism	and
	s, soc design for testability - system	moder	ing, tes	st powe	r dissipatio	n, test acces	ss mechanism	and
		moder	ing, tes	st powe	r dissipatio	n, test acces	ss mechanism	and
REFERENCI		moder	ing, tes	st powe	r dissipatio	n, test acces	ss mechanism	and
REFERENCI						n, test acces	ss mechanism	and
REFERENCI	C(S): J. Donovan, SystemC: From the Gro	ound U	p, Spri	nger, 2	014.			and
REFERENCI 1. D. Black 2 D. Gajsi	E(S): J. Donovan, SystemC: From the Gro ci, S. Abdi, A. Gerstlauer, G. So	ound U	p, Spri	nger, 2	014.			and
REFERENCI 1. D. Black 2. D. Gajs Verificat	E(S): J. Donovan, SystemC: From the Groci, S. Abdi, A. Gerstlauer, G. Scion, Springer, 2009.	ound U chirner,	p, Spri , Emb	nger, 2 edded	014. System D	esign: Moo	deling, Synth	and
REFERENCI 1. D. Black 2. D. Gajs Verificat 3. Erik Lars	E(S): J. Donovan, SystemC: From the Gro ki, S. Abdi, A. Gerstlauer, G. So on, Springer, 2009. on, Introduction to advanced system	ound U chirner, -on-chi	p, Spri , Emb p test c	nger, 2 edded design a	014. System D and optimis	esign: Moo	deling, Synth nger 2009.	and
REFERENCI 1. D. Black 2. D. Gajsl Verificat 3. Erik Lars 4. Grotker, Ghenassi	C(S): J. Donovan, SystemC: From the Gro ki, S. Abdi, A. Gerstlauer, G. So on, Springer, 2009. on, Introduction to advanced system T., Liao, S., Martin, G. & Swan, S. S	ound U chirner, -on-chi	p, Spri , Emb p test o design	nger, 2 edded design a with S	014. System D and optimis ystem C, Sp	esign: Moo ation, Sprin pringer, 201	deling, Synth nger 2009. 1.	esis
REFERENCI 1. D. Black 2. D. Gajsl Verificat 3. Erik Lars 4. Grotker, 5. Ghenassi	E(S): J. Donovan, SystemC: From the Gro ki, S. Abdi, A. Gerstlauer, G. So on, Springer, 2009. on, Introduction to advanced system	ound U chirner, -on-chi	p, Spri , Emb p test o design	nger, 2 edded design a with S	014. System D and optimis ystem C, Sp	esign: Moo ation, Sprin pringer, 201	deling, Synth nger 2009. 1.	and esis

Hoi-junyoo, Kangmin Lee, Jun Kyoungkim, Low power NoC for high performance SoCdesing, CRC press
 M. L. Bushnell and V.D. Agrawal, Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits, Springer, 2009.



Programme	ME-APPLIED I	ELECTI	RONI	CS		R 2019	Semester I
Course Code	Course Name	Ho	urs / W	/eek	Credit	Total	Maximum
Course Coue	Course Name	L	Т	Р	С	Hours	Marks
19AEX08	GENETIC ALGORITHMS	3	0	0	3	45	100
Study the Study th	tive (s): The purpose of learning this ne concepts of Introduction to Genet ne concepts of Applications Of GA,	ic Algor Introdu	ithm, (· · · · · · · · · · · · · · · · · · ·		d Machine I	Learning &
	tions Of Genetics-Based Machine L mes: At the end of this course, learn						
 Gain K Gain K Applica 	nowledge of Introduction to Genetic nowledge of Applications Of GA, I tions Of Genetics-Based Machine L	c Algorit ntroduct earning	thm, G tion Tc	Л Оре		Machine Lo	
	TRODUCTION TO GENETIC Al to Genetic Algorithm – Robustness						9
The 2-armed &	ingo - Mathematical foundations: 2 k-armed Bandit problem. –The bui						
Unit II GA	OPERATORS						
scaling. Codi	n program. – How well does it work ng – A Multi parameter, Mapped, Fi PLICATIONS OF GA		10.00				
applications abeyance – I objective opti	GA – GA application of Historical of GA - Advanced operators & nversion & other reordering operat mization – Knowledge-Based Techr TRODUCTION TO GENETICS-I	technic ors. – o niques. –	ques i ther m GA &	n gene ine-op parall	etic search erators – 1 el processe	h :Domina Niche & Sp es – Real lif	nce, Diploidy & peciation – Multi
	sed Machine learning – Classifier s						onment of credit:
	rigade - Genetic Algorithm - A sin						
Unit V AP	PLICATIONS OF GENETICS-B.	ASED N	ЛАСН	INE L	EARNIN	G	9
	GBMC – Development of CS-1, th efforts. –Current Applications.	e first c	lassifi	er syste	em. – Smi	tch's Poke	r player. – Other
		-					
REFERENCE							
1. David E Educatio	. Gold Berg, Genetic Algorithms n, 2011	in Sea	arch, (Optimi	zation &	Machine I	Learning, Pearso

S.Rajasekaran, G.A.Vijayalakshmi Pai, Neural Networks, Fuzzy Logic and Genetic Algorithms, PHI, 2003 (Chapters 8 and 9)

3. Kalyanmoy Deb, Optimization for Engineering Design, algorithms and examples, PHI 2005

2.

P.10-Chairman - BoS Dept.of ECE - ESEC

ELECTIVE-III

Programme	ME-APPLIED	ELEC	CTRON	ICS		R 2019	Semester	II
Course Code	Course Name	Ho	ours / W	eek	Credit	Total	Maximur	n
Course Code	Course Name	L	Т	Р	С	Hours	Marks	
19AEX09	PATTERN RECOGNITION	3	0	0	3	45	100	
Study th	tive (s): The purpose of learning the concepts of Pattern Classifier, Une concepts of Structural Pattern R es	Insuper	rvised C	lassific		nd Selectio	n & Recent	
	mes: At the end of this course, lea	rners v	vill be a	ble to:	1			
🕶 Gain Kr	nowledge of Pattern Classifier, Un	nsuperv	ised Cl	assifica	tion			
🔹 Gain Kr	owledge of Structural Pattern Red	cogniti	on, Fea	ture Ex	traction An	d Selection	& Recent Ad	vanc
the second se	TTERN CLASSIFIER pattern recognition -Discrimin			0	21.2			9
Problems wit classifier.	telihood estimation –Bayesian pa th Bayes approach –Pattern cla					A STATE OF STATE OF STATE	and the second	
Unit II UN	SUPERVISED CLASSIFICATI	ION						9
Clustering for	unsupervised learning and classi	ficatio	n - Clu	stering	concept-C-	means algo	orithm-Hierarc	hical
clustering pro	cedures- Graph theoretic approach	to pat	tern clu	stering	- Validity of	of clustering	g solutions.	
Unit III ST	RUCTURAL PATTERN RECO	GNIT	ION		1.1			9
	rmal grammars-String generation stic grammars and applications - C						ntactic descrip	tion-
	ATURE EXTRACTION AND S	-		. cro c c i c i	representa			9
Entropy minin	nization - Karhunen - Loeve trans	sforma	tion-fea	ture sel	ection thro	ugh functio	ons approxima	tion-
Binary feature	selection.						2000	
Unit V RE	CENT ADVANCES	11.51		-		1		9
learning in no	k structures for Pattern Recogniti eural Pattern Recognition-Self sing Genetic Algorithms.							
REFERENCE	(S):		-					
1. R.O Duda	P.E Hart and Stork, Pattern Class	sificatio	on, Wile	ey, 2012	2.	TO		
2. Robert J. Sons Inc.,	Sehalkoff, Pattern Recognition: S 2010.	Statisti	cal, Str	uctural	and Neura	al Approach	nes, John Wil	ey &
	nzales, Pattern Recognition Princi		Contraction of the second	Containe in Subset	Carlo Car	and the second		
	adier and P. Eric Smith, Pattern Re	-		5 S	g, John Wi	ley & Sons	, 2006.	
5. IEEE Tran	saction on Pattern Recognition Te	echniqu	ie, 2016				and the second	61.1
C I IIIIII II I		Contraction Contraction	0001					

6. IEEE Engineering Medicine and Biology Magazine, 2006.

R.10-Chairman - BoS Dept.of ECE - ESEC

Programme	ME-APPLIED	ELECT	RONI	CS		R 2019	Semester	Π
Course Code	Course Name	Ho	urs / W	eek	Credit	Total	Maximu	m
Course Coue	Course Maine	L	Т	P	С	Hours	Marks	Ĩ
19AEX10	ADVANCED DIGITAL IMAGE PROCESSING	3	0	0	3	45	100	
	ve (s): The purpose of learning the						110 - 10	
	concepts of Fundamentals Of D		-		50	-	-	
	concepts of Morphological Imag			-	ntation, Re	presentatio	on And Descri	ption
	Recognition And Image Process nes: At the end of this course, lea							
	wledge of Fundamentals Of Dig				Color Im	age Proces	sing	
	owledge of Morphological Image		17 C	075		- 1075-1		tion &
	ecognition And Image Processing		51.0	Billerin	atton, reep	()	, , ind D to trip	non ee
Unit I FUN	DAMENTALS OF DIGITAL I	MAGE	PROC	ESSIN	G	10 M		9
	sual Perception- Image acquisit		and the second second second					
	othing and sharpening - Discret	te 2D tr	ansform	ns - D	FT, DCT,	Walsh-Ha	adamard, Slai	nt, KL
Wavelet Transfe	orm – Haar wavelet.							
Unit II COL	OR IMAGE PROCESSSING							9
Color Image Fu	indamentals-Color Models- RGI	B, CMY	, CMY	K and	HSI Cold	or Models-	Pseudocolor	Image
and the second	tensity Slicing- Intensity to Col-							- Colo
Transformation	 Color Image Smoothing and Sh 	narpenin	g- Colo	r Segn	nentation -	Noise in C	Color Images.	_
Unit III MOR	PHOLOGICAL IMAGE PRO	CESSI	NG					9
	Basic Concepts from Set Theor				The second s		Sales and the second	
and the second second	ng and Closing - Hit-or-Miss T					The second second	Ele man manager a	12
	gion Filling- Extraction of Co	onnected	Com	oonents	s- Convex	Hull- T	hinning-Thick	cening
	ing Gray-Scale Morphology.	TION		COD	DTION	1-1-1-1		
	MENTATION, REPRESENTA							9
and the second sec	- Edge Linking and Boundary	a contraction			Contraction of the second	a construction of the second		logica
	nentation Algorithm - Use of Mar		-				ptors.	9
	CT RECOGNITION AND IM	8						
	attern Classes -Recognition Basifiers- Neural Networks, Fuzzy						and the second	
	ermarking - Steganography.	System	5 - UA	. mag	e compres	SION- JI LA	J, JI LO2000	JDIO
Standards If a	steganography.							
					and an and			
REFERENCE(S	5):	1.11				<u> 1</u>	Secondaria	
1. Rafael C. G	ionzalez, Digital Image Processir	ng, Pears	son Edu	cation	Inc., 3rd I	Edition, 20	008.	
2	onka, Vaclav Hlavac, Roger I		-	Proces	sing, Ana	alysis and	Machine V	ision,
Brooks/Clo	e, Vikas Publishing House 2nd E			. í.,	1		. 311. 1	
TANK AND	ood, Data Compression, Morgan				.a			
	Gonzalez, Richards E.Woods, S	-	F1 1 1*	T	1 1	Contraction of the second		

Rafael C. Gonzalez, Richards E.Woods, Steven Eddins, Digital Image Processing using MATLAB,Pearson Education, Inc., 2014.

Chairman - BoS Dept.of ECE - ESEC

Programme	ME-APPLIED	ELECT	RONI	CS	11.1	R 2019	Semester	II
Course Code	Course Norre	Hours	/Wee	k	Credit	Total	Maximur	n
Course Code	Course Name	L	Т	P	С	Hours	Marks	
19AEX11	SOFT COMPUTING AND OPTIMIZATION TECHNIQUES	3	0	0	3	45	100	
 Study the Study the Optimiza Course Outcom Gain Know Gain Know Optimiza Unit I NEU Machine Learni 	ve (s): The purpose of learning the concepts of Neural Networks, F e concepts of Neuro-Fuzzy Mod tion Techniques nes: At the end of this course, lea owledge of Neural Networks, Fu owledge of Neuro-Fuzzy Mode tion Techniques JRAL NETWORKS ng using Neural Network, Learn	uzzy Log leling, C rners wil zzy Logi ling, Co ning algo	gic onvent l be ab c nventic rithms,	le to: onal C	Optimizatio	n Techniqu urning Neur	ues & Evolutio ral Networks -	onary 9 - Feed
	rks, Radial Basis Function, Uns ance Architectures, Hopfield net		d Learı	ning N	leural Net	works – Se	lf Organizing	map
Unit II FUZ	ZY LOGIC						~	9
250 AVA 201	perations on Fuzzy Sets – Fuzz zzy Inference Systems – Fuzzy E						zy Rules and	Fuzzy
Unit III NEU	RO-FUZZY MODELING							9
and the second of the second s	Fuzzy Inference Systems – Coa tering Algorithms – Rule base St				•			
Unit IV CON	VENTIONAL OPTIMIZATIO	ON TEC	HNIQ	UES		<u> </u>	1. S. S. S.	9
optimization-gra Method, Marqu function method	optimization techniques, Statem dient search method-Gradient of ardt Method, Constrained opti , external penalty function metho JUTIONARY OPTIMIZATIO	of a func imizatior od.	ction, s n —seq	steepes uentia	st gradient	-conjugate	gradient, New	vton's
	hm - working principle, Basic				minologies	s Building	block hypot	
	sman Problem, Particle swam op	1			and the second	NAME OF TAXABLE PARTY AND ADDRESS OF TAXABLE PARTY.	, otoek nypet	
REFERENCE(S	b): oldberg, Genetic Algorithms in 1	<u></u>						1

2. George J. Klir and Bo Yuan, Fuzzy Sets and Fuzzy Logic-Theory and Applications, Prentice Hall, 2010.

3. James A. Freeman and David M. Skapura, Neural Networks Algorithms, Applications, and Programming Techniques, Pearson Edn., 2008.

4. Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, Neuro-Fuzzy and Soft Computing, Prentice-Hall of India, 2006.

5. Mitchell Melanie, An Introduction to Genetic Algorithm, Prentice Hall, 2001.

Chairman - BoS Dept.of ECE - ESEC

Programme	ME-APPLIED ELI	ECTR	ONIC	CS	1.5	R 2019	Semester	Π
	C N	Hour	s/W	eek	Credit	Total	Maximun	n
Course Code	Course Name	L	Т	P	С	Hours	Marks	
19AEX12	SYNTHESIS AND OPTIMIZATION OF DIGITAL CIRCUITS	3	0	0	3	45	100	
 Study Optimiz Study t Optimiz 	tive (s): The purpose of learning this c the concepts of Circuits And Har vation the concepts of Scheduling Algorithm tation & Sequential Logic Optimization mes: At the end of this course, learners	rdware ms An n	Moo d Re	source		X		
Gain KiGain K	nowledge of Circuits And Hardware M nowledge of Scheduling Algorithm ration & Sequential Logic Optimization	lodelin ns And	ng, Ar	chitec		1. A.	and the second sec	
Unit I	CIRCUITS AND HARDWARE MO	DELI	NG					9
a second s	croelectronic Circuits - Computer Aide bra and Application-Hardware Modeli				· · · · · · · · · · · · · · · · · · ·			
Unit II A	ARCHITECTURAL LEVEL SYNTI	HESIS	AND	OPT	IMIZAT	ION		9
	Architectural synthesis Problems- A pipelined circuits.	rea ar	nd per	rforma	ance Estir	nation-Cor	ntrol unit synt	hesis
Unit III S	SCHEDULING ALGORITHMS AN	D RES	SOUR	CE S	HARING		Sec. Con	9
Constraints-	d Scheduling-ASAP Algorithm-ALA Scheduling pipelined circuits-Sharin inding –Module selection problems-Str	ng and	l bin	ding	for Domi			
Unit IV I	OGIC-LEVEL SYNTHESIS AND	OPTIN	AIZA	TION	1			9
	zation Principles-Algorithms and Lo of logic networks-Algebraic and Boole	-						
optimization optimization		FION				1910		1
optimization	EQUENTIAL LOGIC OPTIMIZAT	TION					261	9

1.	Giovanni De Micheli, Synthesis and optimization of Digital Circuits, Tata McGraw-Hill, 2007
2.	John Paul Shen, Mikko H. Lipasti, Modern processor Design, Tata McGraw Hill, 2003
3.	Gary D. Hachtel and Fabio Somenzi, Logic Synthesis and Verification Algorithms, Springer
4	Frank Vahid Digital Design John Wiley & Sons

Chairman - BoR Dept.of ECE - F

ELECTIVE-IV

Programme	ME-APPLIED I	ELECTR	ONIC	S		R 2019	Semester III
Course Code	Course Name	Hou	urs / W	eek	Credi t	Total	Maximum
		L	Т	P	C	Hours	Marks
	ELECTROMAGNETIC						
19AEX13	INTERFERENCE AND COMPATIBILITY	3	0	0	3	45	100
Course Object	ive (s): The purpose of learning th	nis course	is to				
 Study the 	e concepts of EMI Environment, I	EMI Coup	oling P	rincipl	es		
 Study the 	e concepts of EMI/EMC Standard	s And Me	easurer	nents,	EMI Cont	trol Techniq	ues &
EMC De	sign Of PCBs						
Jourse Outcom	nes: At the end of this course, lear	rners will	be abl	e to:			
• Gain Kn	owledge of EMI Environment, El	MI Coupl	ing Pri	nciple	S		
Gain Kn	owledge of EMI/EMC Standards	And Mea	surem	ents, E	MI Contro	ol Techniqu	es & EMC Design
Of PCBs							
Unit I E	MI ENVIRONMENT						9
EMI/EMC con	ncepts and definitions, Sources of	of EMI, o	conduc	ted an	d radiated	d EMI, Tra	nsient EMI, Time
domain Vs Fr	equency domain EMI, Units of	measuren	nent p	aramet	ers, Emis	sion and in	nmunity concepts,
ESD.							
Unit II I	EMI COUPLING PRINCIPLES	5					9
Conducted, Ra	adiated and Transient Coupling,	Common	n Impe	dance	Ground (Coupling, F	Radiated Common
Mode and Gr	ound Loop Coupling, Radiated	Differen	itial M	lode (Coupling,	Near Field	I Cable to Cable
Coupling, Pow	er Mains and Power Supply coupl	ling.					
Unit III I	EMI/EMC STANDARDS AND I	MEASUI	REME	NTS		1.1.1.1.1.1.1	9
	rds - FCC, CISPR,I EC, EN, Mil						
/Systems, EMI	Shielded Chamber, Open Area T	'est Site, '	TEM C	Cell, Se	ensors/Inje	ectors/Coup	lers, Test beds for
	Military Test Method and Proced	ures (462).				
	CMI CONTROL TECHNIQUES					a Sama	9
	ering, Grounding, Bonding, Isol		ansform	ner, T	ransient	Suppressors	s, Cable Routing,
	Component Selection and Mount	ting.					
	MC DESIGN OF PCBS					S. Land	9
	ross Talk, Impedance Control, Po	ower Dist	ributio	n Dece	oupling, Z	Coning, Mot	herboard Designs
and Propagatio	n Delay Performance Models.	857					
EFERENCE(-				
	W., Noise Reduction Technique			-			
	, Introduction to Electromagnetic						
3. Kodali, V	.P., Engineering EMC Principles,	Measure	ments	and Te	chnologie	es, IEEE Pre	ess, London, 2006.
4. Keiser, B 2000	ernhard., Principles of Electroma	agnetic C	ompat	ibility,	Third Ed	dition, Arte	ch House, Dedhar

R.V. Chairman - BoS Dept.of ECE - ESEC

Course Code	ME-APPLIED I	ELECTI	RONIC	S		R 2019	Semester	III
Course Code	Course Name	Hou	irs / We	eek	Credit	Total	Maximu	m
	course reality	L	Т	P	С	Hours	Marks	
19AEX14	NANO ELECTRONICS	3	0	0	3	45	100	
Study th	tive (s): The purpose of learning this e concepts of Introduction to Nano ne concepts of Properties of Nano tions	electron	ics, Fab					And
Gain Kn Gain Kr Applicat Jnit I IN Microelectronic mechanics- Scl	mes: At the end of this course, learn owledge of Introduction to Nanoe nowledge of Properties of Nano ions NTRODUCTION TO NANOELE cs towards bio molecule electro- nrodinger wave equation- Wave m tronics- Semiconductors- Crysta	lectronic electron CCTROM onics-Pa echanics	rticles of part	cation no Str and ticles:	ructure De waves- W - Atoms a	vices & Lo vave-particlo nd atomic o	ogic Devices e duality- V orbitals- Mate	9 Vave trials
Semiconductor netero structure	hetero structures- Lattice-matche es- Carbon nano materials: nano tub	ed and p bes and f	seudo i fullerene	norph es.	ic hetero s			
characterization crystals- Meth	ny, etching, and other means for fain of nanostructures- Spontaneous for ods of nano tube growth- Che nano-electromechanical systems.	formatio	n and o	rderin	g of nanos	structures- (Clusters and i	nano
Unit III P	ROPERTIES							9
Magneto transp Neurons – The	roelectrics-Electronic Properties a port in Layered Structures-Organic e Molecular Basis of their Electr Fluorescence Methods-Scanning F	Molecul rical Ex	es – Ele citabilit	ectroni y-Circ	ic Structure	es, Propertie	es, and Reacti	ons-
	ANO STRUCTURE DEVICES							
								9
Electron transp Statistics of th Electron transp wells- Electron diodes- Field-e	ort in semiconductors and nanostr e electrons in solids and nanostr ort in nanostructures-Electrons in t is in quantum wires- Electrons in ffect transistors- Single-electron-t rs- Nano-electromechanical system	ructures- tradition quantur transfer	- Densi al low-o m dots- devices	ty of dimen Nano - Pote	states of sional strue ostructure ential-effec	electrons in ctures- Elec devices- Ro t transistor	n nanostructu etrons in quan esonant-tunne	lids- ares- atum eling
Electron transp Statistics of th Electron transp wells- Electron diodes- Field-e diodes and lase	ort in semiconductors and nanosti e electrons in solids and nanosti ort in nanostructures-Electrons in t s in quantum wires- Electrons in ffect transistors- Single-electron-t	ructures- tradition quantur transfer devices	- Densi al low-o m dots- devices - Quant	ty of dimen Nano - Pote	states of sional strue ostructure ential-effec	electrons in ctures- Elec devices- Ro t transistor	n nanostructu etrons in quan esonant-tunne	lids- ires- itum eling

1. Vladimir V. Mitin, Viatcheslav A. Kochelap, Michael A. Stroscio, Introduction to Nanoelectronics: Science, Nanotechnology, Engineering, and Applications, Cambridge University Press 2011

Chairman - Bra Dept.of ECE - E

2.	Supriyo Datta, Lessons from Nanoelectronics: A New Perspective on Transport, World Scientific 2012
3.	George W. Hanson, Fundamentals of Nanoelectronics, Pearson 2009
4.	Korkin, Anatoli; Rosei, Federico (Eds.), Nanoelectronics and Photonics, Springer 2008
5.	Mircea Dragoman, Daniela Dragoman, Nanoelectronics: principles and devices, CRC Press 2006
6.	Karl Goser, Peter Glosekotter, Jan Dienstuhl, Nanoelectronics and Nanosystems: From Transistors to Molecular and Quantum Devices, Springer 2004
7.	W. R. Fahrner, Nanotechnology and Nan electronics: Materials, Devices, Measurement Techniques (SpringerVerlag Berlin Heidelberg 2005)

R.L-

Chairman - Bog Dept.of ECE - ESFO

Charter 1 - 100

Programme	ME-APPLIED	ELECT	RONIC	CS	N.	R 2019	Semester	II
1	Commo Norma	Hour	rs / We	eek	Credit	Total	Maximu	m
Course Code	Course Name	L	T	Р	C	Hours	Marks	
19AEX15	MEMS AND NEMS	3	0	0	3	45	100	
Course Objective	e (s): The purpose of learning t	this course	e is to					
• Study the c	oncepts of Overview Of MEM	IS And NI	EMS, N	MEMS	Fabricatio	n Technolog	gies	
• Study the c	oncepts of Micro Sensors, Mic	cro Actuat	ors &	Nano s	systems An	d Quantum	Mechanics	
Course Outcome	s: At the end of this course, lea	arners will	be abl	le to:	2.		1.1.1	
Gain Know	ledge of Overview Of MEMS	S And NE	MS, M	EMS I	Fabrication	Technologi	es	
Gain Know	ledge of Micro Sensors, Micr	o Actuato	rs & N	ano sy	stems And	Quantum M	1echanics	
Unit I OVER	VIEW							9
New trends in Eng	ineering and Science: Micro a	and Nanos	scale s	ystems	, Introduct	ion to Desi	gn of MEMS	and
NEMS, MEMS ar	d NEMS - Applications, De	evices an	d struc	ctures.	Materials	for MEMS	: Silicon, sil	icon
compounds, polyme	ers, metals.							
Unit II MEM	S FABRICATION TECHNO	DLOGIES	S					9
see the set of the second s	cation processes: Photolithog		<u></u>	plantat	tion Diffi	ision Oxid	ation Thin	film
	RO SENSORS							
		and the second second second second		N //1		0		9
	esign of Acoustic wave sensor							iezo
bressure sensor.	sensors-engineering mechan							iezo
Unit IV MICR	sensors-engineering mechan							iezo stive
Dealow of Astronton	sensors-engineering mechan	ics behin	d thes	e Mic	rosensors.	Case stud	y: Piezo-resis	iezo stive 9
-	sensors-engineering mechanics COACTUATORS s: Actuation using thermal for	ics behin	d thes	e Mic using	shape men	Case study	y: Piezo-resis	iezo stive 9 sing
piezoelectric crysta	sensors-engineering mechan COACTUATORS s: Actuation using thermal fo ls, Actuation using Electrosta	ics behin prces, Actu tic forces	d thes uation (Paral	e Mic using lel pla	shape men	Case study	y: Piezo-resis	iezo stive 9 sing
piezoelectric crysta Micromechanical M	sensors-engineering mechan COACTUATORS s: Actuation using thermal fo ls, Actuation using Electrostat lotors and pumps. Case study:	ics behin orces, Actu tic forces Comb dri	d thes uation (Paral ve actu	e Mic using lel pla iators.	shape men	Case study	y: Piezo-resis	iezo stive 9 sing ors),
biezoelectric crysta Micromechanical M Unit V NANC	sensors-engineering mechan COACTUATORS s: Actuation using thermal fo ls, Actuation using Electrosta lotors and pumps. Case study: DSYSTEMS AND QUANTUR	ics behin orces, Actu tic forces Comb dri M MECH	d thes uation (Paral ve actu IANIC	e Mic using lel plan ators.	shape men te, Torsion	Case study	y: Piezo-resis , Actuation u drive actuato	iezo stive 9 sing ors), 9
biezoelectric crysta Micromechanical M Unit V NANC Atomic Structures a	sensors-engineering mechanics COACTUATORS s: Actuation using thermal for ls, Actuation using Electrostation lotors and pumps. Case study: DSYSTEMS AND QUANTUR and Quantum Mechanics, Mole	ics behin orces, Actu tic forces Comb dri M MECH ecular and	d thes uation (Paral ve actu IANIC Nanos	using lel plan ators. Structure	shape men te, Torsion re Dynamic	Case stud	y: Piezo-resis , Actuation u drive actuato ger Equation	iezo stive 9 sing ors), 9 and
biezoelectric crysta Micromechanical M Unit V NANC Atomic Structures a Wave function The	sensors-engineering mechan COACTUATORS s: Actuation using thermal for ls, Actuation using Electrostar lotors and pumps. Case study: DSYSTEMS AND QUANTUR and Quantum Mechanics, Mole ory, Density Functional Theorem	ics behin orces, Actu tic forces Comb dri M MECH ecular and ry, Nanos	d thes uation (Paral ve actu IANIC Nanos tructur	using lel plan ators. S structures and	shape men te, Torsion re Dynamic	Case stud	y: Piezo-resis , Actuation u drive actuato ger Equation	iezo stive 9 sing ors), 9 and
biezoelectric crysta Micromechanical M Unit V NANC Atomic Structures a Wave function The	sensors-engineering mechanics COACTUATORS s: Actuation using thermal for ls, Actuation using Electrostation lotors and pumps. Case study: DSYSTEMS AND QUANTUR and Quantum Mechanics, Mole	ics behin orces, Actu tic forces Comb dri M MECH ecular and ry, Nanos	d thes uation (Paral ve actu IANIC Nanos tructur	using lel plan ators. S structures and	shape men te, Torsion re Dynamic	Case stud	y: Piezo-resis , Actuation u drive actuato ger Equation	iezo stive 9 sing ors), 9 and
Diezoelectric crysta Micromechanical M Unit V NANC Atomic Structures a Wave function The Fields and their qua	sensors-engineering mechanics COACTUATORS s: Actuation using thermal for ls, Actuation using Electrostar lotors and pumps. Case study: DSYSTEMS AND QUANTUR and Quantum Mechanics, Mole ory, Density Functional Theorem ntization, Molecular Wires and	ics behin orces, Actu tic forces Comb dri M MECH ecular and ry, Nanos	d thes uation (Paral ve actu IANIC Nanos tructur	using lel plan ators. S structures and	shape men te, Torsion re Dynamic	Case stud	y: Piezo-resis , Actuation u drive actuato ger Equation	iezo stive 9 sing ors), 9 and
Diezoelectric crysta Micromechanical M Unit V NANC Atomic Structures a Wave function The Pields and their qua REFERENCE(S)	sensors-engineering mechanics COACTUATORS s: Actuation using thermal for ls, Actuation using Electrostar lotors and pumps. Case study: DSYSTEMS AND QUANTUR and Quantum Mechanics, Mole ory, Density Functional Theorem ntization, Molecular Wires and	ics behin orces, Actu tic forces Comb dri M MECH ecular and ry, Nanos d Molecul	d thes uation (Paral ve actu IANIC Nanos tructur ar Circ	e Mic using lel plan ators. S structur es and uits.	shape mem te, Torsion re Dynamic Molecular	Case stud	y: Piezo-resis , Actuation u drive actuato ger Equation	iezo stive 9 sing ors), 9 and
Diezoelectric crysta Micromechanical M Unit V NANC Atomic Structures a Vave function The Fields and their qua REFERENCE(S) 1. Chang Liu,	sensors-engineering mechanics COACTUATORS s: Actuation using thermal for ls, Actuation using Electrostar lotors and pumps. Case study: DSYSTEMS AND QUANTUR and Quantum Mechanics, Mole ory, Density Functional Theor ntization, Molecular Wires and	ics behin orces, Actu tic forces Comb dri M MECH ecular and ry, Nanos d Molecul	d thes Jation (Paral ve actu IANIC Nanos tructur ar Circ on Indi	e Mic using lel plan ators. S structur es and uits.	shape men te, Torsion re Dynamic Molecular ted, 2006.	Case stud	y: Piezo-resis , Actuation u drive actuato ger Equation	iezo stive 9 sing ors), 9 and
Diezoelectric crysta Micromechanical M Unit V NANC Atomic Structures a Wave function The Pields and their qua REFERENCE(S) 1. Chang Liu, 2. Marc Mado	sensors-engineering mechanics COACTUATORS s: Actuation using thermal for ls, Actuation using Electrostat lotors and pumps. Case study: DSYSTEMS AND QUANTUL and Quantum Mechanics, Mole ory, Density Functional Theorem ntization, Molecular Wires and Foundations of MEMS, Pearson	ics behin orces, Actu tic forces Comb dri M MECH ecular and ry, Nanos d Molecul on educati ication, Cl	d thes uation (Paral ve actu IANIC Nanos tructur ar Circ on Indi RC pre	e Mic using lel pla lators. S structur es and uits. ia limit ss 200	shape mem te, Torsion re Dynamic Molecular ted, 2006. 4.	Case study hory Alloys bar, Comb	y: Piezo-resis , Actuation u drive actuato ger Equation	iezo stive 9 sing ors), 9 and

4. Sergey Edward Lyshevski, MEMS and NEMS: Systems, Devices, and Structures CRC Press, 2002.

5. Tai Ran Hsu, MEMS and Microsystems Design and Manufacture, Tata McGraw Hill, 2002.

R. Longer - Bos Dept.of ECE - ESTO

Programme	ME-APPLIED ELI	ECTRO	NICS			R 2019	Semester	II
Course Code	Course Name		ours / Week		Credi t	Total	Maxim	
		L	Т	Р	С	Hours	Mark	(S
19AEX16	SYSTEM IDENTIFICATION AND ADAPTIVE CONTROL	3	0	0	3	45	100	
 Study the Study the Course Outcor 	ive (s): The purpose of learning this c e concepts of System Identification, R e concepts of State Estimation, Adapti nes: At the end of this course, learners owledge of System Identification, Re	ecursiv ive Con s will be	e meth trol Sc e able t	heme to:	s & Appli	cations of A	Adaptive Cor	ntrol
	owledge of State Estimation, Adaptiv							rol
	tem Identification	e contr	or ben	emes	a rippire		auptive com	9
Frequency and error method -	tems, The system identification pulysis, Correlation analysis and Spectro Maximum Likelihood – Instrumental	ral anal <u>y</u> Variabl	ysis. P e meth	arame nods				lictio
	ecursive methods and Closed Loop							
closed loop: identification. Unit III St	thods: Recursive least squares methods: Recursive least squares method- rariable method- Input signal design Identifiability considerations – Dir tate Estimation	for ide rect and	entifica d indi	ation. rect	Identifica dentificat	tion of sys ion – Joir	stems operation nt input / o	ing i outpu
closed loop: identification. Unit III St Linear Optima	ariable method- Input signal design Identifiability considerations – Dir	for ide rect and Stability	entifica d indi Anal	ntion. rect	Identificat dentificat	tion of sys ion – Joir r State Esti	nt input / o	ing i outpu ende
closedloop:identification.Unit IIIUnit IIIStLinear OptimaKalman filterUnit IVA	rariable method- Input signal design Identifiability considerations – Dir tate Estimation Il State Estimation: Kalman filter - S - Bucy filter Adaptive Strate Estimation daptive Control Schemes	for ide rect and Stability on: Para	entifica d indi Anal meter	ntion. rect ysis N Identi	Identificat dentificat Ion-Linea fication v	tion of sys ion – Joir r State Esti ia Extented	imation: Ext	ing in outpu endec er
closed loop: identification. Unit III St Linear Optima Kalman filter - Unit IV A Internal Mode Stability and r control with c knowledge. In law.	variable method- Input signal design Identifiability considerations – Dir tate Estimation Il State Estimation: Kalman filter - S - Bucy filter Adaptive Strate Estimation	for ide rect and Stability on: Para paramete control ptive co	entifica d indi Anal: meter ers -A : Prob ontrol	ysis N Identi daptiv olem f	Identificat dentificat lon-Linea fication v ve Interna ormulatio pust adap	tion of sys ion – Joir r State Esti ia Extented al Model C m - Ordina tive contro	imation: Ext Kalman filto Control scher ry direct ada	ing i ing i i outpute
closedloop:identification.Identification.Unit IIIStLinear OptimaKalman filter -Unit IVAInternal ModeStability and rcontrol with cknowledge. Inlaw.Unit VAOptimal adaptstepping – InvePlants with acinverse. control	ariable method- Input signal design Identifiability considerations – Dir tate Estimation Il State Estimation: Kalman filter - S - Bucy filter Adaptive Strate Estimation daptive Control Schemes I Control (IMC) schemes: Known probustness analysis. Robust adaptive lead zone – New robust direct adaptive direct adaptive periodic control: Prob	for ide rect and Stability on: Para paramete control ptive co blem fo Problem back sys ed inve	entifica d indi Analy meter ers -A : Prob ontrol rmulat n state stem. A rses –	ysis N Identi daptiv olem f - Rol tion – ement Adapt	Identificat dentificat Ion-Linea fication v ve Interna ormulation bust adap Adaptive – Adapti ive inverse e feedbac	tion of sys ion – Joir r State Esti ia Extented al Model C on - Ordina tive control c control sc ve tracking se for actua k designs–	imation: Ext imation: Ext Kalman filte Control scher ry direct ada of with least cheme and co g – adaptive tor compens Output fee	ing i
closed loop: identification. Unit III Unit III State Linear Optimal Kalman filter - Unit IV A Internal Mode Stability and response control with control law. A Optimal adapt stepping Inverse Plants with action adaptive fuzzy/	variable method- Input signal design Identifiability considerations – Dir tate Estimation Il State Estimation: Kalman filter - S - Bucy filter Adaptive Strate Estimation daptive Control Schemes I Control (IMC) schemes: Known probustness analysis. Robust adaptive lead zone – New robust direct adaptive direct adaptive periodic control: Prob pplications of Adaptive Control ive tracking for nonlinear systems: erse concepts – Design of strict feedle tuator non-linearities – Parameterized and designs – Designs for multivative neural control.	for ide rect and Stability on: Para paramete control ptive co blem fo Problem back sys ed inve	entifica d indi Analy meter ers -A : Prob ontrol rmulat n state stem. A rses –	ysis N Identi daptiv olem f - Rol tion – ement Adapt	Identificat dentificat Ion-Linea fication v ve Interna ormulation bust adap Adaptive – Adapti ive inverse e feedbac	tion of sys ion – Joir r State Esti ia Extented al Model C on - Ordina tive control c control sc ve tracking se for actua k designs–	imation: Ext imation: Ext Kalman filte Control scher ry direct ada of with least cheme and co g – adaptive tor compens Output fee	ing i
closed loop: identification. Unit III State Linear Optimal Kalman filter - Unit IV A Internal Mode Stability and r control with c knowledge. In law. Unit V A Optimal adapt stepping – Inverse contro adaptive fuzzy/ EFERENCE(1 Torsten S	variable method- Input signal design Identifiability considerations – Dir tate Estimation Il State Estimation: Kalman filter - S - Bucy filter Adaptive Strate Estimation daptive Control Schemes I Control (IMC) schemes: Known probustness analysis. Robust adaptive lead zone – New robust direct adaptive direct adaptive periodic control: Prob pplications of Adaptive Control ive tracking for nonlinear systems: erse concepts – Design of strict feedle tuator non-linearities – Parameterized and designs – Designs for multivative neural control.	for ide rect and Stability on: Para paramete control ptive co blem fo Problem back sys ed inve ariable	entifica d indi Analy meter ers -A : Prob ontrol rmulat rses – system	ysis N Identi Identi Identi Identi Identi Identi Plem f - Rol tion – Ement Adapt State	Identificat dentificat lon-Linea fication v ve Interna ormulatic bust adap Adaptive – Adapti ive inverse feedbac 1 non-line	tion of sys ion – Joir r State Esti ia Extented al Model C m - Ordina tive control sc ve tracking se for actua k designs– ear dynamic	imation: Ext imation: Ext Kalman filte Control scher ry direct ad l with least cheme and co g – adaptive tor compens Output feed cs. Stable N	ing i

R.W-

Chairman - BoS Dept.of ECE - ESEC

3.	Lennart Ljung, System Identification: Theory for the User, Prentice-Hall, Second Edition, New Jersey, USA, 1999.
4.	Karl J.Astrom and Bjorn Wittenmark, Adaptive Control, Pearson Education, Second Edition, New Delhi, 2003.
5.	Eveleigh, V.W. Adaptive Control and optimization Techniques, Tata McGraw Hill Newyork, 2007.

R.b.

Chairman - BoS Dept.of ECE - ESEC

Programme	ME-APPLIED EI	R 2019	Semester	III				
a a 1	Course Name	Hou	rs / W	eek	Credit	Total	Maximum Marks 100	
Course Code	Course Name	L	T	Р	C	Hours		
19AEX17	DSP ARCHITECTURES AND PROGRAMMING	3	0	0	3	45		
Course Obje	ctive (s): The purpose of learning this	course is	s to					
 Study t 	he concepts of Fundamentals Of Progr	rammab	le DS	Ps, Spe	ecial Functi	ons		
Study t	he concepts of Linear Programming, A	Algebrai	c Equ	ations	& Ordinary	Differenti	al Equations	
Course Outco	omes: At the end of this course, learne	rs will b	e able	e to:				
 Unders 	tand of Fundamentals Of Programmal	ble DSP	s, Spe	cial Fu	inctions			
•= Unders	tand of Linear Programming, Algebra	ic Equa	tions	& Ordi	nary Diffe	rential Equa	ations	
Unit I FL	INDAMENTALS OF PROGRAMM	ABLE	DSPs				· · ·	9
Multiplier and	IN HE I'M AND IN NO. I'M A	D C.	64.1	1		1.		
	d Multiplier accumulator - Modified	Bus St	ructur	es and	Memory	access in H	PDSPs – Mu	ltiple
	ry - Multi-port memory - VLIW archi							
access memor On chip Perip	ry - Multi-port memory - VLIW archi							
access memor On chip Perip Unit II SI	ry – Multi-port memory – VLIW archinherals.	tecture-	Pipeli	ining –	Special A	ddressing m	nodes in P-DS	SPs - 9
access memor On chip Perip Unit II SI Architecture	y – Multi-port memory – VLIW archi herals. PECIAL FUNCTIONS	tecture- essing m	Pipeli	ining –	Special Ac	ddressing m guage Instru	nodes in P-DS	SPs - 9 eline
access memor On chip Perip Unit II SH Architecture - structure, Ope	ry – Multi-port memory – VLIW archi herals. PECIAL FUNCTIONS - Assembly language syntax - Addre	tecture- essing m	Pipeli	ining –	Special Ac	ddressing m guage Instru	nodes in P-DS	SPs - 9 eline
access memor On chip Perip Unit II SI Architecture - structure, Ope signals.	ry – Multi-port memory – VLIW archi herals. PECIAL FUNCTIONS - Assembly language syntax - Addre	tecture- essing m	Pipeli	ining –	Special Ac	ddressing m guage Instru	nodes in P-DS	SPs – 9 eline
access memor On chip Perip Unit II SH Architecture - structure, Ope signals. Unit III LI	ry – Multi-port memory – VLIW architherals. PECIAL FUNCTIONS – Assembly language syntax - Addree eration – Block Diagram of DSP sta	tecture- essing m arter kit	Pipeli nodes – Aj	ining – – Asso oplicati	Special Ad embly lang ion Progra	ddressing m guage Instru ms for pro	nodes in P-DS uctions - Pip cessing real	SPs - 9 eline time 9
access memor On chip Perip Unit II SI Architecture - structure, Ope signals. Unit III LI Architecture o	y – Multi-port memory – VLIW archi herals. PECIAL FUNCTIONS - Assembly language syntax - Addre eration – Block Diagram of DSP sta NEAR PROGRAMMING	essing m arter kit	Pipeli nodes – Aj	ining – – Asse oplicati	Special Ad embly lang ion Progra System: In	ddressing m guage Instru ms for pro	uctions - Pip cessing real – DSP Starte	SPs - 9 eline time 9 r Kit
access memor On chip Perip Unit II SI Architecture - structure, Ope signals. Unit III LI Architecture of Support Tools	ry – Multi-port memory – VLIW architherals. PECIAL FUNCTIONS – Assembly language syntax - Addree eration – Block Diagram of DSP state NEAR PROGRAMMING of the C6x Processor - Instruction Set -	essing marter kit - DSP D Files -	Pipeli nodes – Aj	ining – – Asse oplicati	Special Ad embly lang ion Progra System: In	ddressing m guage Instru ms for pro	uctions - Pip cessing real – DSP Starte	SPs - 9 eline time 9 r Kit
access memor On chip Perip Unit II SI Architecture - structure, Ope signals. Unit III LI Architecture of Support Tools Application P	y – Multi-port memory – VLIW architherals. PECIAL FUNCTIONS – Assembly language syntax - Addreeration – Block Diagram of DSP state NEAR PROGRAMMING of the C6x Processor - Instruction Set - S- Code Composer Studio - Support	essing marter kit - DSP D Files -	Pipeli nodes – Aj	ining – – Asse oplicati	Special Ad embly lang ion Progra System: In	ddressing m guage Instru ms for pro	uctions - Pip cessing real – DSP Starte	SPs - 9 eline time 9 r Kit
access memorOn chip PeripUnit IISIArchitecturestructure, Opesignals.Unit IIILIArchitecture ofSupport ToolsApplication PUnit IVAIArchitecture of	ry – Multi-port memory – VLIW architherals. PECIAL FUNCTIONS – Assembly language syntax - Addree eration – Block Diagram of DSP state NEAR PROGRAMMING of the C6x Processor - Instruction Set - s- Code Composer Studio - Support rograms for processing real time signal	essing m arter kit - DSP D Files - ls.	Pipeli nodes – Aj Develo Progr DSP	ining – – Asso oplicati pment ammin proces	Special Ad embly lang ion Progra System: In g Example sors- Addu	ddressing m guage Instru- ms for pro itroduction es to Test t	uctions - Pip cessing real – DSP Starte the DSK Too	SPs - 9 eline time 9 r Kit ols - 9
access memor On chip Perip Unit II SI Architecture - structure, Ope signals. Unit III LI Architecture of Support Tools Application P Unit IV AI Architecture of language instr	y – Multi-port memory – VLIW archin herals. PECIAL FUNCTIONS - Assembly language syntax - Addree eration – Block Diagram of DSP state NEAR PROGRAMMING of the C6x Processor - Instruction Set - s- Code Composer Studio - Support rograms for processing real time signa LGEBRAIC EQUATIONS of ADSP-21XX and ADSP-210XX set	essing marter kit - DSP D Files - ls. eries of r design,	Pipeli nodes – Aj Develo Progr DSP , FFT	ining – – Asso oplicati pment ammin proces	Special Ad embly lang ion Progra System: In g Example sors- Addu	ddressing m guage Instru- ms for pro itroduction es to Test t	uctions - Pip cessing real – DSP Starte the DSK Too	SPs - 9 eline time 9 r Kit ols - 9
access memorOn chip PeripUnit IISIArchitecture -structure, Opesignals.Unit IIILIArchitecture ofSupport ToolsApplication PrUnit IVAIArchitecture oflanguage instrUnit VOI	y – Multi-port memory – VLIW archin herals. PECIAL FUNCTIONS - Assembly language syntax - Addree eration – Block Diagram of DSP state NEAR PROGRAMMING of the C6x Processor - Instruction Set - s- Code Composer Studio - Support rograms for processing real time signa LGEBRAIC EQUATIONS of ADSP-21XX and ADSP-210XX set uctions – Application programs –Filter	essing marter kit - DSP D Files - ls. - design, - TIONS	Pipeli nodes – Aj Develo Progr DSP , FFT	ning – – Asso oplicati pment ammin proces calcula	Special Ad embly lang ion Progra System: In g Example sors- Addr ation.	ddressing m guage Instru- ms for pro- ntroduction es to Test to ressing mod	nodes in P-DS uctions - Pip cessing real – DSP Starte the DSK Too des and asser	9 elina time 9 r Ki ols - 9 mbly 9

REF	ERENCE(S):
1.	Avtar Singh and S. Srinivasan, Digital Signal Processing – Implementations using DSP Microprocessors with Examples from TMS320C54xx, cengage Learning India Private Limited, Delhi 2012
2.	B. Venkataramani and M.Bhaskar, Digital Signal Processors – Architecture, Programming and Applications – Tata McGraw – Hill Publishing Company Limited. New Delhi, 2003.
3.	RulphChassaing, Digital Signal Processing and Applications with the C6713 and C6416 DSK, A JOHN WILEY & SONS, INC., PUBLICATION, 2015
4.	User guides Texas Instrumentation, Analog Devices, Motorola.

P.10-

Chairman - Bos Dept.of ECE - ESEC

Programme	ME-APPLIED EL	ECTR	RONIC	CS		R 2019	Semester	III
Course Code	Course Name	Hou	rs / W	eek	Credit	Total Hours	Maxim	um
Course Code	course mane	L	Т	Р	С		Marks	
19AEX18	SPEECH AND AUDIO SIGNAL PROCESSING	3	0	0	3	45	100	
Course Object	tive (s): The purpose of learning this co	ourse i	s to					
Study ba	asic concepts of processing speech and	audio	signa	ls				
 Study an 	nd analyze various M-band filter-banks	s for au	udio co	oding				
• Underst	and audio coding based on transform c	oders.						
Study til	me and frequency domain speech proce	essing	metho	ods			A second second	
Course Outco	mes: At the end of this course, learners	s will b	be able	e to:				
Evaluate	e audio coding and transform coders							
• Discuss	time and frequency domain methods for	or spee	ech pro	ocessin	g	-		
• Explain	predictive analysis of speech							
Jnit I ME	CHANICS OF SPEECH AND AUD	10						9
	Review of Signal Processing Theory-							
Discrete time	modelling of Speech production - C	Classif	ication	n of Sp	eech sound	ds – Phone	es – Phonen	nes ·
	Phonemic alphabets - Articulatory fe					172.0		
Simultaneous	Masking, Masking-Asymmetry, and	the s	Spread	d of M	asking- No	on-simultar	neous Maski	ing
Percentual Fr	ntropy - Basic measuring philosophy	. C.I	tiv	in the second	a objective	NE REPRESENCE	Verill Agreements and their	1. Sec. 10. 10. 10.
refeeptual Li	httopy - Basic measuring philosophy	y -Suc	ojectiv	e versi	is objectiv	e perceptu	al testing -	Th
see the state of the state of the state of the state of the	dio quality measure (PAQM) - Cogniti		and the second second			the second second second	al testing -	Th
perceptual aud Jnit II TIN	dio quality measure (PAQM) - Cognitiv ME-FREQUENCY ANALYSIS: FIL	ve effe TER	ects in BANH	judging KS ANI	g audio qua	lity. FORMS		9
perceptual aud Jnit II TIN ntroduction - A	dio quality measure (PAQM) - Cogniti ME-FREQUENCY ANALYSIS: FIL Analysis-Synthesis Framework for M-	ve effe / TER band F	ects in BANH Filter I	judging KS AN Banks-	g audio qua D TRANSI Filter Bank	lity. FORMS s for Audio	o Coding: D	9 esig
perceptual aud Init II TI ntroduction - A Considerations	dio quality measure (PAQM) - Cognitie ME-FREQUENCY ANALYSIS: FIL Analysis-Synthesis Framework for M- - Quadrature Mirror and Conjugate Q	ve effe / TER band I uadrat	ects in BANH Filter I ure Fi	judging KS AN Banks- lters - T	g audio qua D TRANSI Filter Bank Free-Structu	lity. FORMS s for Audio ared QMF a	o Coding: Do and CQF M-	9 esig ban
perceptual aud Jnit II TIM ntroduction - A Considerations Banks - Cosine	dio quality measure (PAQM) - Cognitiv ME-FREQUENCY ANALYSIS: FIL Analysis-Synthesis Framework for M- - Quadrature Mirror and Conjugate Q e Modulated "Pseudo QMF" M-band H	ve effe / TER band I uadrat Banks	ects in BANH Filter I ure Fi -Cosin	judging KS AN Banks- Iters - T ne Mod	g audio qua D TRANSI Filter Bank Free-Structu ulated Perf	lity. FORMS s for Audio ared QMF a fect Recons	o Coding: Do and CQF M- struction (PR	9 esig ban) M
perceptual aud Jnit II TIM Introduction - A Considerations Banks - Cosine	dio quality measure (PAQM) - Cognitie ME-FREQUENCY ANALYSIS: FIL Analysis-Synthesis Framework for M- - Quadrature Mirror and Conjugate Q	ve effe / TER band I uadrat Banks	ects in BANH Filter I ure Fi -Cosin	judging KS AN Banks- Iters - T ne Mod	g audio qua D TRANSI Filter Bank Free-Structu ulated Perf	lity. FORMS s for Audio ared QMF a fect Recons	o Coding: Do and CQF M- struction (PR	9 esign band
perceptual aud J nit II TI ntroduction - A Considerations Banks - Cosine band Banks ar	dio quality measure (PAQM) - Cognitiv ME-FREQUENCY ANALYSIS: FIL Analysis-Synthesis Framework for M- - Quadrature Mirror and Conjugate Q e Modulated "Pseudo QMF" M-band H	ve effe TER band I uadrat Banks nsform	ects in BANH Filter H ure Fi -Cosin n (MD	judging KS AN Banks- Iters - T ne Mod	g audio qua D TRANSI Filter Bank Free-Structu ulated Perf	lity. FORMS s for Audio ared QMF a fect Recons	o Coding: Do and CQF M- struction (PR	9 esign band
perceptual aud Init II TIM ntroduction - A Considerations Banks - Cosine band Banks ar Transform - Pre- Unit III AU	dio quality measure (PAQM) - Cognitiv ME-FREQUENCY ANALYSIS: FIL Analysis-Synthesis Framework for M- - Quadrature Mirror and Conjugate Q e Modulated "Pseudo QMF" M-band H and the Modified Discrete Cosine Tran- e-echo Distortion- Pre-echo Control St DIO CODING AND TRANSFORM	ve effe TER band I uadrat Banks nsform rategie COD	ects in BANH Filter H ure Fi -Cosin n (MD es ERS	judging SS AN Banks- Iters - T ne Mod OCT) -	g audio qua D TRANSI Filter Bank Free-Structu ulated Perf Discrete F	lity. FORMS s for Audio ured QMF a ect Recons ourier and	o Coding: Do and CQF M- struction (PR Discrete Co	9 esign band) M osind 9
perceptual aud Jnit II TIN ntroduction - I Considerations Banks - Cosine pand Banks ar Transform - Pro Jnit III AU Lossless Audio	dio quality measure (PAQM) - Cognitie ME-FREQUENCY ANALYSIS: FIL Analysis-Synthesis Framework for M- - Quadrature Mirror and Conjugate Q e Modulated "Pseudo QMF" M-band H and the Modified Discrete Cosine Trans- e-echo Distortion- Pre-echo Control St DIO CODING AND TRANSFORM to Coding – Lossy Audio Coding -	ve effe TER band F uadrat Banks nsform rategie COD ISO-M	ects in BANH Filter Fi ure Fi -Cosin n (MD es ERS MPEG-	judging (S AN) Banks- Iters - T ne Mod DCT) - -1A, 2.	g audio qua D TRANSI Filter Bank Free-Structu ulated Perf Discrete F	lity. FORMS s for Audio ared QMF a ect Recons ourier and aned, 4A	o Coding: Do and CQF M- struction (PR Discrete Co Audio Codi	9 esign band) M osind osind 9 ing
perceptual aud Init II TIM ntroduction - A Considerations Banks - Cosine band Banks ar Transform - Pro Init III AU Lossless Audio Dptimum Codi	dio quality measure (PAQM) - Cognitiv ME-FREQUENCY ANALYSIS: FIL Analysis-Synthesis Framework for M- - Quadrature Mirror and Conjugate Q e Modulated "Pseudo QMF" M-band H ad the Modified Discrete Cosine Tran- e-echo Distortion- Pre-echo Control St DIO CODING AND TRANSFORM to Coding – Lossy Audio Coding – ing in the Frequency Domain – Perce	ve effe TER band I uadrat Banks nsform rategie COD ISO-M ptual	ects in BANH Filter F ure Fi -Cosin n (MD es ERS MPEG- Transf	judging (S AN) Banks- Iters - T ne Mod DCT) - -1A, 2. form C	g audio qua D TRANSI Filter Bank Free-Structu lulated Perf Discrete F A, 2A-Adv oder –Bran	lity. FORMS s for Audio ured QMF a ect Recons ourier and raned, 4A denburg -	o Coding: Do and CQF M- struction (PR Discrete Co Audio Codi Johnston Hy	9 esig ban) M osin osin 9 ing ybrid
perceptual aud Jnit II TIN ntroduction - I Considerations Banks - Cosine band Banks ar Transform - Pro Jnit III AU Lossless Audio Optimum Codi Coder - CNET	dio quality measure (PAQM) - Cognitie ME-FREQUENCY ANALYSIS: FIL Analysis-Synthesis Framework for M- - Quadrature Mirror and Conjugate Q e Modulated "Pseudo QMF" M-band H and the Modified Discrete Cosine Trans- e-echo Distortion- Pre-echo Control St DIO CODING AND TRANSFORM to Coding – Lossy Audio Coding - ing in the Frequency Domain - Percer Coders - Adaptive Spectral Entropy C	ve effe TER band I uadrat Banks nsform rategic COD ISO-M ptual Coding	ects in BANH Filter H ure Filter H -Cosin n (MD es ERS MPEG Transf g –Diff	judging (S AN) Banks- Iters - T ne Mod DCT) - - 1A, 2 form C ferentia	g audio qua D TRANSI Filter Bank Free-Structu ulated Perf Discrete F A, 2A-Adw oder –Bran I Perceptua	lity. FORMS s for Audio ured QMF a ect Recons ourier and raned, 4A denburg -	o Coding: Do and CQF M- struction (PR Discrete Co Audio Codi Johnston Hy	9 esig ban) M osin osin 9 ing ybrid
perceptual auditionUnit IITIMIntroduction - IConsiderationsBanks - Cosineband Banks arFransform - PriUnit IIIAULossless AuditionOptimum CoditionCoder - CNETSubstitution - D	dio quality measure (PAQM) - Cognitie ME-FREQUENCY ANALYSIS: FIL Analysis-Synthesis Framework for M- - Quadrature Mirror and Conjugate Q e Modulated "Pseudo QMF" M-band H and the Modified Discrete Cosine Trans- e-echo Distortion- Pre-echo Control St DIO CODING AND TRANSFORM to Coding – Lossy Audio Coding – ing in the Frequency Domain – Percer Coders - Adaptive Spectral Entropy C CT with Vector Quantization -MDCT	ve effe TER band I uadrat Banks nsform rategic COD ISO-M ptual Coding with V	ects in BANH Filter H ure Fi -Cosin (MD es ERS MPEG Transf (-Diff /ector	judging KS ANI Banks- Iters - T ne Mod DCT) - -1A, 2, form C ferentia Quanti	g audio qua D TRANSI Filter Bank Free-Structu lulated Perf Discrete F A, 2A-Adw oder –Bran I Perceptua zation	lity. FORMS s for Audio red QMF a ect Recons ourier and raned, 4A denburg - I Audio Co	o Coding: Do and CQF M- struction (PR Discrete Co Audio Codi Johnston Hy oder - DFT N	9 band band band band band band 9 ing ybrid Noise
perceptual audUnit IITINIntroduction - IConsiderationsBanks - CosineDand Banks arTransform - ProUnit IIIAULossless AudioOptimum CodiCoder - CNETSubstitution -DUnit IVTIN	dio quality measure (PAQM) - Cognitiv ME-FREQUENCY ANALYSIS: FIL Analysis-Synthesis Framework for M- - Quadrature Mirror and Conjugate Q e Modulated "Pseudo QMF" M-band H and the Modified Discrete Cosine Tra- e-echo Distortion- Pre-echo Control St DIO CODING AND TRANSFORM to Coding – Lossy Audio Coding – ing in the Frequency Domain - Perce Coders - Adaptive Spectral Entropy C CT with Vector Quantization -MDCT ME AND FREQUENCY DOMAIN M	ve effe TER band I uadrat Banks nsform rategic COD ISO-N ptual Coding with V METH	ects in BANH Filter I ure Fil -Cosin (MD es ERS MPEG Transf g -Diff Vector IODS	judging (S AN) Banks- Iters - T ne Mod OCT) - -1A, 2, form C form C form C form C form S	g audio qua D TRANSI Filter Bank Free-Structu Julated Perf Discrete F A, 2A-Adw oder –Bran I Perceptua zation PEECH P	lity. FORMS s for Audio ured QMF a cect Recons ourier and caned, 4A denburg - l Audio Co ROCESSI	o Coding: Do and CQF M- struction (PR Discrete Co Audio Codi Johnston Hy oder - DFT N	9 esign band) M osind osind 9 ybrid Noise 9
perceptual audUnit IITINIntroduction - IConsiderationsBanks - Cosineband Banks arTransform - ProUnit IIIAULossless AudioOptimum CodiCoder - CNETSubstitution -DUnit IVTINTime domain	dio quality measure (PAQM) - Cognitie ME-FREQUENCY ANALYSIS: FIL Analysis-Synthesis Framework for M- - Quadrature Mirror and Conjugate Q e Modulated "Pseudo QMF" M-band H and the Modified Discrete Cosine Trans- e-echo Distortion- Pre-echo Control St DIO CODING AND TRANSFORM to Coding – Lossy Audio Coding - ing in the Frequency Domain - Percer Coders - Adaptive Spectral Entropy C CT with Vector Quantization -MDCT ME AND FREQUENCY DOMAIN M parameters of Speech signal – Met	ve effe TER band I uadrat Banks nsform rategic COD ISO-M ptual Coding with V VETH thods	ects in BANH Filter H ure Fi -Cosin (MD es ERS APEG- Transf g –Diff Vector IODS for e	judging (S AN) Banks- Iters - T ne Mod DCT) - -1A, 2. form C form C ferentia Quanti FOR S xtractin	g audio qua D TRANSI Filter Bank Free-Structu lulated Perf Discrete F A, 2A-Adw oder –Bran I Perceptua zation PEECH P g the para	lity. FORMS s for Audio ared QMF a ect Recons ourier and raned, 4A denburg - l Audio Co ROCESSI ameters :E	o Coding: Do and CQF M- struction (PR Discrete Co Audio Codi Johnston Hy oder - DFT N NG nergy, Aver	9 essig ban () M ossin 9 ing ybrid Noise 9 rage
perceptual audUnit IITINIntroduction - IConsiderationsBanks - Cosineband Banks arTransform - PriUnit IIIAULossless AudioOptimum CodiCoder - CNETSubstitution -DUnit IVTINFime domainMagnitude - Z	dio quality measure (PAQM) - Cognitiv ME-FREQUENCY ANALYSIS: FIL Analysis-Synthesis Framework for M- - Quadrature Mirror and Conjugate Q e Modulated "Pseudo QMF" M-band H and the Modified Discrete Cosine Trans- e-echo Distortion- Pre-echo Control St DIO CODING AND TRANSFORM to Coding – Lossy Audio Coding – ing in the Frequency Domain – Percer Coders - Adaptive Spectral Entropy C CT with Vector Quantization -MDCT ME AND FREQUENCY DOMAIN M parameters of Speech signal – Meter ero crossing Rate – Silence Discriminal	ve effe TER band F uadrat Banks nsform rategic COD ISO-M ptual Coding with V METH thods ation u	ects in BANH Filter H ure Fi -Cosin (MD es ERS MPEG Transf (-Diff /ector IODS for e: using 2	judging KS ANJ Banks- Iters - T ne Mod DCT) - -1A, 2, form C ferentia Quanti FOR S xtractin ZCR an	g audio qua D TRANSI Filter Bank Free-Structu ulated Perf Discrete F A, 2A-Adw oder –Bran I Perceptua zation PEECH P g the para d energy S	lity. FORMS s for Audio ared QMF a ect Reconstourier and caned, 4A denburg - l Audio Co ROCESSI ameters :E hort Time	o Coding: Do and CQF M- struction (PR Discrete Co Audio Codi Johnston Hy oder - DFT N NG nergy, Aver Fourier anal	9 esig ban) M osin 9 ing ybrid Noise 9 age ysis
perceptual aud Unit II TIN Introduction - I Considerations Banks - Cosine band Banks ar Transform - Pro Jnit III AU Lossless Audio Optimum Codi Coder - CNET Substitution -D Jnit IV TIN Fime domain Magnitude - Z Formant extr	dio quality measure (PAQM) - Cognitie ME-FREQUENCY ANALYSIS: FIL Analysis-Synthesis Framework for M- - Quadrature Mirror and Conjugate Q e Modulated "Pseudo QMF" M-band H and the Modified Discrete Cosine Tran- e-echo Distortion- Pre-echo Control St DIO CODING AND TRANSFORM to Coding – Lossy Audio Coding - ing in the Frequency Domain - Percer Coders - Adaptive Spectral Entropy C CT with Vector Quantization -MDCT ME AND FREQUENCY DOMAIN M parameters of Speech signal – Metero ero crossing Rate – Silence Discrimina- raction – Pitch Extraction using time	ve effe TER band I uadrat Banks nsform rategic COD ISO-M ptual Coding with V METH thods ation u and f	ects in BANH Filter H ure Filter H -Cosin n (MD es ERS APEG Transf g –Diff Vector IODS for ecusing 2 freque	judging (S AN) Banks- Iters - T ne Mod OCT) - -1A, 2 form C form C form C ferentia Quanti FOR S xtractin ZCR an ncy do	g audio qua D TRANSI Filter Bank Free-Structu lulated Perf Discrete F A, 2A-Adw oder –Bran I Perceptua zation PEECH P g the para d energy S main metho	lity. FORMS s for Audio ured QMF a ect Recons ourier and aned, 4A denburg - l Audio Co ROCESSI ameters :E hort Time ods Homor	o Coding: Do and CQF M- struction (PR Discrete Co Audio Codi Johnston Hy oder - DFT N NG nergy, Aver Fourier anal morphic Spe	9 esig ban) M osin 9 ing ybrid Noise 9 age ysis
perceptual aud Jnit II TII Introduction - I Considerations Banks - Cosine band Banks ar Fransform - Pre Jnit III AU Lossless Audio Optimum Codi Coder - CNET Substitution -D Jnit IV TIN Fime domain Magnitude - Z Formant extra	dio quality measure (PAQM) - Cognitie ME-FREQUENCY ANALYSIS: FIL Analysis-Synthesis Framework for M- - Quadrature Mirror and Conjugate Q e Modulated "Pseudo QMF" M-band H and the Modified Discrete Cosine Trans- e-echo Distortion- Pre-echo Control St DIO CODING AND TRANSFORM to Coding – Lossy Audio Coding – ing in the Frequency Domain – Perce Coders - Adaptive Spectral Entropy C CT with Vector Quantization -MDCT ME AND FREQUENCY DOMAIN M parameters of Speech signal – Metero ero crossing Rate – Silence Discrimina- raction – Pitch Extraction using time tral analysis of Speech – Formant and D	ve effe TER band I uadrat Banks nsform rategie COD ISO-M ptual Coding with V METH thods ation u and f Pitch I	ects in BANH Filter H ure Filter H -Cosin n (MD es ERS APEG Transf g –Diff Vector IODS for ecusing 2 freque	judging (S AN) Banks- Iters - T ne Mod OCT) - -1A, 2 form C form C form C ferentia Quanti FOR S xtractin ZCR an ncy do	g audio qua D TRANSI Filter Bank Free-Structu lulated Perf Discrete F A, 2A-Adw oder –Bran I Perceptua zation PEECH P g the para d energy S main metho	lity. FORMS s for Audio ured QMF a ect Recons ourier and aned, 4A denburg - l Audio Co ROCESSI ameters :E hort Time ods Homor	o Coding: Do and CQF M- struction (PR Discrete Co Audio Codi Johnston Hy oder - DFT N NG nergy, Aver Fourier anal morphic Spe	9 essig band osin 9 ybrid Noise 9 rage ysis eech
perceptual aud Jnit II TIN Introduction - J Considerations Banks - Cosine band Banks ar Transform - Pro Jnit III AU Lossless Audio Optimum Codi Coder - CNET Substitution -D Jnit IV TIN Time domain Magnitude - Z Formant extra Analysis: Ceps Jnit V PR	dio quality measure (PAQM) - Cognitiv ME-FREQUENCY ANALYSIS: FIL Analysis-Synthesis Framework for M- - Quadrature Mirror and Conjugate Q e Modulated "Pseudo QMF" M-band H and the Modified Discrete Cosine Tran- e-echo Distortion- Pre-echo Control St DIO CODING AND TRANSFORM to Coding – Lossy Audio Coding - ing in the Frequency Domain - Perce Coders - Adaptive Spectral Entropy C CT with Vector Quantization -MDCT ME AND FREQUENCY DOMAIN M parameters of Speech signal – Meter ero crossing Rate – Silence Discrimina- raction – Pitch Extraction using time tral analysis of Speech – Formant and D EDICTIVE ANALYSIS OF SPEECH	ve effe TER band I uadrat Banks nsform rategic COD ISO-M ptual Coding with V METH thods ation u and f Pitch I H	ects in BANH Filter H ure Filter H -Cosin n (MD es ERS APEG Transf g –Diff /ector IODS for e: using 2 freque: Estima	judging (S AN) Banks- Iters - T ne Mod OCT) - -1A, 2 form C form	g audio qua D TRANSI Filter Bank Free-Structu lulated Perf Discrete F A, 2A-Adw oder –Bran I Perceptua zation PEECH P og the para d energy S main meth- Homomorp	lity. FORMS s for Audio ared QMF a ect Recons ourier and aned, 4A denburg - l Audio Co ROCESSI ameters :E hort Time ods Homon hic Vocode	o Coding: Do and CQF M- struction (PR Discrete Co Audio Codi Johnston Hy oder - DFT N NG nergy, Aver Fourier anal morphic Spe	9 esig ban) M osin 9 ybrid Nois 9 vage ysis eech 9
perceptual audUnit IITIIntroduction - IConsiderationsBanks - Cosineband Banks arTransform - PreUnit IIIAULossless AudieOptimum CodieCoder - CNETSubstitution -DUnit IVTINTime domainMagnitude - ZFormant extrAnalysis: CepsUnit VPRCormulation of	dio quality measure (PAQM) - Cognitie ME-FREQUENCY ANALYSIS: FIL Analysis-Synthesis Framework for M- - Quadrature Mirror and Conjugate Q e Modulated "Pseudo QMF" M-band H and the Modified Discrete Cosine Trans- e-echo Distortion- Pre-echo Control St DIO CODING AND TRANSFORM to Coding – Lossy Audio Coding – ing in the Frequency Domain – Percer Coders - Adaptive Spectral Entropy C CT with Vector Quantization -MDCT ME AND FREQUENCY DOMAIN M parameters of Speech signal – Meter ero crossing Rate – Silence Discrimina- raction – Pitch Extraction using time tral analysis of Speech – Formant and D EDICTIVE ANALYSIS OF SPEECH Linear Prediction problem in Time	ve effe TER band I uadrat Banks nsform rategic COD ISO-M ptual Coding with V METH thods ation u and f Pitch I H Doma	ects in BANH Filter H ure Fi -Cosin (MD es ERS APEG- Transf (-Diff Vector IODS for e. using 2 freque: Estima	judging KS ANJ Banks- Iters - T ne Mod DCT) - -1A, 2, form C form C ferentia Quanti FOR S xtractin ZCR an ncy do ttion - I Basic P	g audio qua D TRANSI Filter Bank Free-Structu lulated Perf Discrete F A, 2A-Adv oder –Bran I Perceptua zation PEECH P Ig the para id energy S main metho Homomorp Principle –	lity. FORMS s for Audio ared QMF a ect Recons ourier and raned, 4A denburg - l Audio Co ROCESSI ameters :E hort Time ods Homon hic Vocode	o Coding: Do and CQF M- struction (PR Discrete Co Audio Codi Johnston Hy oder - DFT N NG nergy, Aver Fourier anal morphic Spe ers	9 essig ban osin 9 ng ybrid Noise Noise 9 rage ysis eech 9 od -
perceptual aud Unit II TIN Introduction - I Considerations Banks - Cosine band Banks ar Transform - Pre Unit III AU Lossless Audio Optimum Codi Coder - CNET Substitution -D Unit IV TIN Fime domain Magnitude - Z - Formant extra Analysis: Ceps Unit V PR Covariance met	dio quality measure (PAQM) - Cognitie ME-FREQUENCY ANALYSIS: FIL Analysis-Synthesis Framework for M- - Quadrature Mirror and Conjugate Q e Modulated "Pseudo QMF" M-band H and the Modified Discrete Cosine Trans- e-echo Distortion- Pre-echo Control St DIO CODING AND TRANSFORM to Coding – Lossy Audio Coding – ing in the Frequency Domain – Percer Coders - Adaptive Spectral Entropy C CT with Vector Quantization -MDCT ME AND FREQUENCY DOMAIN M parameters of Speech signal – Meter ero crossing Rate – Silence Discrimina- raction – Pitch Extraction using time tral analysis of Speech – Formant and D EDICTIVE ANALYSIS OF SPEECH Linear Prediction problem in Time thod – Solution of LPC equations – C	ve effe TER band F uadrat Banks nsform rategie COD ISO-N ptual Coding with V TETH thods ation u and f Pitch F H Doma holesk	ects in BANH Filter H ure Fi -Cosin (MD es ERS MPEG Transf (-Diff Vector IODS for e: using 2 freque: Estima	judging KS ANI Banks- Iters - T ne Mod DCT) - -1A, 2, form C ferentia Quanti FOR S xtractin ZCR an ncy do tion - I Basic F thod - 1	g audio qua D TRANSI Filter Bank Free-Structu ulated Perf Discrete F A, 2A-Adv oder –Bran I Perceptua zation PEECH P g the para d energy S main meth- Homomorp Principle – Durbin''s R	lity. FORMS s for Audio ared QMF a ect Reconstourier and caned, 4A denburg - l Audio Corre ameters :E hort Time ods Homon hic Vocode Auto corre ecursive al	o Coding: Do and CQF M- struction (PR Discrete Co Audio Codi Johnston Hy oder - DFT N NG nergy, Aver Fourier anal morphic Spe ers	9 esig ban osin 9 ing ybrid Nois 9 rage ysis eech 9 od -
perceptual aud Jnit II TIN Introduction - I Considerations Banks - Cosine band Banks ar Transform - Pro Jnit III AU Lossless Audio Dptimum Codi Coder - CNET Substitution -D Jnit IV TIN Fime domain Magnitude - Z - Formant extra Analysis: Cepsi Jnit V PR Ormulation of Covariance met Domation and s	dio quality measure (PAQM) - Cognitie ME-FREQUENCY ANALYSIS: FIL Analysis-Synthesis Framework for M- - Quadrature Mirror and Conjugate Q e Modulated "Pseudo QMF" M-band H and the Modified Discrete Cosine Trans- e-echo Distortion- Pre-echo Control St DIO CODING AND TRANSFORM to Coding – Lossy Audio Coding – ing in the Frequency Domain – Percer Coders - Adaptive Spectral Entropy C CT with Vector Quantization -MDCT ME AND FREQUENCY DOMAIN M parameters of Speech signal – Meter ero crossing Rate – Silence Discrimina- raction – Pitch Extraction using time tral analysis of Speech – Formant and D EDICTIVE ANALYSIS OF SPEECH Linear Prediction problem in Time	ve effe TER band I uadrat Banks nsform rategie COD ISO-M ptual Coding with V METH thods ation u and f Pitch I H Doma holesk ethods	ects in BANH Filter H ure Fi -Cosin (MD es ERS MPEG Transf (-Diff Vector IODS for e: using 2 freque: Estima	judging KS ANI Banks- Iters - T ne Mod DCT) - -1A, 2, form C ferentia Quanti FOR S xtractin ZCR an ncy do tion - I Basic F thod - 1	g audio qua D TRANSI Filter Bank Free-Structu ulated Perf Discrete F A, 2A-Adv oder –Bran I Perceptua zation PEECH P g the para d energy S main meth- Homomorp Principle – Durbin''s R	lity. FORMS s for Audio ared QMF a ect Reconstourier and caned, 4A denburg - l Audio Corre ameters :E hort Time ods Homon hic Vocode Auto corre ecursive al	o Coding: Do and CQF M- struction (PR Discrete Co Audio Codi Johnston Hy oder - DFT N NG nergy, Aver Fourier anal morphic Spe ers	9 esig ban) M osin 9 ybri Nois 9 vage ysis eech 9 od -

Chairman - BoS Dept.of ECE - ESE

REF	ERENCE(S):
1.	B.Gold and N.Morgan, Speech and Audio Signal Processing, Wiley and Sons, 2018.
2.	L.R.Rabiner and R.W.Schaffer, Digital Processing of Speech Signals, Prentice Hall, 2002.
3.	Mark Kahrs, Karlheinz Brandenburg, Kluwer Applications of Digital Signal Processing to Audio And Acoustics, Academic Publishers,
4.	Udo Zölzer, Digital Audio Signal Processing, Second Edition A John Wiley& sons Ltd

1

Chairman - BoS Dept.of ECE - ESEC

Programme	ME-APPLIED ELE	ECT	RONIC	CS		R 2019	Semester	
Course Code		Hours / Week			Credit	Total Hours	Maximu Marks	ım
		L	Т	Ρ	С			
19AEX21	MULTIMEDIA COMPRESSION TECHNIQUES	3	0	0	3	45	100)
 To under audio, im To under technolog To appred To unders 	tive (s): The purpose of learning t stand the basic ideas of compression age and Video. rstand the principles and standard gies, algorithms, and performance. ciate the use of compression in multin stand and implement compression sta mes: nt basic compression algorithms with	n alg ls an medi anda	orithms nd thei ia proce rds in d	relate r app essing etail.	ed to multin plications v application	vith an emp	phasis on und	lerlyin
	in diside compression algorithms with ad implement some basic compressio				5 equivaler	n open soure	e environment.	
	analyze different approaches of com				ms in multi	media related	d mini projects	-
	NDAMENTALS OF COMPRESSI							9
udio – Storage	nultimedia – Graphics, Image and V requirements of multimedia applica nents of Information Theory – Error I	ation	s – Ne	ed fo	r compress	ion – Taxor	nomy of comp	
and the second se	(T COMPRESSION	Fice	Compi	655101	II – LOSSY C	ompression.		9
	- Adaptive Huffman coding – Arithm	netic	coding	- Sha	annon-Fano	coding – D	ictionary techn	
ZW family algo						Ũ		
	GE COMPRESSION		1.1	1.1				9
	on: Fundamentals — Compression n – Implementation using Filters – E							
	DIO COMPRESSION	-						9
	on Techniques - law, A-Law comp							
	tion to speech coding - G.722 - N	MPE	G audi	o – p	rogressive	encoding -	Silence compr	ression
and the second se	on – Formant and CELP vocoders.			-				
	EO COMPRESSION							9
nd MPEG-4 - M	n techniques and Standards – MPEG otion estimation and compensation te rrent Trends in Compression standard	echn						
REFERENCE(5):					1		
	Solomon, "Data Compression - The	Cor	nplete l	Refere	ence", Four	th Edition, S	Springer Verlog	g, Nev
	Hankerson, Greg A Harris, Peter ssion' Second Edition, Chapman					o Informatio	on Theory and	d Dat
2010.	Sayood: Introduction to Data Comp				1.1.1.2	in Harcourt	India, Third E	Editior
	Drew, Ze-Nian Li, "Fundamentals o		and the second se	and the second se	and the second se			
	mes : Digital Video Compression, M							
	Shi, Huifang Sun, "Image and Vide entals", CRC Press, 2003	eo C	ompres	sion f	or Multime	edia Enginee	ering, Algorithi	ns an

R.b-

Chairman - BoS Dept.of ECE - ESEC

Programme	gramme ME-APPLIED ELECTRONICS							· II
C C 1	Course Name		ours / V	Week	Credit	Total	Maxim	um
Course Code	Course Name	L	Т	Р	С	Hours	Marks	
19AEX20	WAVELET TRANSFORMS AND ITS APPLICATIONS	3	0	0	3	45	100	
Course Object	ive (s): The purpose of learning this con	urse is	s to					
 Study the 	e basics of signal representation and Fo	urier	theory					
• Understa	and Multi Resolution Analysis and Wav	elet c	oncepts	3				
 Study the 	e wavelet transform in both continuous	and d	iscrete	domain	is:			
 Understa 	and the applications of Wavelet transfor	m						
ourse Outcom	es: At the end of this course, learners w	ill be	able to	:				
 Identify t 	the limitations of Fourier transforms an	d its a	pplicat	ions				
	wavelet transform based coding							
	signals and images using wavelet trans	forms						
	oduction							9
ector spaces -	properties - dot product - basis-dim	ensio	n, orth	ogonali	ty and ort	honormali	ty-relations	hip
	and signals-signal spaces-concept of co			-				T
	ier Analysis and STFT	0			1	0.0		9
	orm-drawbacks of Fourier analysis- wi	ndow	functio	on - Sh	ort-time F	ourier Tra	nsform (ST	FT)
	ogram plot-phase-space plot in time-fre							
	uency plane for STFT.				U			0
Unit III Cont	inuous Wavelet Transform							9
Wavelet transfo	rm properties-concept of scale and its	relatio	on with	freque	ncy-contin	uous Wave	elet Transfo	rm
	function and wavelet functions: Daube							
orthogonal wave	elets - Tilling of time scale plane for CV	WΤ.			1			
Unit IV Discr	ete Wavelet Transform and Multi-Re	esolut	tion An	alysis				9
Discrete Wavel	et Transform (DWT)-Filter bank and	sub-t	and co	ding p	rinciples. N	Multi-resol	ution analy	sis-
Fime scale diffe	erence equations for wavelets and scal	ing fi	inctions	s-Wave	let filters-s	scale varia	tion in disc	rete
domain-Mallet's	s algorithm for DWT-Inverse DWT co	mput	ation by	y filter	banks. Intr	oduction t	o multiway	elet
transforms.								
Unit V Wave	elet Packet Analysis and Applications							9
Haar wavelet pa	ackets - application -best basis selection	n and	l cost fi	unction	s. Sub-ban	d coding c	of images-Ir	nage
compression-Im	age de-noising - image coding using	g wa	velet tr	ree cod	er – EZW	code an	d SPIHT o	code
ntroduction to s	second generation wavelets.							
REFERENCE(8).	-						
	A Tour on Wavelet Signal Processing,	Floor	ior No	w Dalh	Decemb	2005		_
					2	2005		
	and Bopardikar. A.S, Wavelet Transfo					Draatian 1	Drantica II-	11 -
1	P. and Ramachandran K.I. Insight in v Delhi, 2010.	to Wa	avelets-	r rom	neory to	Practice, I	Tentice Ha	11 0
4 Strang G	and Nauven T. Wavelets and Filter Bar	ke V	Vellecle	v Caml	oridge Pres	s 2006		

4. Strang G and Nguyen T., Wavelets and Filter Banks, Wellesley Cambridge Press, 2006

5. Vetterli M, and Kovacevic J., Wavelets and Sub- band Coding, Prentice Hall, 2015

P.Io-

Chairman - BoS Dept.of ECE - ESEC

