A Low Power Structure Design of 2D-LFSR and Encoding Technique for BIST

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Abstract

BIST is a design technique that allows a circuit to test itself. The technique can provide shorter test time compared to an externally applied test and allows the use of low-cost test equipment during all stages of production. Due to the randomness properties of Linear Feedback Shift Registers (LFSRs), this requires very little hardware overhead. In this paper, structure design and optimization of a Built-In Self-Test (BIST) design based on two-dimensional (2-D) Linear Feedback Shift Registers (LFSRs) are described. The 2-D LFSRs can generate both precomputed test patterns (for detecting random-pattern-resistant faults) and random patterns (for detecting random-pattern-detectable faults) and have the advantages of high fault coverage and at-speed testing. The configurable 2-D LFSR test generator can be adopted in two basic BIST execution options: test-per-clock (parallel BIST) and test-per-scan (serial BIST). Generally, a circuit or system consumes more power in test mode than in normal mode. This extra power consumption can give rise to severe hazards in circuit. For LFSR-Reseeding Scheme takes advantage of the fact that the number of transitions in a test cube is always less than the number of blocks that do not contain transitions, the logic value fed into the scan chain is simply held constant. This approach reduces the number of transitions in the scan chains and thus minimizing power consumption.

Key Words: Built-In Self-Test (BIST), Linear Feedback Shift Registers (LFSRs), Design For-Testability (DFT), LFSR reseeding, Two-Dimensional (2-D) Linear Feedback Shift Registers (LFSRs)

1. INTRODUCTION

The increasing demands for high-density and high performance integrated circuits dictate the Built-In Self Test (BIST) schemes to guarantee high fault coverage, which is expected to be produced by a simple test-pattern generator in an acceptable number of vectors. The BIST involves performing the test-vector generation and the output-response analysis on a chip through the built-in hardware. BIST is a powerful Design For-Testability (DFT) technique for addressing highly complex Very-Large-Scale Integration (VLSI) testing problems. BIST designs include on-chip circuitry to provide test patterns and analyze output responses.

Performing tests on the chip greatly reduces the need for complex external equipment. The main motivation for considering power consumption during testing is generally, a circuit consumes much more power in test mode than in normal mode. BIST techniques are mainly employed to improve the circuit's fault coverage, test application time, and test development efforts.

The test generation techniques in the BIST include pseudorandom testing [7], pseudo exhaustive testing, weighted random testing using Linear Feedback Shift Registers (LFSRs) and reseeding of the LFSRs [8]. The problem with these techniques is generally do not provide a high enough fault coverage due to the presence of random-pattern resistant faults. The test-point insertion requires an extensive modification of the circuit and degrades circuit performance. Improving the fault coverage by adding logic to embedded a set of precomputed test patterns to detect the random pattern-resistant faults within a short time. These patterns are obtained by automatic test-pattern-generation tools and can be stored in a Read Only Memory (ROM) or generated through software. In pseudo-random testing, the fault coverage is limited by the presence of random pattern resistant (RP-resistant) faults.

Weighted pattern generation inserts a combinational circuit between the output of the Pseudo-Random Pattern Generator (PRPG) and the Circuit Under Test (CUT) to increase the frequency of occurrence of one logic value while decreasing the other logic value. This approach may increase the probability of detecting those faults that are difficult to detect using the typical LFSR pattern generation technique. Although weighted pattern generation is simple in design, achieving adequate fault coverage for a BIST circuit remains a problem [11].

Test point insertion adds control points and observation points for providing additional controllability and observability to improve the detection probability of random pattern-resistant faults. A control point can be connected to a primary input, an existing scan cell output, or a dedicated scan cell output. An observation point can be connected to a primary output through an additional multiplexer, an existing scan cell input, or a dedicated scan cell input. Because test points add area and performance overhead, an important issue for test point insertion is where to place the test points in the circuit to maximize the coverage and minimize the number of test points required. Once the test points have been inserted, the logic that drives the control points must be designed. When a control point is activated, it forces the logic value at a particular node in the circuit to a fixed value. During normal operation, all control points must be deactivated. During testing, there are different strategies as to when and how the control points are activated. One approach is random activation, where the control points are driven by the pseudo-random pattern generator. The drawback of this approach is that when a large number of control points are inserted, they can interfere with each other and may not improve the fault coverage as much as desired. An alternative to random activation is to use deterministic activation. A major drawback of test point insertion is that it requires modifying the circuit under test. In some cases this is not possible or not desirable [11].

Mixed-mode BIST involves supplementing the pseudorandom patterns with some deterministic patterns that detect random pattern-resistant faults and are generated using on-chip hardware. Pseudorandom patterns are generated to detect the random pattern-testable faults, and then some additional deterministic patterns are generated to detect the random pattern-resistant faults. There are a number of ways for generating deterministic patterns on-chip [11]. The simplest approach for generating deterministic patterns on-chip is to store them in a read-only-memory (ROM). The problem with this approach is that the size of the required ROM is often prohibitive [11]. Instead of storing the test patterns themselves in a

ROM, techniques have been developed for storing LFSR seeds that can be used to generate the test patterns. The LFSR that is used for generating the pseudo-random patterns is also used for generating the deterministic patterns by reseeding it with computed seeds. One problem is that for an LFSR with a fixed characteristic (feedback) polynomial, it may not always be possible to find a seed that will efficiently generate the required deterministic test patterns [4]. A third approach for mixed-mode BIST is to embed the deterministic patterns in the pseudo-random sequence. Many of the pseudo-random patterns generated during pseudo-random testing do not detect any new faults, so some of those "useless" patterns can be transformed into deterministic patterns that detect random pattern-resistant faults [11].

Hybrid BIST involves combining BIST and external testing by supplementing the pseudo-random patterns with deterministic data from the tester to improve the fault coverage. The simplest approach is to perform top-up ATPG for the faults not detected by BIST. To obtain a set of deterministic test patterns that "top-up" the fault coverage to the desired level and then store those patterns directly on the tester. In a system-on-chip, test scheduling can be done to overlap the BIST run time with the transfer time for loading the deterministic patterns from the tester. Hybrid BIST schemes have been developed, which attempt to store the deterministic patterns on the tester in a compressed form and then make use of the existing BIST hardware to decompress them[3].

2. OVERALL BLOCK DIAGRAM

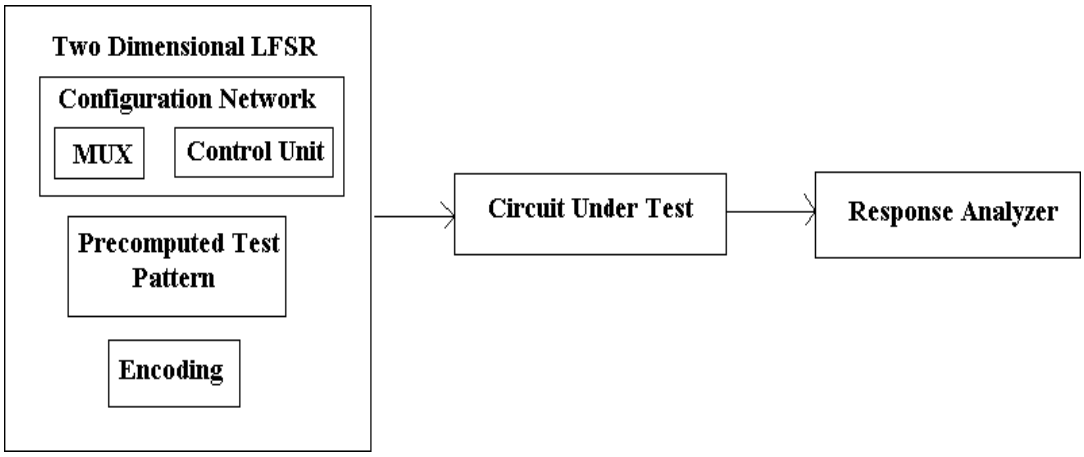

Figure1. Overall block diagram

1.1 Two-Dimensional (2-D) Linear Feedback Shift Registers (LFSRS)

A 2-D LFSR-based test pattern generator is proposed to generate an embedded deterministic sequence of test patterns followed by pseudorandom patterns. The generator mainly consists of four types of function blocks:

- Flip-Flop Array (FFA)
- Configuration Networks (CN)
- Multiplexers (MUXs)
- Control Unit (CU)

2.2 Circuit Under Test (CUT)

Circuit under test is the circuit which is to be tested to find the faults present in that circuit. Controllability, observability and predictability are the three most important factors that determine the complexity of driving a test for a circuit. A circuit under test fails when its observed behavior is different from its expectated behavior.

2.3 Output Response Analyzer (ORA)

The Output Response Analyzer (ORA) compacts the output responses of the CUT to the many test patterns produced by the TPG into a single Pass/Fail indication. The output response analyzer is sometimes referred to as an Output Data Compaction (ODC) circuit. The significance of the output response analyzer is that there is no need to compare every output response from the circuit under test with the expected output response external to the device. Only the final Pass/Fail indication needs to be checked at the end of the BIST sequence in order to determine the fault- free/faulty status of the CUT.

3. Two-dimensional (2-d) linear feedback shift registers (LFSRs)

1.2 Conventional LFSRs

An LFSR is a shift register that, when clocked, advances the signal through the register from one bit to the next most-significant bit. Some of the outputs are combined in exclusive-OR configuration to form a feedback mechanism. A linear feedback shift register can be formed by performing exclusive-OR on the outputs of two or more of the flip-flops together and feeding those outputs back into the input of one of the flip-flops [9].

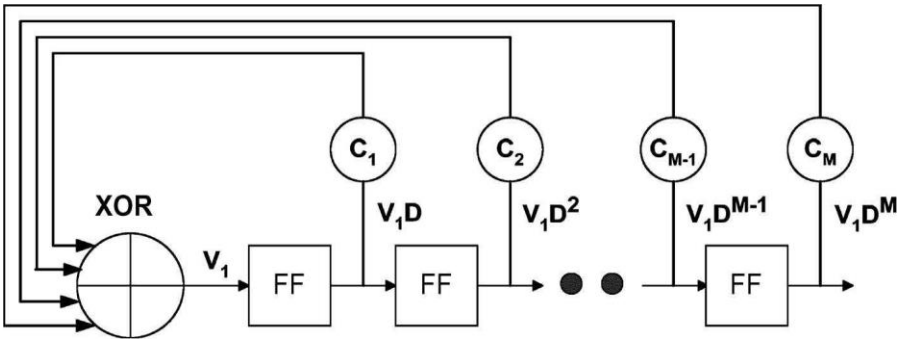

Figure 2. Conventional LFSRs

The output *V*1 of LFSRs is governed by the following Boolean equation:

$$V_1 = C_1 V_1 D^1 + C_2 V_1 D^2 + \cdots + C_M V_1 D^M \qquad (1)$$

Where, $V_1 D^i$, i = 1, . . . , M is the i^{th} delay of FF,

Ci, i = 1, . . . , M represents whether the $V_1 D^i$ is connected to the XOR gate or not.

Linear feedback shift registers make extremely good pseudorandom pattern generators. When the outputs of the flip-flops are loaded with a seed value (anything except all 0s, which would cause the LFSR to produce all 0 patterns) and when the LFSR is clocked, it will generate a pseudorandom pattern of 1's and 0's. LFSR output streams are deterministic. The output stream is reversible; an LFSR with mirrored tap sequence will cycle through the states in reverse order. However, an LFSR with a well-chosen feedback function can produce a sequence of bits which appears random and which has a very long cycle.

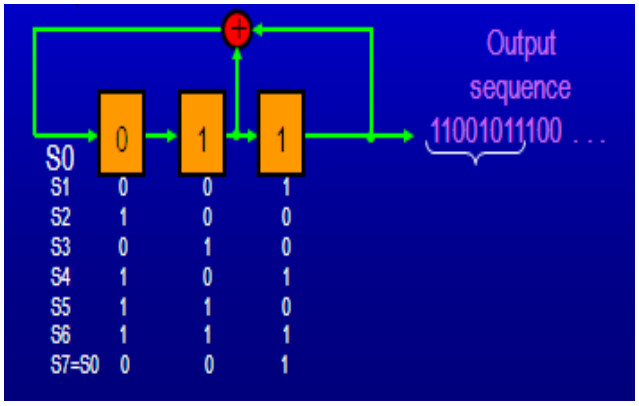

Figure 3. LFSR Example

1.3 Precomputed test pattern generation

For BIST in general, test patterns are generated on-chip by a TPG and the responses of the CUT are compressed and analyzed by an on chip signature analyzer. There are generally three strategies of test:

(1) Exhaustive Test
(2) Deterministic Test
(3) Pseudorandom Test

Steps to generate precomputed test pattern:-

1) Set F to be the set of all target faults (a set of detectable faults). Set K equal to the number of primary inputs.
2) If F is empty, stop.
3) Generate N random patterns by fixing the inputs that have a weight 0 (1), and randomly specifying the other inputs (N is a predetermined constant).
4) For each random pattern generated, perform fault simulation for every fault f.
5) If f is detected, remove f from F.
6) If no fault was detected by the previously applied N tests, set K = K - 1.
7) Go to Step (2).

1.4 Configurable 2-D LFSRs

A 2-D LFSR-based test pattern generator is proposed to generate an embedded deterministic sequence of test patterns followed by pseudorandom patterns. The generator mainly consists of four types of function blocks: - the Flip-Flop Array (FFA), the Configuration Networks (CN), the Multiplexers (MUXs), and the Control Unit (CU). The

FFA is an N*M flip-flop array, where is the N number of inputs of a circuit under test (CUT) and M is the number of stages of the 2-D LFSR. To reduce the hardware, M is usually a small number. Each CN consists of XOR gates and an inverter if necessary. The MUX selects one of the configuration networks to feed the feedback signals to the FFA. The MUX is controlled by the CU. When resetting the generator, the initial states of FFA are set to alternating 1 and 0, in each column of the FFA [9].

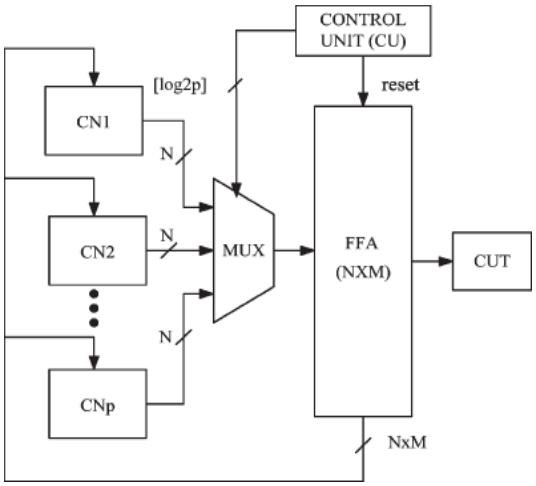

Figure 4. Configurable 2-D LFSRs

This configurable 2-D LFSR test generator generates the following:

1) A sequence of deterministic test patterns to detect random-pattern-resistant faults and
2) A sequence of random test patterns to detect random-pattern detectable faults

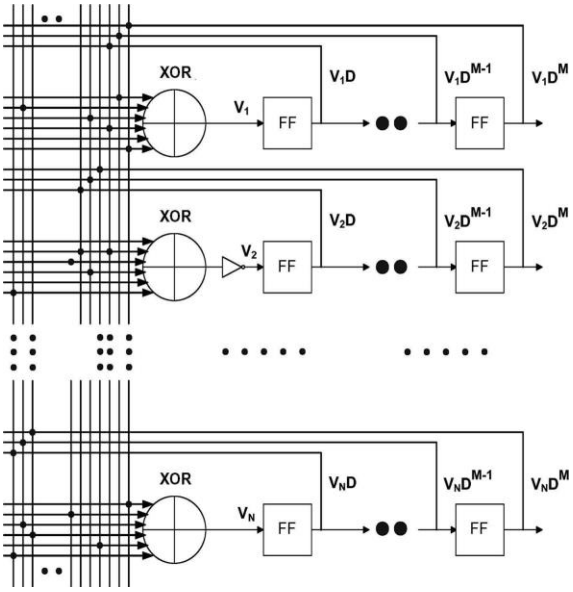

Figure 5. Structure of 2-D LFSRs

The resulting 2-D LFSR-based multi sequence test generator is able to generate a given test-vector set at significantly lower hardware compared with a previous work while retaining high fault coverage.The configurable 2-D LFSR test generator can be adopted in two basic BIST execution options:

1. Test-Per-Clock (parallel BIST)
2. Test-Per-Scan (serial BIST)

1.5 Test-per-clock (parallel BIST)

In test-per-clock BIST, test patterns are applied to the circuit under test (CUT) by the test generator. The response analyzer captures the responses every clock cycle. The scheme can execute tests much faster than the test-per-scan BIST scheme but at an expense of more hardware overhead [2].

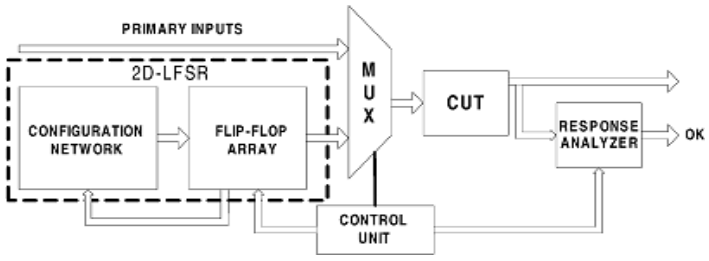

Figure 6. Test-per-clock BIST

1.6 Test-per-scan (serial BIST)

In test-per-scan BIST, test patterns are shifted into a serial scan path or multiple scan paths to test the CUT. The test responses are subsequently captured by the scan flip-flops and shifted out to the response analyzer while new patterns are being shifted in. The hardware overhead is low in test-per-scan BIST [2].

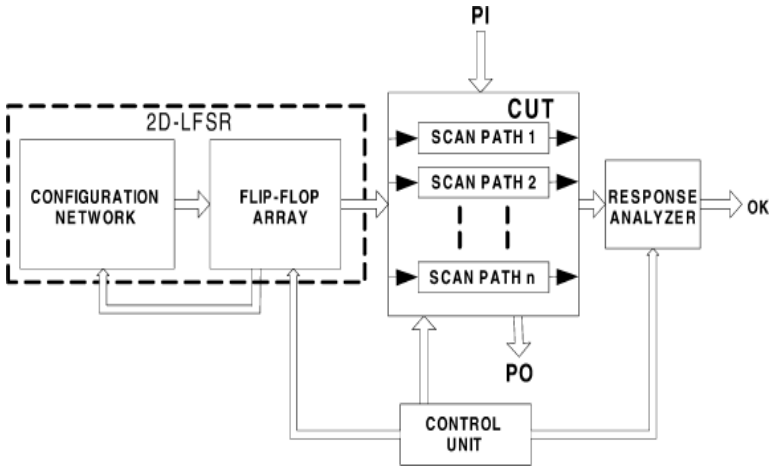

Figure 7. Test-per-scan BIST

In test-per-clock BIST, the area overhead is increased based on the precomputed test patterns. In test-per-scan BIST, test patterns are shifted into a serial scan path to test the CUT. The memory transition is high in test-per-scan BIST compared to test-per-clock BIST. LFSR reseeding encoding technique is used in test-per-scan BIST to reduce the memory transition and power consumption [3].

4. LFSR-Reseeding Scheme

Power dissipation during test is a significant problem as the size and complexity of systems-on-chip (SOCs) continue to grow. A new test-data-compression scheme based on linear feedback shift registers (LFSR) reseeding that significantly reduces power consumption during test. The basic idea in LFSR reseeding is to generate deterministic test cubes by expanding seeds. A seed is an initial state of the LFSR that is expanded by running the LFSR. The proposed encoding scheme encodes each test cube with two kinds of data: "hold flags" and "data bits." Each test cube is divided into several blocks, and each block has a 1-bit hold flag. The hold flag indicates whether a transition occurs in a block [3].

There are three types of blocks.

1) Transition block (hold flag = 0). One or more transitions exist in the block. Either both 0 and 1are present in the block (e.g., XX1X0X) or only 0 or 1 is present, but the last specified bit from a previous block was the opposite value.

2) Non transition block (hold flag = 1). No transition occurs in the current block. Only 0 or 1 is present in the block, and the last specified bit from a previous block is same (e.g., X0XX0X).

3) Don't care block (hold flag = X). No specified bits occur in the block; all are don't cares.

Block	Block1	Block2	Block3	Block4
Original	0 X X 1	X 1 1 1	1 X 1 X	X X X X
Encoded	0 0 X X 1	1 - - - -	1 - - - -	X X X X X

Figure 8. Example of encoding test data.

The original test cube contains seven specified bits. The encoded data only has three specified hold flags and two specified data bits, giving a total of only five specified bits. The proposed encoding scheme reduces the number of specified bits that need to be generated using LFSR reseeding. The proposed encoding scheme provides to reduce the test power for LFSR reseeding. LFSR reseeding is a powerful approach for reducing test storage. The proposed encoding scheme provides a way to reduce the test power for LFSR reseeding while still preserving or even improving the compression that is achieved. The block size can be easily adjusted to tradeoff test-power reduction versus hardware overhead.

5. RESULTS AND DISCUSSIONS

The 2-D LFSR fault coverage output was shown in fig .9. Based on the selection line 2D LFSR can generate both precomputed test patterns (for detecting random-pattern-resistant faults) and random patterns (for detecting random-pattern-detectable faults) and have the advantages of high fault coverage.

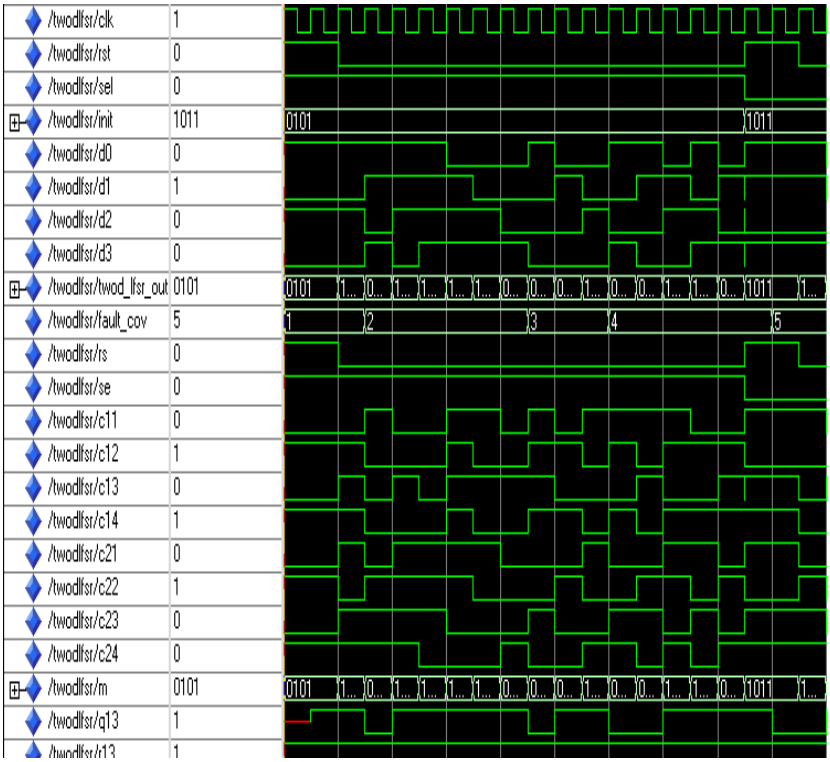

Figure 9. Simulation result for fault coverage

Table 1. Comparison Table for Fault Coverage

S.No	Benchmark Circuit	Fault Coverage For Normal LFSR	Fault Coverage For 2D-LFSR
1	S27	67%	83%

The configurable 2-D LFSR test generator can be adopted in two basic BIST execution options: test-per-clock (parallel BIST) and test-per-scan (serial BIST). Serial BIST simulation result was shown in fig.10.

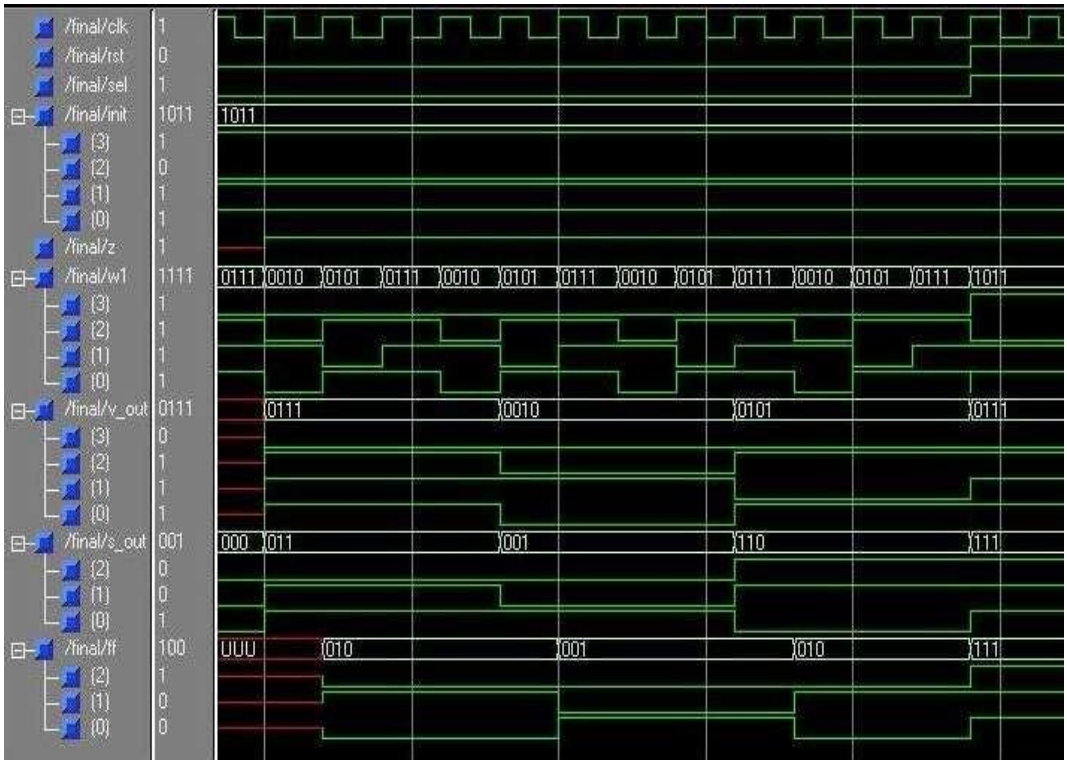

Figure 10. Simulation result for serial BIST

The memory transition is high in test-per-scan BIST compared to test-per-clock BIST. LFSR reseeding encoding technique is used in test-per-scan BIST to reduce the memory transition and power consumption. Power output without encoding algorithm was shown in table .2. The memory transition was reduced and power also reduced by using LFSR reseeding encoding algorithm shown in table .3.

Table 2. Power Consumption without Encoding Algorithm

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		52
Vccint 2.50V:	18	46
Vcco33 3.30V:	2	7
Clocks:	15	38
Inputs:	2	5
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 2.50V:	1	3
Quiescent Vcco33 3.30V:	2	7

Table 3. Power Consumption with Encoding Algorithm

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		43

Vccint 2.50V:	15	37
Vcco33 3.30V:	2	7

Clocks:	12	29
Inputs:	2	5
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0

Quiescent Vccint 2.50V:	1	3
Quiescent Vcco33 3.30V:	2	7

Comparison Table for Power Consumption with and without encoding algorithm was shown in table .4. From the comparison table the percentage improvement of power consumption is 17%.

Table 4. Comparison Table for Power Consumption

S. No	Benchmark Circuit	Power Consumption Without Encoding Algorithm	Power Consumption With Encoding Algorithm
1	S27	52mW	43mW

Percentage Improvement=17%

6. CONCLUSION

A new approach to optimize configurable 2-D LFSR for generating both embedded and random test pattern in BIST has been proposed. This configurable 2-D LFSR-based test pattern generator generates: 1) a deterministic sequence of test patterns for random-pattern-resistant faults 2) random test patterns for random-pattern-detectable faults. The configurable 2-D LFSR test generator can be adopted in two basic BIST execution options: test-per-clock (Parallel BIST) and test-per-scan (serial BIST). The proposed 2-D LFSR structure will be implemented in SPARTAN-3E FPGA by using VHDL. By comparing normal LFSR and 2D-LFSR, the percentage improvement for fault coverage is 16%. The memory transition is high in test-per-scan BIST compared to test-per-clock BIST. LFSR reseeding encoding technique is used in test-per-scan BIST to reduce the memory transition and power consumption. This approach reduces the number of transitions in the scan chains and thus minimizing power consumption. By using encoding algorithm, the percentage improvement for power consumption is 17%.

REFERENCES

[1] Xinhui zhang, Chienhenry chen and aravindkumar chakravarthy, "Structure Design and Optimization of 2-D LFSR-Based Multisequence Test Generator in Built-In Self-Test", IEEE transactions on Instrumentation and Measurement, vol.57, no.3, March 2008.
[2] C.I.H. Chen and K. George, "Configurable two-dimensional linear feedback shifter registers for parallel and serial built-in self-test," IEEE transactions on Instrumentation and Measurement, vol. 53, no. 4, pp. 1005–1014, Aug. 2004.
[3] Jinkyu Lee and Nur A. Touba, "LFSR-Reseeding Scheme Achieving Low-Power Dissipation During Test" , IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 26, no. 2, February 2007.
[4] Dimitri Kagaris, Spyros Tragoudas, Amitava Majumdar, "Test-set partitioning for multi- weighted random LFSRs", Integration, the VLSI journal, 1999.
[5] Gert Jervan ,Elmet Orasson, Helena Kruus, Raimund Ubar, "Hybrid BIST optimization using reseeding and test set compaction", Journal of Microprocessors and Microsystems,2008.
[6] Patrick Girard, "Survey of Low-Power Testing of VLSI Circuits", Journal on IEEE Design & Test of Computers, 2002.
[7] P.Rosinger, B.M.Al Hashini & N.Nicolici,"Dual multiple-polynomial LFSR for low-power mixed-mode BIST",IEEE proc., on computer digital techniques, vol.150, No.4.,2003.
[8] Nur A. Touba and Edward J. Mccluskey, "Altering a pseudo-random bit sequence for scan-based BIST", IEEE International Test Conference, 1996.
[9] Xiaodong Zhang and Kaushik Roy, "Design and Synthesis of Low Power Weighted Random Pattern Generator Considering Peak Power Reduction", Journal of Electronic Testing, 2001.
[10] Zhanglei Wang, Krishnendu Chakrabarty and Michael Bienek, "A Seed-Selection Method To Increase Defect Coverage For LFSR-Reseeding-Based Test Compression", 12th IEEE European Test Symposium, 2007.
[11] Laung-Terng Wang, Cheng-Wen Wu, "VLSI Test Principles and Architectures", 2008.