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Selection Of Multilevel Inverter For Photovoltaic Application

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Abstract

To utilize renewable energy resources for supplying electrical load, power converters play a vital role. In photovoltaic system, inverter is essential for connecting generated DC power to the grid. Due to the need of high quality electricity with low harmonic content in output of inverter and also necessity of cost reduction, we have to reduce the filter size. By using different Pulse Width Modulation (PWM) techniques harmonic content in inverter output parameters and filter requirement gets reduced. Different Carrier based PWM techniques (PSPWM,LSPWM) are employed to Cascaded-H-Bridge(CHB) inverter and Diode Clamped Inverter (DCI) and at different modulation indices harmonics in the inverter output are simulated and compared with different modulation techniques.

Keywords - PWM, *PSPWM, LSPWM, SVPWM, CHB, DCI.*

1. INTRODUCTION

The solar inverter is a critical component in a solar energy system. It performs the conversion of the variable DC output of the Photovoltaic (PV) module(s) into a clean sinusoidal 50 Hz AC current that is then applied directly to the commercial electrical grid or to a local, off-grid electrical network (Jeyraj Selvaraj et al, 2009). The heart of the inverter is a real-time microcontroller. The controller executes the very precise algorithms required to invert the DC voltage generated by the solar module into AC. This controller is programmed to perform the control loops necessary for all the power management functions necessary including DC/DC and DC/AC (Yuncong Jiang et al, 2012). The controller also maximizes the power output from the PV through complex algorithms called maximum power point tracking (MPPT(Yuncong

Jiang et al, 2012). The PV maximum output power is dependent on the operating conditions and varies from moment to moment due to temperature, shading, soilage, cloud cover, and time of day so tracking and adjusting for this maximum power point is a continuous process.

This paper discuss about various inverter toplogies adoptable for solar PV and different modulation tecniques are discussed. Simulation and analysis are carrier out for Cascaded H-Bridge(CHB) multilevel inverter and Diode Clamped Inverter(DCI) with Phase Shifted Pulse Width Modulation(PSPWM) and Level Shifted Pulse Width Modulation (LSPWM) for various modulation indices and their harmonic spectrums are analysed. Finally better inverter for solar PV is selected (Rodriguez J et al, 2002).

Some of the benefits of Multilevel Inverter

Reduced dv/dt rating, decrease voltage stress of switch.
Series connection of switches for high voltage applications are reduced or neglected which reduce complexity of circuit.
As the level increases, output voltage resembles with sinusoidal voltage and so reduction in harmonic content.
Reduced ElectroMagnetic Interference (EMI) problems.

Some of popular MLI topologies are listed below

Diode-Clamped Inverter (DCI)
Flying Capacitor Inverter (FC)
Cascaded H-Bridge Inverter (CHB)

1.1. *Diode Clamped Inverter*

Number of active switches are 6(m-1), clamping diodes are 3(m-1)(m-2) and (m-1) dc link capacitors(m is number of level).Deviation of Neutral point is major problem in DCI which causes because of unbalanced voltage, unequivalent sharing of capacitor voltage due to manufacturers tolarence and dynamic switching of device. There is need of only one DC voltage bus. Nine-level DCI is simulated using different PWM techniques and their harmonics compared with CHB inverter(Naga haskar Reddy V et al, 2011) (Nabae A and Akagi H, 1981) (Pou J, et al, 2005) .

1.2. *Flying Capacitor Inverter*

Number of active switches are 6(m-1), clamping diodes are 3(m-1)(m-2), (m-1) dc link capacitors and 3(m-1)(m-2)/2 auxillary capacitors.Since it has large number of capacitors, there is more possible condition of failure of inveter due to capacitor failure. So, it is not discussed here (Meynard T and Foch H, 1992) (Kang D.W et al , 2005) (Lin B.R and Huang C.H, 2006).

1.3. Cascaded H-Bridge *Inverter*

Consists of number of H-bridges connected in series. H number of H-bridges cascaded to form 2H+1 level of inverter. It need seperate DC bus for each H-bridge

and number of switches (MOSFET/IGBT) per phase of m-level inverter is given as 2(m-1) and number of antiparallel diode also 2(m-1)) (Kou X, et al, 2006) (Azli N. A, and Choong Y. C, 2006).

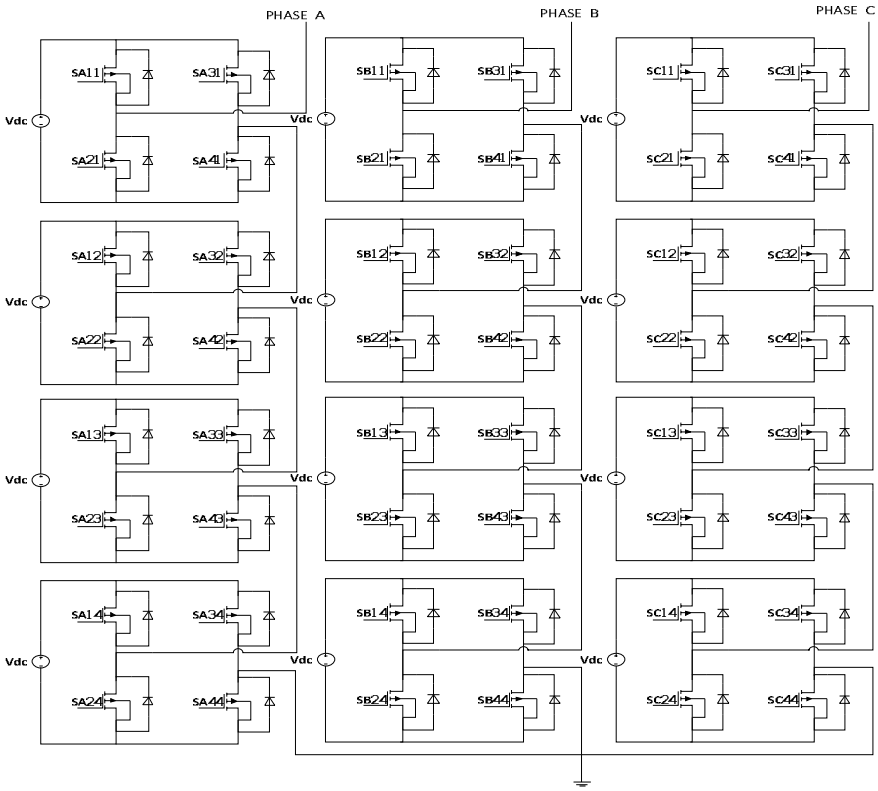

Fig .1. Circuit diagram of nine-level CHB inverter

Fig.1 shows the power circuit of nine-level CHB inverter with three-phase RLC load.V_{dc} are input dc bus voltage, which are supplied by PV array.

Switching states of nine-level CHB inverter is given in table.1. There is redundancy of switching state (to get same level of voltage, different switching are possible) which is an advantage of MLI which allows the flexiblity in switching. The above mentioned switching states and corresponding voltage levels are acheived by different types of carrier based pulse width modulation techniques which are discussed in chapter 2.

Table .1. Switching states

PHASE VOLTAGE V_{AN}	Switching states							
	S11	S31	S12	S32	S13	S33	S14	S34
0	1	1	1	1	1	1	1	1
4Vdc	1	0	1	0	1	0	1	0
-4Vdc	0	1	0	1	0	1	0	1
3Vdc	1	1	1	0	1	0	1	0
	1	0	1	1	1	0	1	0
	1	0	1	0	1	1	1	0
	1	0	1	0	1	0	1	1
-3Vdc	1	1	0	1	0	1	0	1
	0	1	1	1	0	1	0	1
	0	1	0	1	1	1	0	1
	0	1	0	1	0	1	1	1
2Vdc	1	1	1	1	1	0	1	0
	1	1	1	0	1	1	1	0
	1	1	1	0	1	0	1	1
	1	0	1	1	1	1	1	0
	1	0	1	1	1	0	1	1
	1	0	1	0	1	1	1	1
-2Vdc	1	1	1	1	0	1	0	1
	1	1	0	1	1	1	0	1
	1	1	0	1	0	1	1	1
	0	1	1	1	1	0	1	1
	0	1	1	1	1	1	1	0
	0	1	0	1	1	1	1	1
Vdc	1	0	1	1	1	1	1	1
	1	1	1	0	1	1	1	1
	1	1	1	1	1	0	1	1
	1	1	1	1	1	1	1	0
-Vdc	0	1	1	1	1	1	1	1
	1	1	0	1	1	1	1	1
	1	1	1	1	0	1	1	1
	1	1	1	1	1	1	0	1

2. PROPOSED SWITCHING METHODS FOR MULTILEVEL INVERTERS

There are two types of multiple carrier PWM techniques which has multiple carriers compared with reference signal to generate pulse for switch. Both the types are explained in following section (Kanchan R. S, et al, 2008).

2.1 Phase Shifted (PS) PWM

Number of carrier signals required for m level CHB inverter with PSPWM is given by (m-1) which are all equal in magnitude and having same frequency and they are in phase shift of φ, which is given as

$$\varphi = 360^{\circ} / (m-1) \tag{1}$$

Reference signal V_{ref} is compared with V_{cr1} and pulse is generated for S11 during $V_{ref} > V_{cr1}$, similarly V_{cr2}, V_{cr3} and V_{cr4} are used to generate pulse for S12, S31 and S41 respectively.

Likewise, V'_{cr1},V'_{cr2},V'_{cr3} and V'_{cr4} which are in 180° phase shift with V_{cr1},V_{cr2},V_{cr3} and V_{cr4} are used to generate pulse for S31, S32, S33 and S34 respectively when $V_{ref} < V'_{cr}$.

Frequency modulation index and Amplitude modulation index is given by $m_a = \hat{v}_{ref} / \hat{v}_{cr}$ and $m_f = f_{ref} / f_{cr}$ respectively.

Switching frequency of device is given by

$$f_{sw,dev} = m_f \times f_{cr} \tag{2}$$

Switching frequency of inverter is given by

$$f_{sw,inv} = (m-1) \times f_{sw,dev} \tag{3}$$

Total DC voltage is

$$E = \frac{m-1}{2} \times V_{dc} \tag{4}$$

Maximum DC voltage utilization is given by,

$$V_{AB1,max} = \sqrt{3} \times \frac{V_{pk}}{\sqrt{2}} \times E = 0.612(m-1)V_{dc} \text{ for } m_a=1 \tag{5}$$

For 9 level inverter,

The number of carriers signals are 8, and they are in phase shift of 45°.

Inverter phase voltage (V_{AN}) is given by,

$$V_{AN} = V_{H1} + V_{H2} + V_{H3} + V_{H4} \tag{6}$$

V_{H1}, V_{H2}, V_{H3} and V_{H4} are voltages across H-bridges 1, 2, 3 and 4 respectively.

Inverter phase voltage is obtained by 9 steps 0,V_{dc}, $2V_{dc}$,$3V_{dc}$,$4V_{dc}$,$-V_{dc}$,$-2V_{dc}$,$-3V_{dc}$ and $-4V_{dc}$. Comparision of carrier and reference for PSPWM techniques are shown in fig 2.

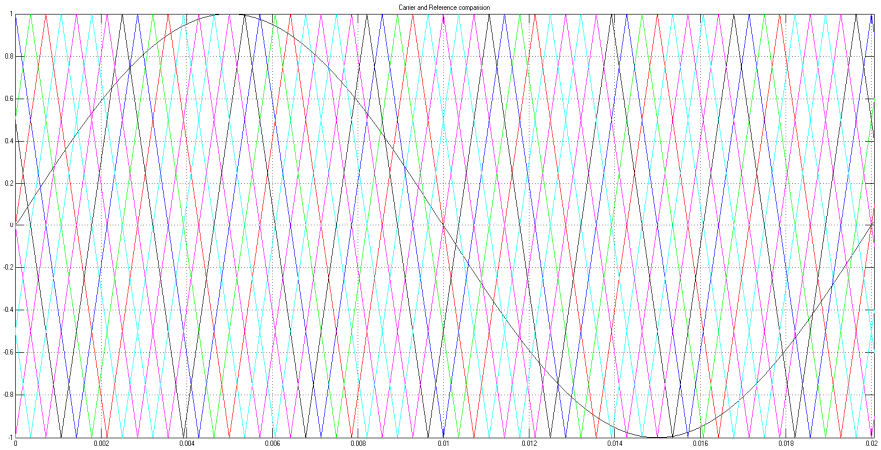

Fig .2. Comparison of carrier and reference for generating pulses using PSPWM

The corresponding generated pulses are shown in fig 3, which are simulated at f_{cr}=10050Hz and m_a=1.

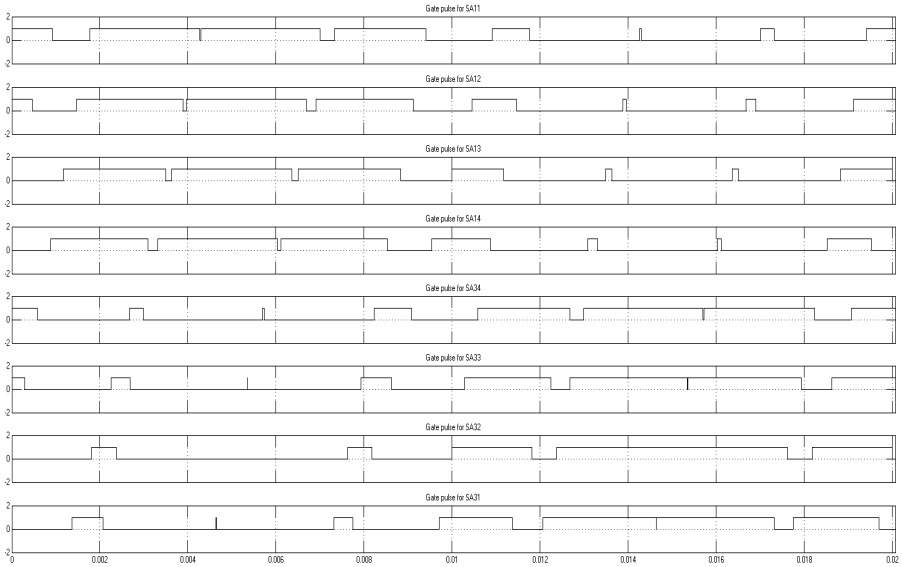

Fig .3. Pulses Generated using PSPWM

2.2 Level Shifted (LS) PWM

Number of carrier signals required for m level CHB inverter with LSPWM is given by (m-1) which are all equal in magnitude and having same frequency and they are vertically disposed. Reference signal V_{ref} is compared with V_{cr1} and pulse is generated

for S11 during $V_{ref} > V_{cr1}$, similarly V_{cr2}, V_{cr3} and V_{cr4} are used to generate pulse for S12, S31 and S41 respectively.

Likewise, V'_{cr1},V'_{cr2},V'_{cr3} and V'_{cr4} which are in 180° phase shift with V_{cr1},V_{cr2},V_{cr3} and V_{cr4} are used to generate pulse for S31, S32, S33 and S34 respectively when $V_{ref} < V'_{cr}$.(uppermost and lowermost carrier signals generate pulse for upper swithes of both leg of first H-bridge H1.)

Frequency modulation index and Amplitude modulation index is given by

$$m_a = \frac{\hat{v}_{ref}}{\hat{v}_{cr} \times (m-1)} \quad \text{for} \quad 0 < m_a \leq 1 \tag{7}$$

and $m_f = f_{ref} / f_{cr}$ respectively.

Switching frequency of device is given by

$$f_{sw,dev} = f_{cr} / (m-1) \tag{8}$$

Switching frequency of inverter is given by

$$f_{sw,inv} = f_{cr} \tag{9}$$

Total DC voltage is $$E = \frac{m-1}{2} \times V_{dc} \tag{10}$$

Maximum DC voltage utilization is given by,

$$V_{AB1,max} = \sqrt{3} \times \frac{V_{pk}}{\sqrt{2}} \times E = 0.612(m-1)V_{dc} \text{ for, } m_a=1 \tag{11}$$

There are three types of LSPWM.

i. In-Phase Disposition (IPD) PWM
   Where all carriers are in-phase with each other.
ii. Phase Opposite Disposition (POD) PWM
   Where all alternative carriers are oppositly disposed.
iii. Adjacent Phase Opposite Disposition (APOD) PWM

Where all carriers above zero reference line are in-phase with each other and carriers below zero reference line are in opposite with carriers above zero reference line. Comparision of carrier and reference for IPD-PWM, POD-PWM, APOD-PWM techniques are shown in figures 4, 5 and 6 respectively and the corresponding generated pulses are shown in figures7, 8 and 9 , which are simulated at f_{cr}=10050Hz and m_a=1.

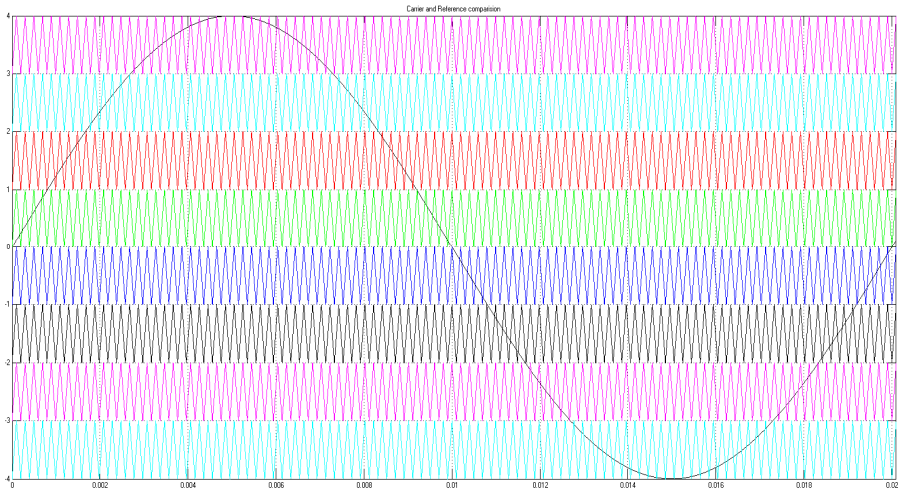

Fig .4. Comparison of carrier and reference for generating pulses using IPD technique.

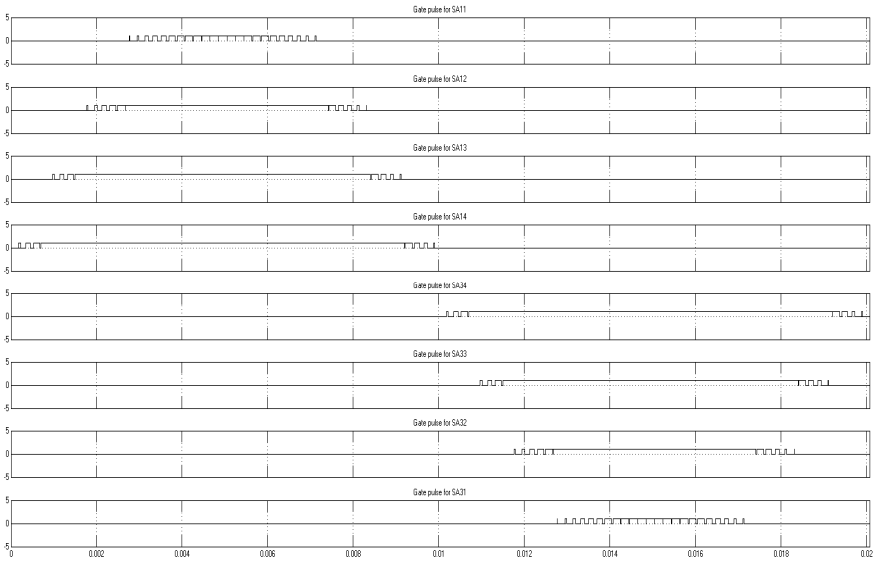

Fig .5. Pulses generated using IPD technique.

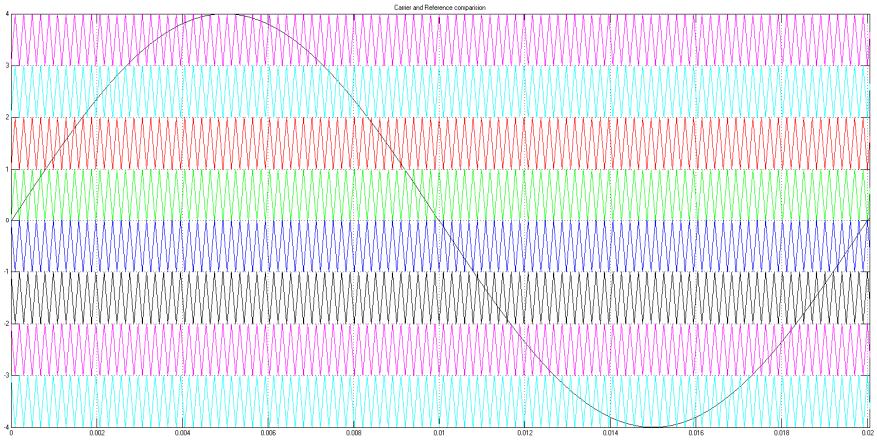

Fig. 6. Comparison of carrier and reference for generating pulses using POD technique.

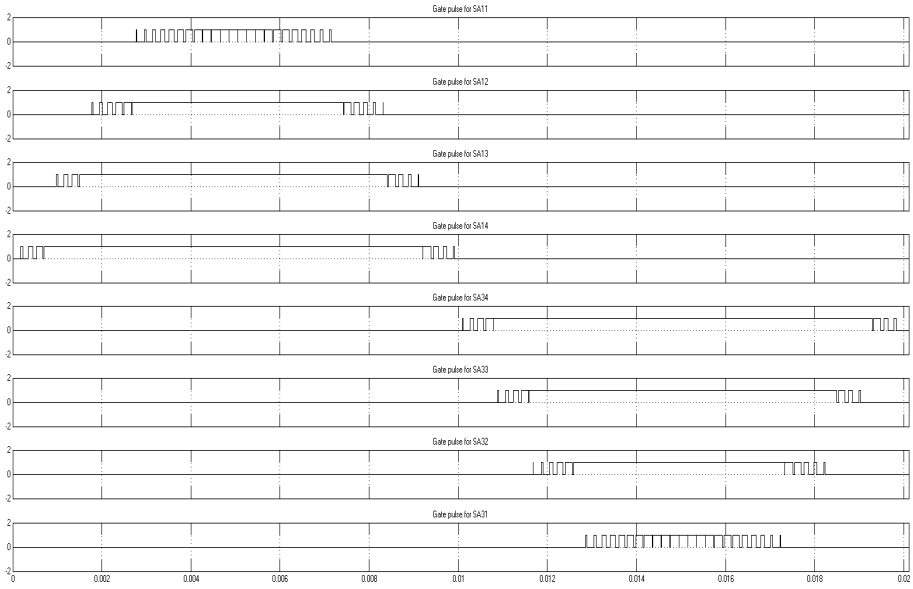

Fig .7. Pulses generated using POD technique.

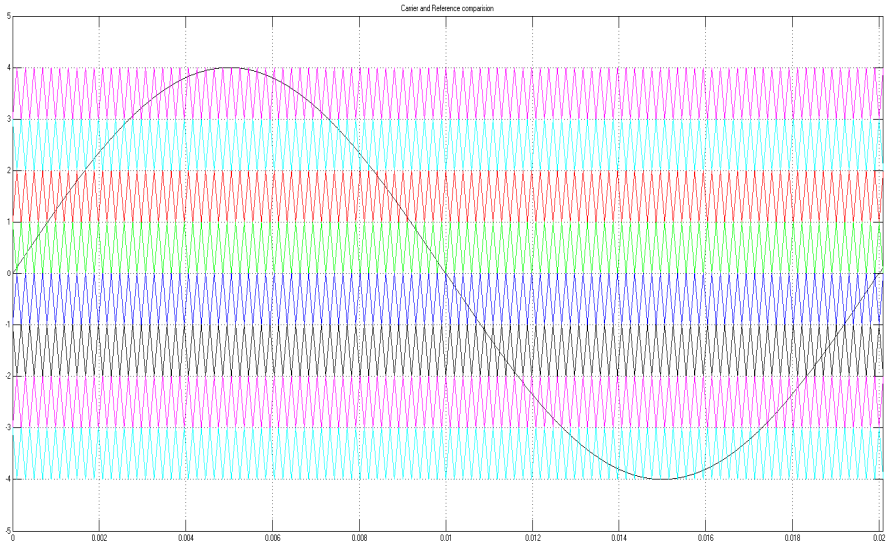

Fig .8. Comparison of carrier and reference for generating pulses using APOD technique.

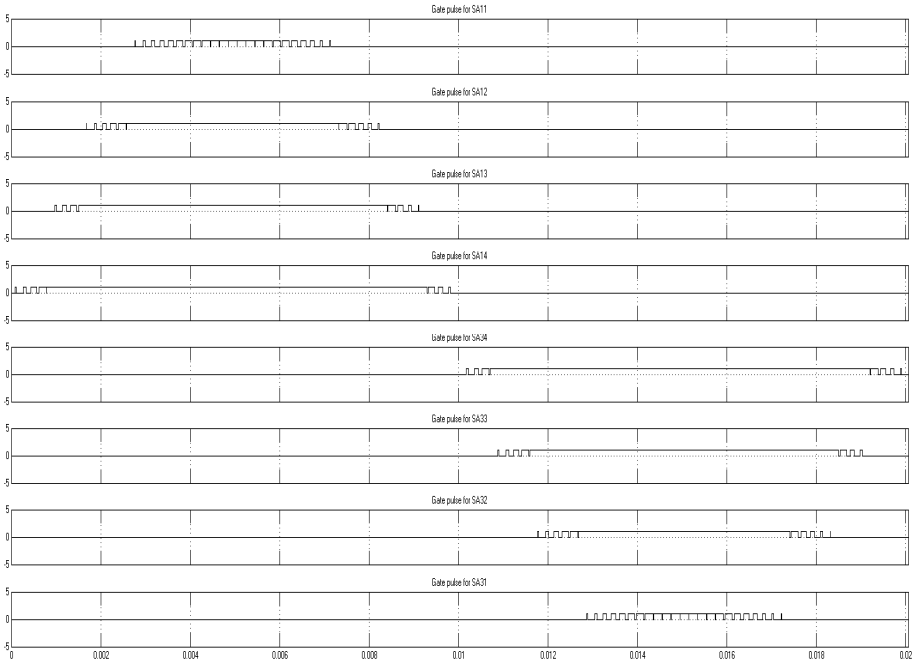

Fig .9. Pulses generated using APOD technique.

2.2 Space Vector Pulse Width Modulation (SVPWM)

In all the above mentioned modulation techniques, all the three phase reference signals are compared with carriers seperately but in SVPWM all three phase reference are composed into single vector and that vector is used to calculate ON time of each switches. So, during any change in reference signal, it affects ON time of all the switches which helps to maintain generated output voltage of inverter in balanced condition but in SPWM this condition leads to unbalanced voltage (Kanchan R. S, et al, 2008) (Celanovic N and Boroyevich D, 2008).

For generating SVPWM, following steps need to be carried out.

- abc to α-β transformation (3φ-2φ transformation)
- Calaculation of reference signal magnitude and angle.
- Sector identification
- Calculation of dwell times T0, T1 and T2.
- Calculation of Ta, Tb and Tc.
- Compare Ta, Tb and Tc with V_{cr} to generate pulse for switches.

Another important advantages of SVPWM is that DC utilization is higher than SPWM. So, for same rating of load it requires smaller voltage than SPWM.

Maximum DC voltage utilization is given by,

$$V_{LL,max} = \frac{\sqrt{3}}{\sqrt{2}} \times \frac{2}{3} \times V_{dc} \cos 30^{\circ} \times (m-1) = 0.707(m-1)V_{dc} \quad \text{for } m_a=1 \qquad (12)$$

Amplitude modulation index is given by,

$$m_a = \sqrt{3} \times \frac{\$_{ref}}{V_{dc}} \qquad \text{for } 0 < m_a \leq 1 \qquad (13)$$

Carrier and reference comparison and pulse generation of carrier based SVPWM technique are shown in fig. 10 and 11 respectively.

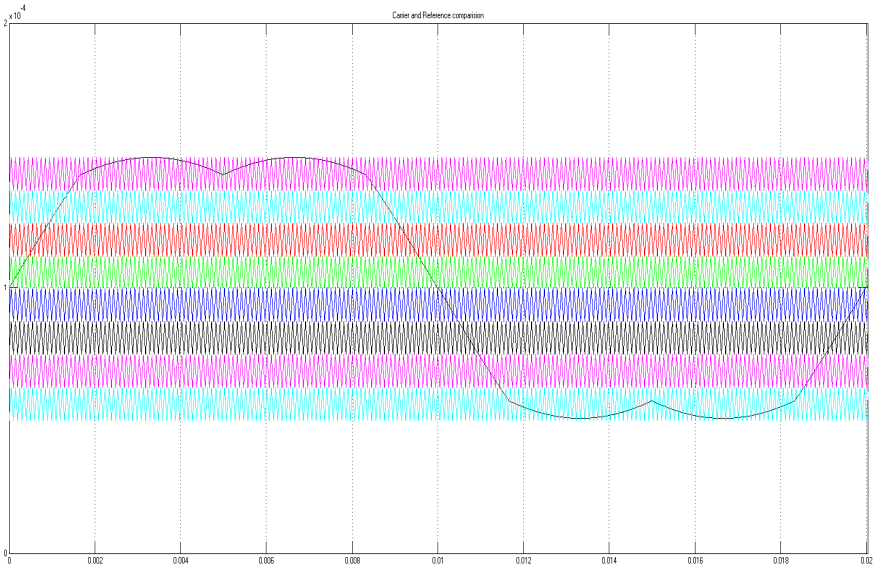

Fig .10. Comparison of carrier and reference for generating pulses using SVPWM technique.

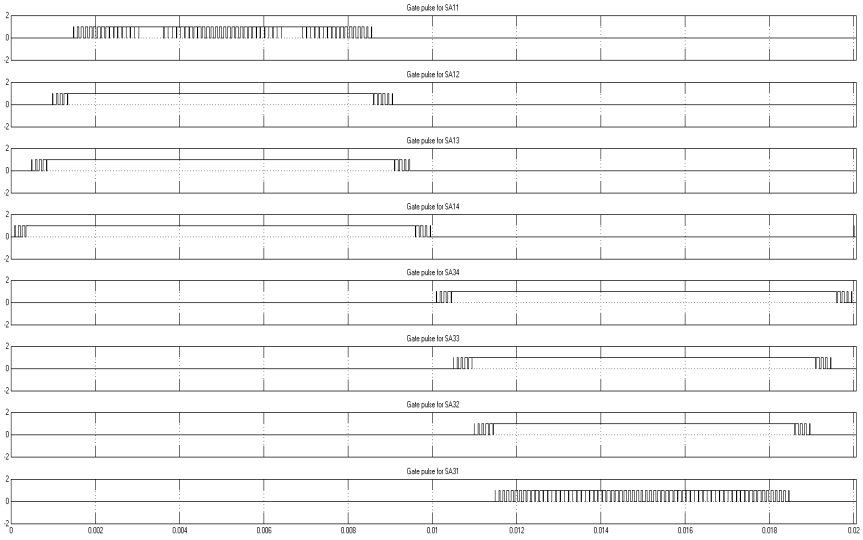

Fig .11. Pulses generated using SVPWM technique

3. ANALYSIS OF HARMONICS IN INVERTER OUTPUT PARAMETERS FOR CHB INVERTER AN DCI USING VARIOUS PWM TECHNIQUES

Nine level Cascaded H –bridge multilevel Inverter and Diode clamped multilevel inverter are simulated with different switching techniques. Harmonics for phase

voltage, Line voltage and Line current of two inverters are captured. Based on the harmonics for different pluses different graphs are obtained.

Fig.12 shows line voltage THD of CHB inverter using different modulation technique for modulation indices(m_a) 1,0.8,0.6 are represented as 1,2 and 3 respectively with f_s=10050Hz.As the m_a decreases, harmonic content increases in the output parameters. From below graph it is clear that SVPWM technique has lower harmonics compared all other technique for all values of m_a. Also SVPWM has harmonic frequency of order $pm_f \pm qf_{ref}$ with p and q as even(odd) and odd(even) integer. In the comparision graph Fig 12 , SVPWM tecchnique has lower harmonics compare to all other different switching pulses.

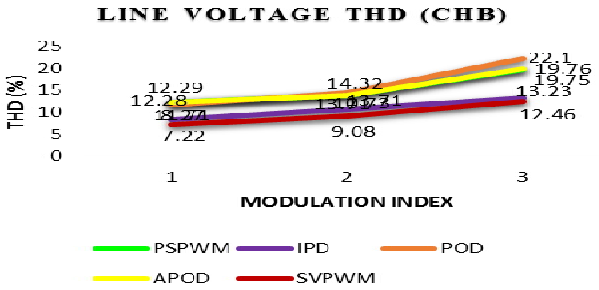

Figure.12. Comparison of line voltage THD for CHB inverter with f_{cr}=10050Hz for m_a=1,0.8,0.6.

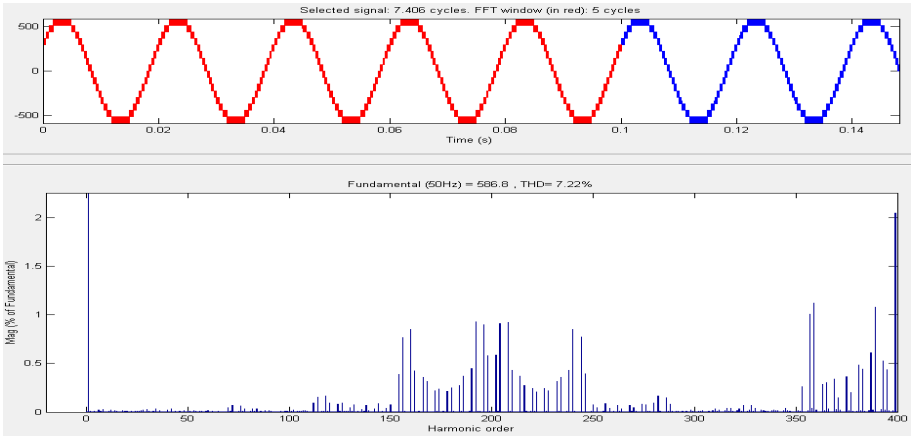

Figure .13. Harmonic spectrum of CHB line voltage using SVPWM

Harmonic spectrum of CHB inverter line voltage using SVPWM technique is shown in figure 13. Since harmonic contents are moved to high frequency, filter requirement get reduced which result in reduction in size and loss. Upto 150th order, harmonic content is very low and maximum cut-off frequency of output filter of

inverter is increased as 7500Hz. Peak line voltage of inverter is 586.8V (415V rms) with 74V individual dc bus for each H-bridge which are supplied by PV array.

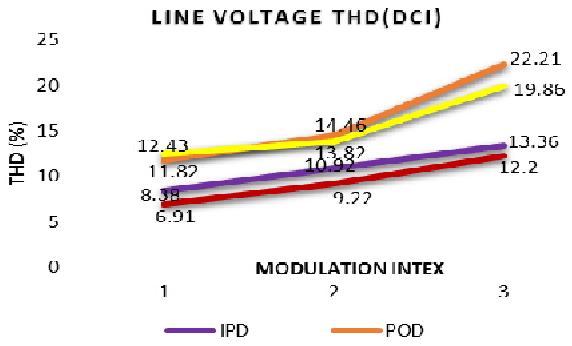

Fig .14. Comparison of line voltage THD for DCI with f_{cr}=10050Hz for m_a=1,0.8,0.6.

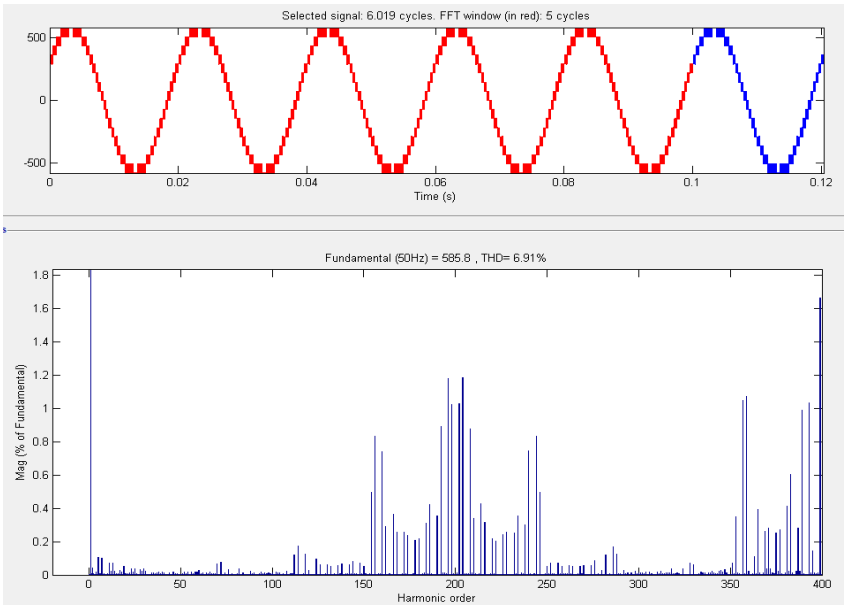

Fig .15. Harmonic spectrum of DCI line voltage using SVPWM

Line voltage harmonic content of DCI is shown in fig.14 and harmonic spectrum of DCI using SVPWM technique with m_a=1 is shown in fig.15. In the comparision graph Fig 14, SVPWM tecchnique has lower harmonics compare to all other different switching pulses.

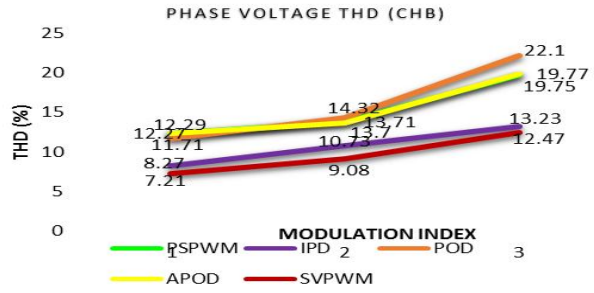

Fig .16. Comparison of phase voltage THD for CHB inverter with f_{cr}=10050Hz for m_a=1,0.8,0.6.

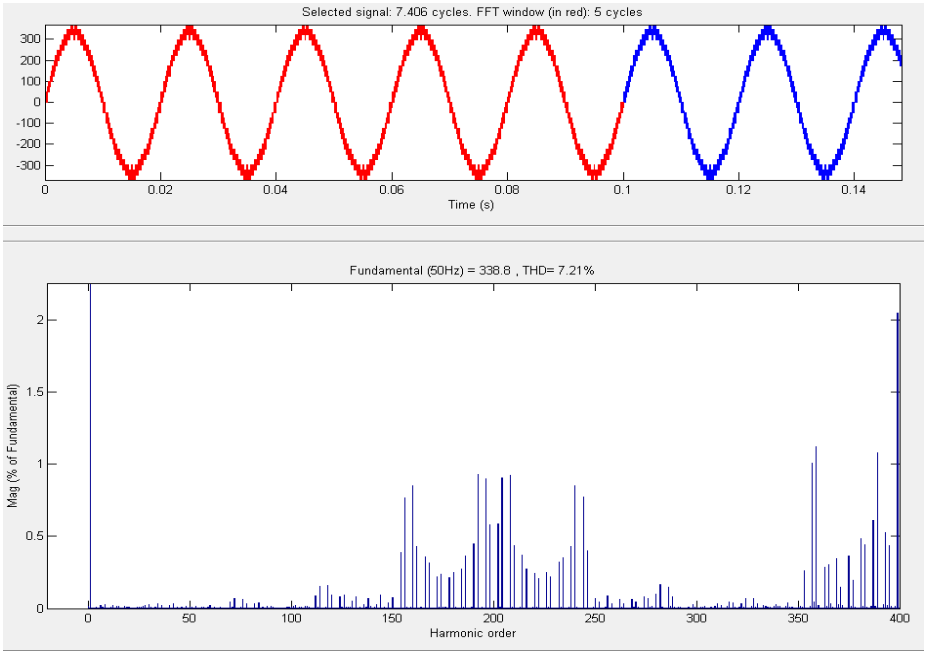

Fig .17. Harmonic spectrum of CHB phase voltage using SVPWM

For DCI also harmonic contents are significant only after 150th order for f_{cr}=10050Hz. This has THD slightly lesser than CHB line voltage THD but there is no significant improvement.As similar to line voltage THD, phase voltage THD for CHB inverter with different modulation techniques are simulated and they are compared and shown in fig.16 and Harmonic spectrum of CHB phase voltage using SVPWM shown in fig.17. which have THD as equal to line voltage THD of respective topologies. In the comparision graph Fig 16 , SVPWM tecchnique has lower harmonics compare to all other different switching pulses. Phase voltage THD for DCI inverter with different modulation techniques are simulated and they are compared and shown in fig. 18 and Harmonic spectrum of CHB phase voltage using

APOD technique shown in fig.19. In the comparision graph Fig 18 , SVPWM tecchnique has lower harmonics compare to all other different switching pulses.

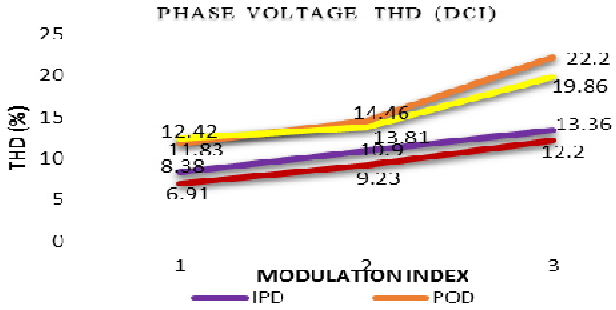

Fig .18. Comparison of phase voltage THD for DCI with f_{cr}=10050Hz for m_a=1,0.8,0.6.

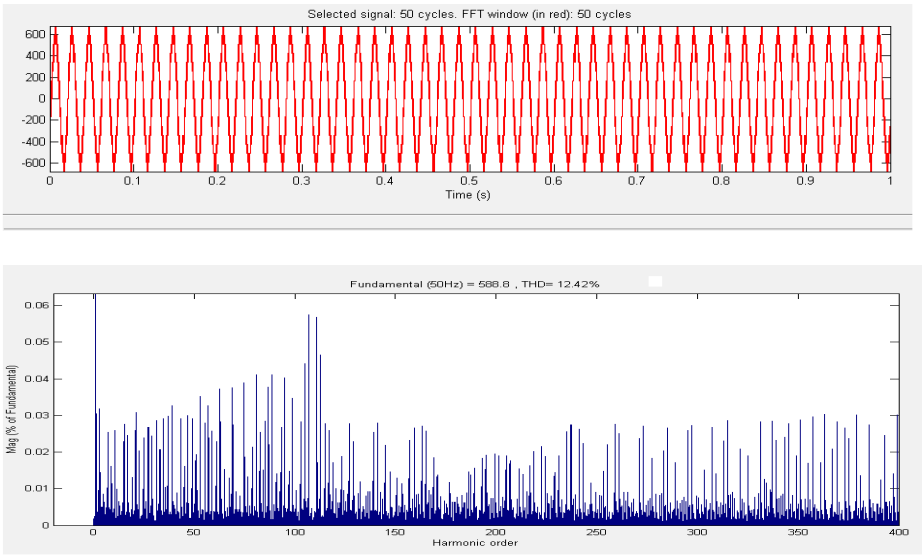

Fig .19. Harmonic spectrum of DCI phase voltage using APOD technique.

Line current have minimum THD with PSPWM technique but it has larger amount of lower order harmonic. It is difficult to design filter for lower order harmonics as the size of filter will be very large with higher loss. So, next to PSPWM, SVPWM has line current with lower THD and harmonic contents are significant only above 150th order and filter design is easy with compact and reduced cost. Harmonic content are centered around f_{cr}.

Fig. 20 shows line current THD of CHB inverter using different modulation technique for modulation indices(m_a) 1,0.8,0.6 are represented. Line current has harmonic content as 1.82% with peak current of 9.833A(6.95A rms). In the

comparision graph Fig 20 , SVPWM tecchnique has lower harmonics compare to all other different switching pulses.

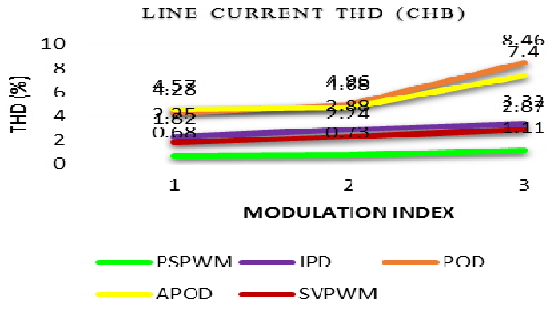

Fig .20. Comparision of line current THD for CHB inverter with f_{cr}=10050Hz for m_a=1,0.8,0.6.

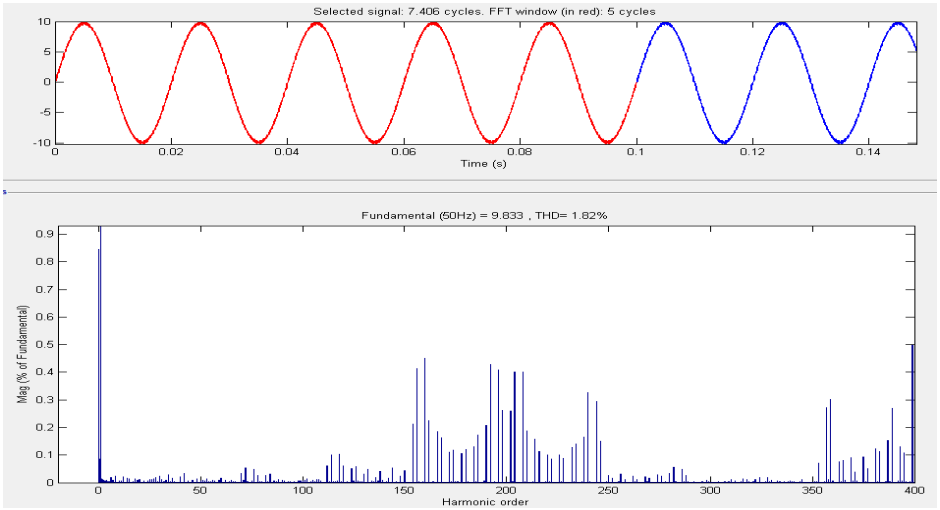

Fig .21. Harmonic spectrum of CHB line current using SVPWM

Harmonic spectrum for CHB line current using SVPWM with f_{cr}=10050Hz is shown in fig. 21.Line current THD comparision and harmonic spectrum using SVPWM modulation technique for DCI are shown in figure 22. and figure 23. respectively. In the comparision graph Fig 22 , SVPWM tecchnique has lower harmonics compare to all other different switching pulses. Here in x-axis modulation indices are labeled as 1, 2 and 3 which are correspoding to modulation index of 1, 0.8 and 0.6 respectively.

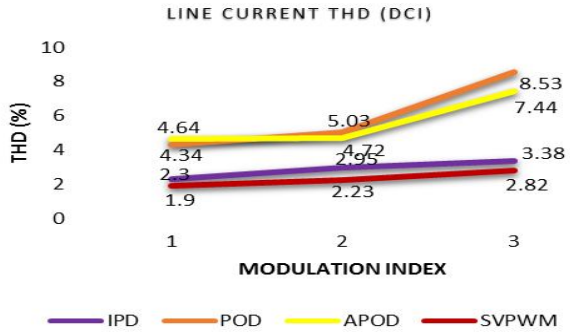

Fig .22. Comparison of line current THD for DCI inverter with f_{cr}=10050Hz for m_a=1,0.8,0.6.

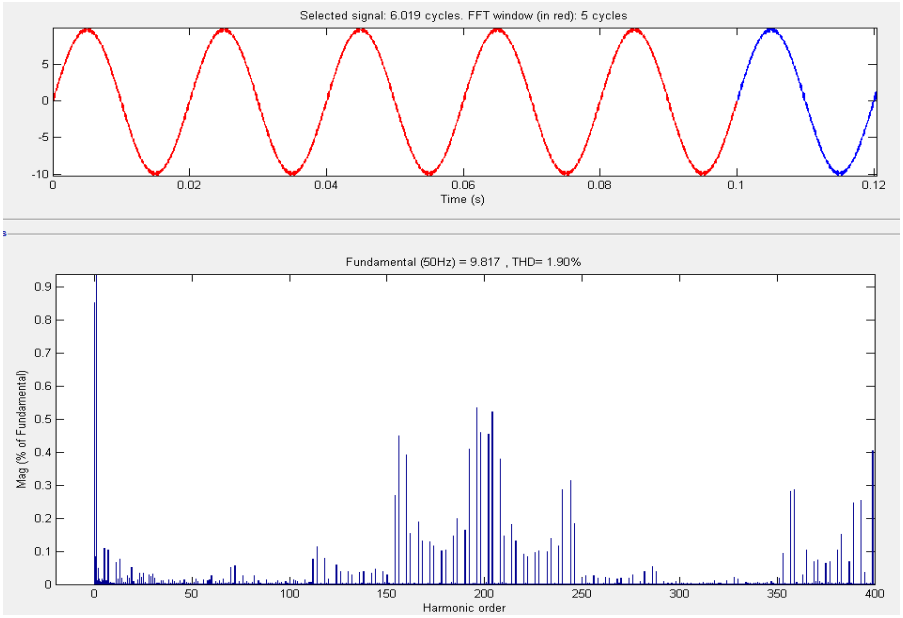

Fig .23. Harmonic spectrum of DCI line current using SVPWM

From fig. 23, it is clear that line current harmonics are very much low, but we need to decrese voltage harmonics and it needs filter. Depending on filter reactance and load reactance, line current harmonics gets affected. If we employ passive filter then there is a chance for resonance problem it can be eliminated by active filters. In grid-interactive systems, load impedance will vary rapidly. So active filters are best solution for these systems and also it depends on rating of the plant since active filters are not economical for low power rating. All the above harmonic contents are measuresed without filter.

4. COMPARISON OF CASCADED H – BRIDGE INVERTER WITH DIODE CLAMPED INVERTER

Line voltage and Line current of two inverters are captured. Harmonics for phase voltage, Line voltage and Line current of two inverters are captured. Based on the harmonics of CHB inverter and DCI different graphs are obtained. Fig. 24. shows the MATLAB simulation diagram of nine-level CHB inverter using SVPWM technique where power circuit and pulse generation circuts are not shown which are made as subsystem and only overview of simulation circuit is shown in the figure.

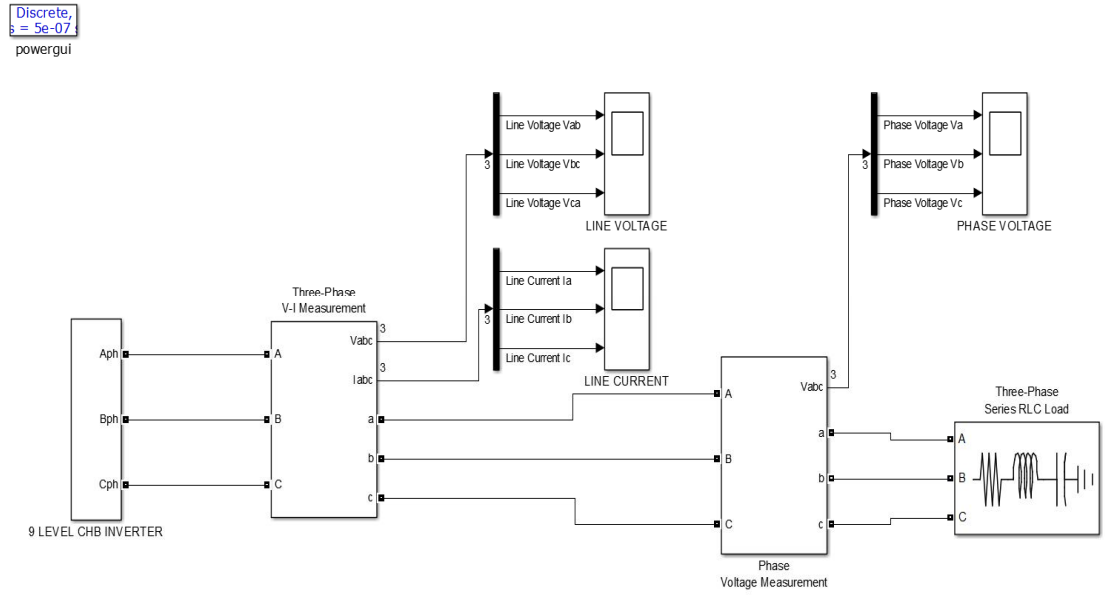

Fig .24. Simulation diagram of nine-level CHB inverter

Simulation of three phase line voltage and line current of CHB inverter using SVPWM technique are shown in fig 25 and 26 respectively. Simulation of three phase line voltage and line current of DCI inverter using SVPWM technique are shown in fig 27 and 28 respectively.

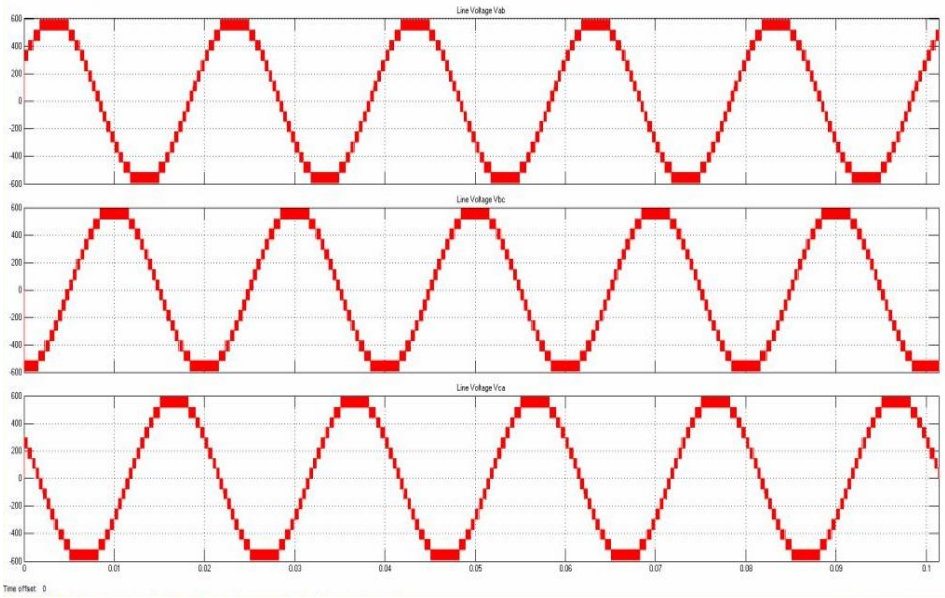

Fig .25. Simulation output of CHB inverter three phase line voltage using SVPWM.

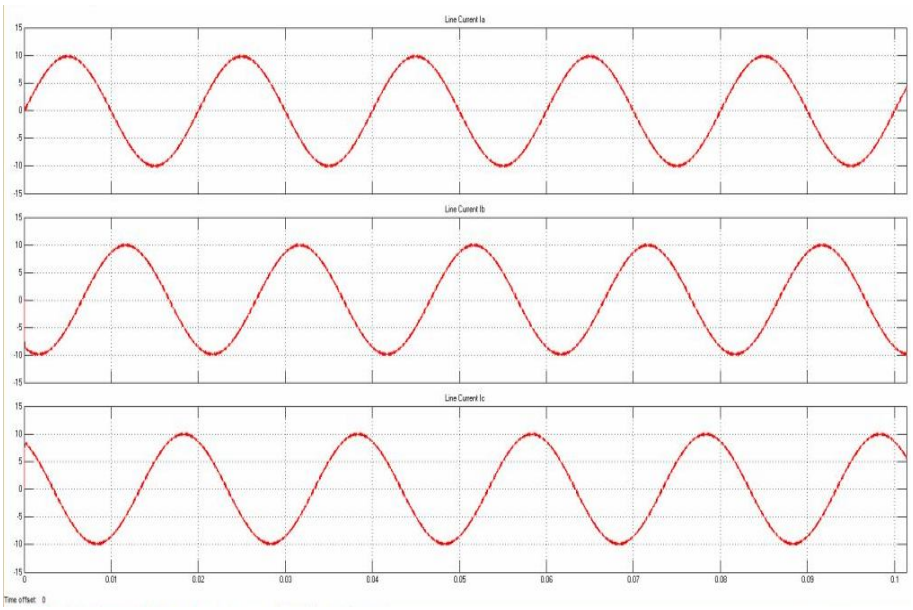

Fig .26. Simulation output of CHB inverter three phase line current using SVPWM.

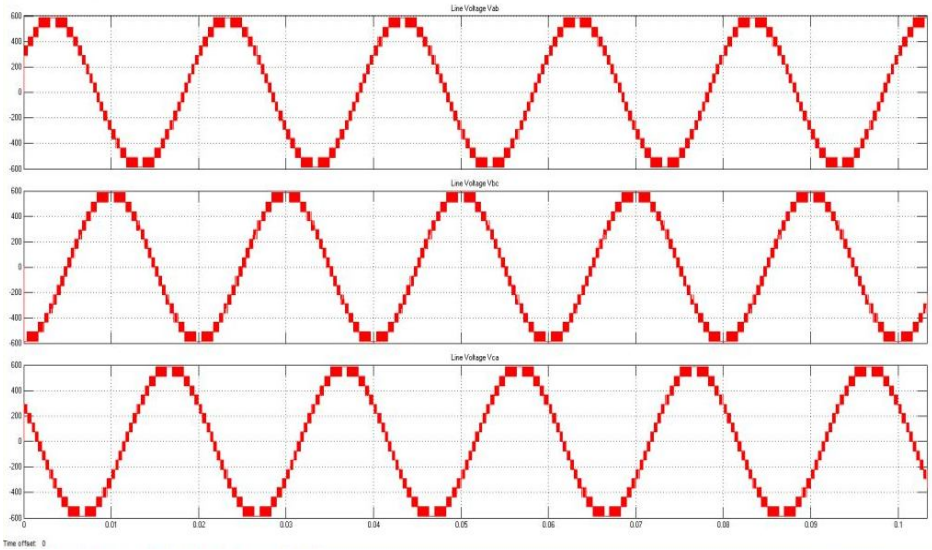

Fig .27. Simulation output of DCI three phase line voltage using SVPWM.

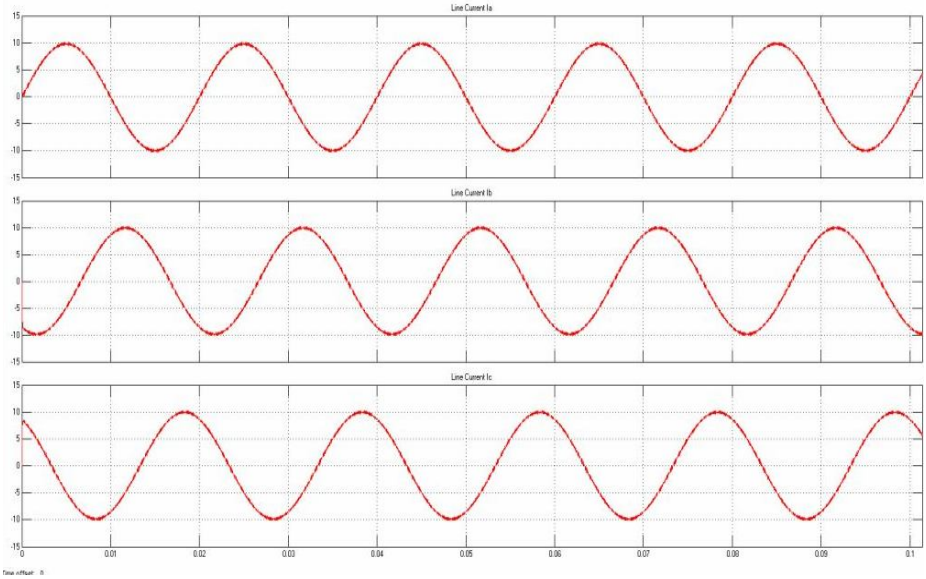

Fig .28. Simulation output of DCI three phase line voltage using SVPWM.

In fig 29. CHB inverter and DCI are compared based on line voltage THD for POD switching pluse with f_{cr}=10050Hz for m_a=1,0.8,0.6. In fig 30. inverters are compared based on line voltage THD for APOD switching pluse.

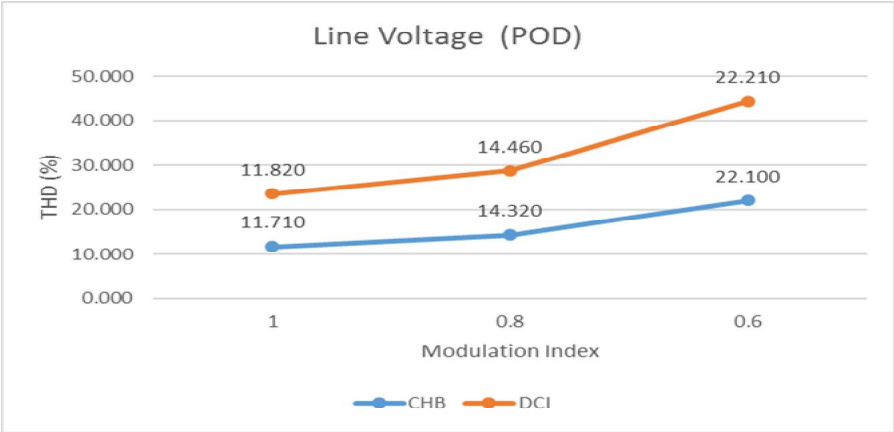

Fig .29. Comparison of line voltage THD for POD Switching pluse with f_{cr}=10050Hz for m_a=1,0.8,0.6.

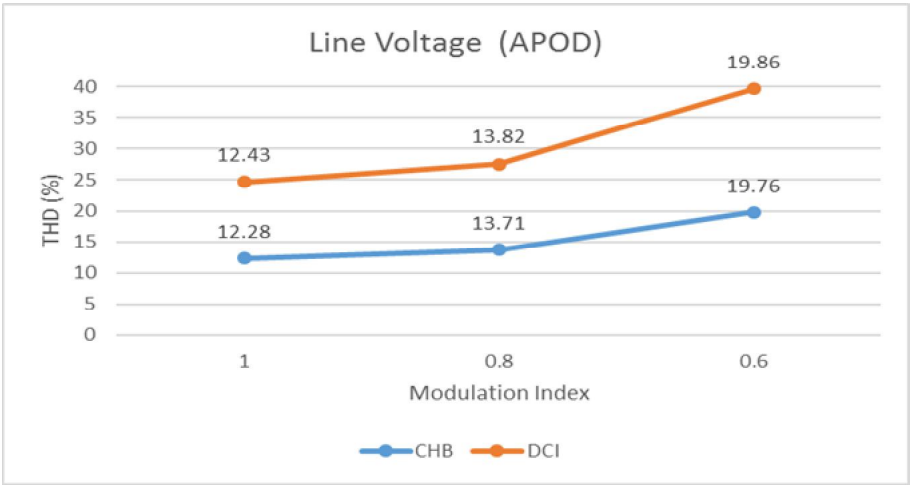

Fig .30. Comparison of line voltage THD for APOD Switching pluse with f_{cr}=10050Hz for m_a=1,0.8,0.6.

In fig31.inverters are compared based on line voltage THD for IDP switching pluse. In fig 32. inverters are compared based on line voltage THD for SVPWM switching pluse. Line voltage THD of CHB inverter is better than the DCI for different switching techniques.

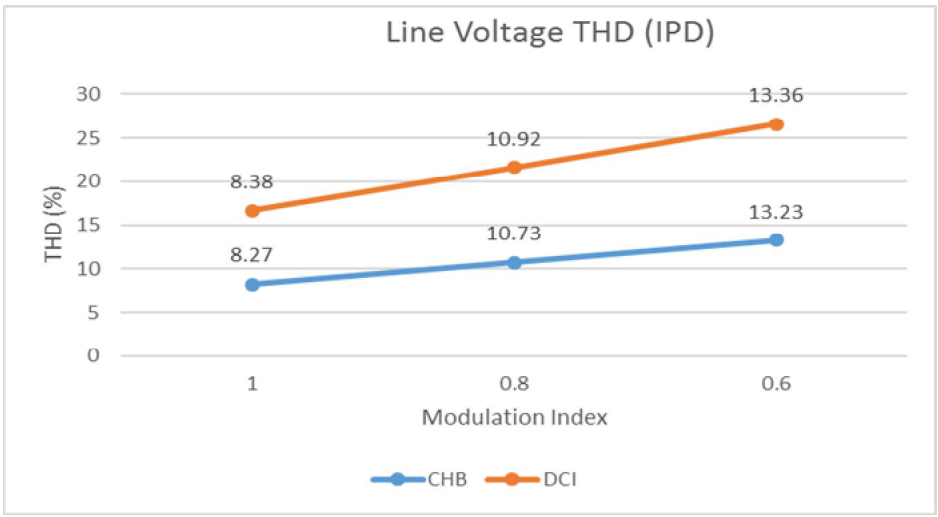

Fig .31. Comparison of line voltage THD for IDP Switching pluse with f_{cr}=10050Hz for m_a=1,0.8,0.6.

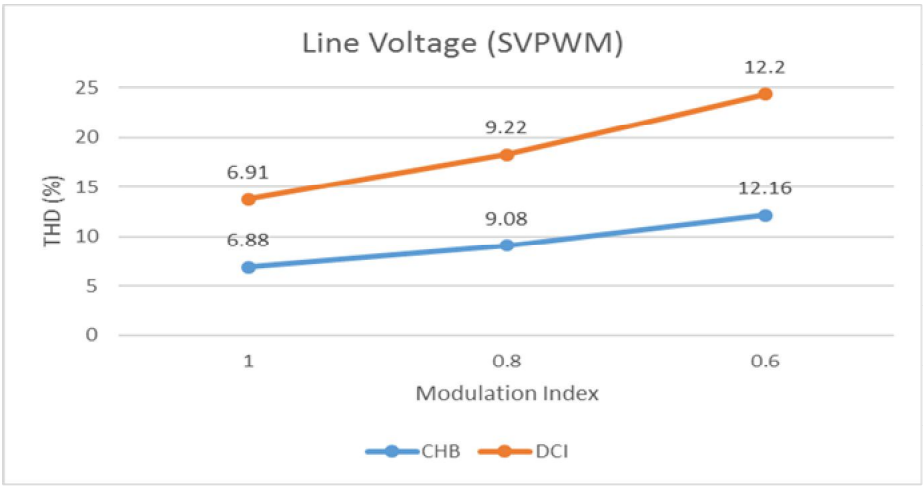

Fig .32. Comparison of line voltage THD for SVPWM Switching pluse with f_{cr}=10050Hz for m_a=1,0.8,0.6.

In fig 33. CHB inverter and DCI are compared based on line current THD for POD Switching pluse. In fig 34. Inverters are compared based on line current THD for APOD switching pluse.

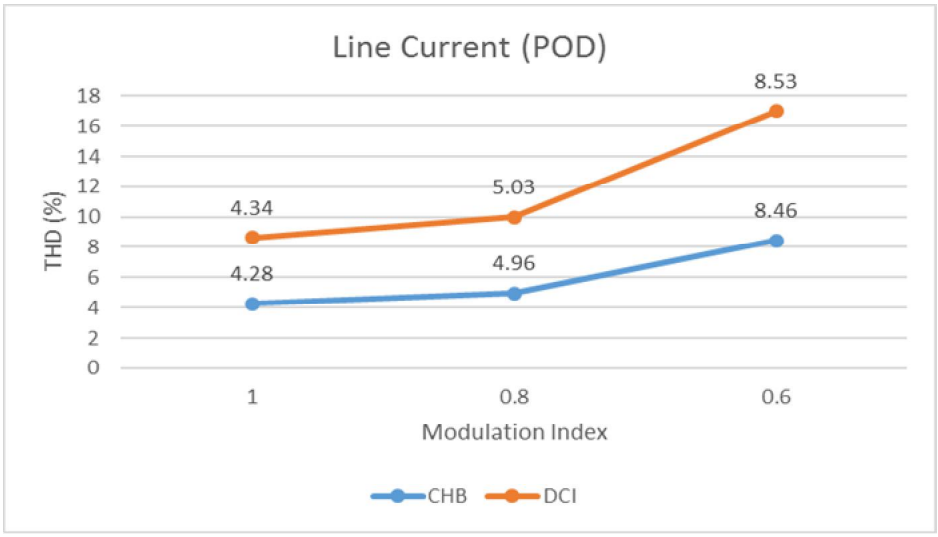

Fig .33. Comparison of line current THD for POD Switching pluse with f_{cr}=10050Hz for m_a=1,0.8,0.6.

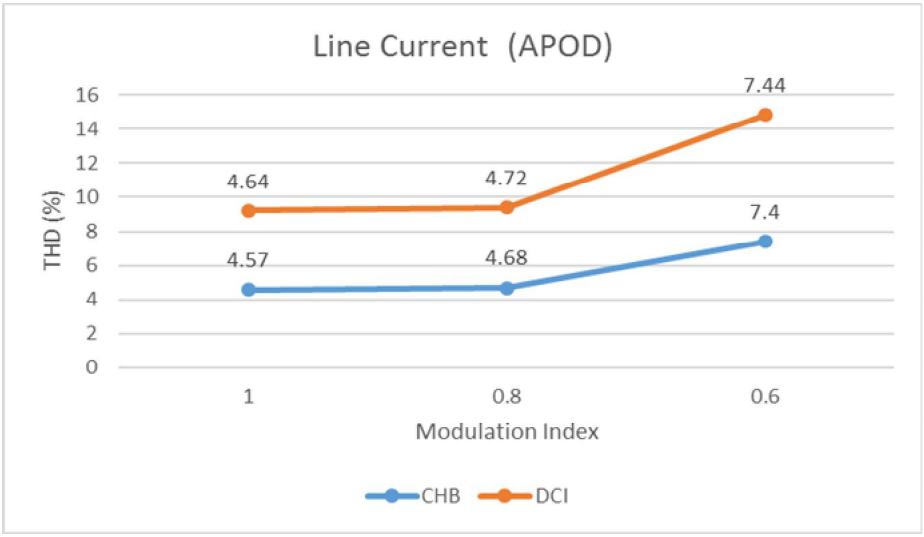

Fig .34. Comparison of line current THD for APOD Switching pluse with f_{cr}=10050Hz for m_a=1,0.8,0.6.

In fig 35. Inverters are compared based on line current THD for IDP switching pluse. In fig 36. Inverters are compared based on line current THD for SVPWM switching pluse.

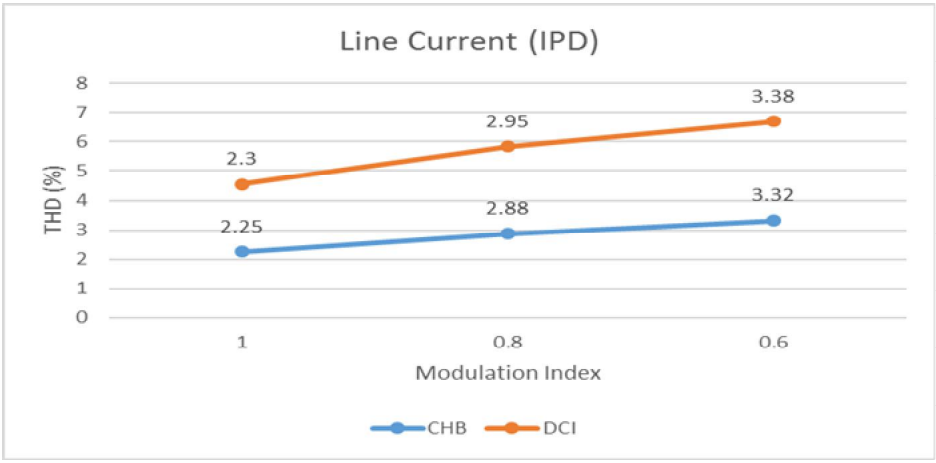

Fig .35. Comparison of line current THD for IDP Switching pluse with f_{cr}=10050Hz for m_a=1,0.8,0.6.

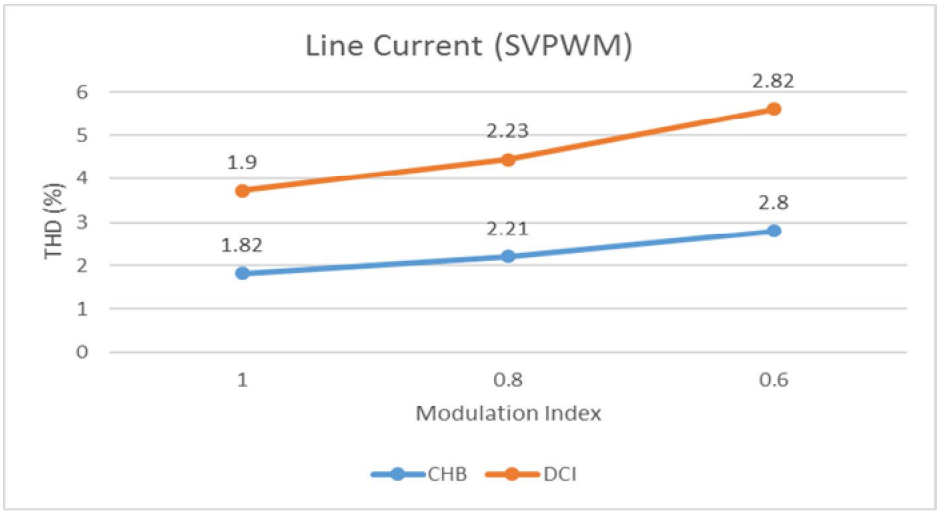

Fig .36. Comparison of line current THD for SVPWM Switching pluse with f_{cr}=10050Hz for m_a=1,0.8,0.6.

Line current THD of CHB inverter is better than the DCI for different switching techniques.

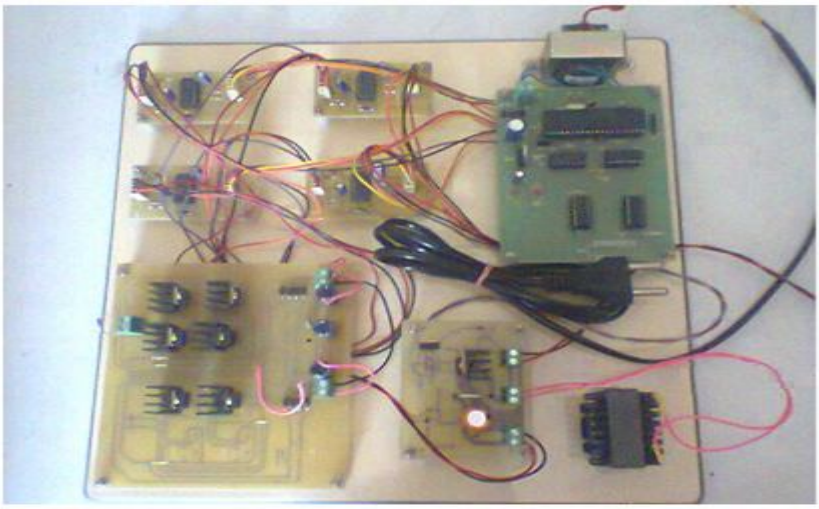

Fig .37. Hardware implementation of Cascaded H – Bridge Multilevel inverter.

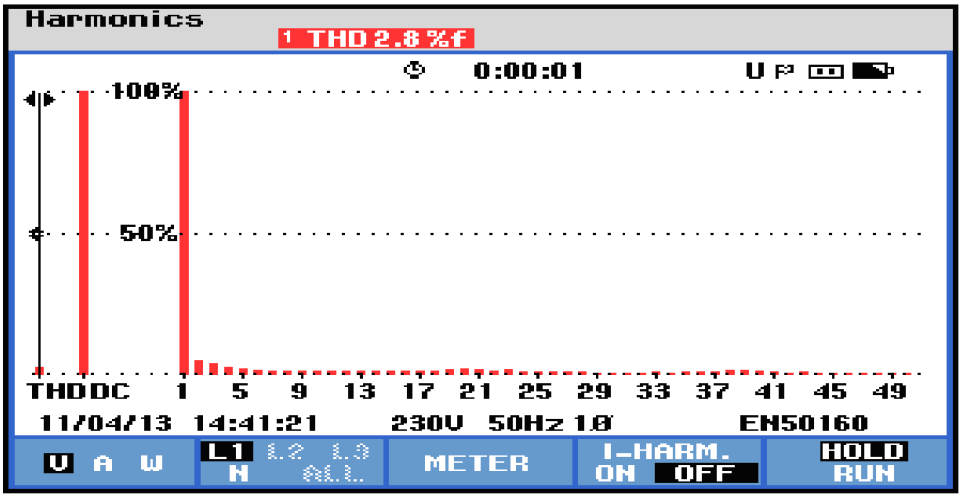

Fig .38. Harmonic spectrum of CHB line voltage.

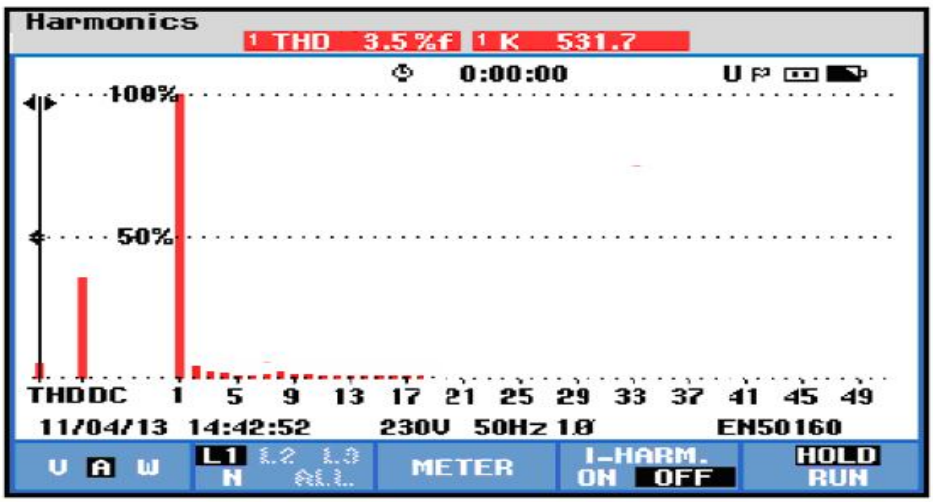

Fig .39. Harmonic spectrum of CHB line current using

Hardware implementation of Cascade H- Bridge Multilevel inverter is shown in figure 37. Harmonic spectrum of CHB inverter for line voltage and line current are shown in fig 38. and 39. respectively.

5. CONCLUSION

Nine-level CHB inverter and DCI simulated using different PWM techniques such as PSPWM, IPD, POD, APOD, SVPWM at different modulation index (m_a=1, 0.8 and 0.6) with f_{cr} as 10050Hz with power rating of 5kVA. Since our dc bus voltage is obtained by PV array, it is easily made into many dc voltage bus after a dc converter. Since CHB having many advantages over DCI and their simpler structure, it is selected as one of the best topology for PV application.

Among different modulation techniques, IPD and SVPWM provide lower harmonic content with higher order harmonics above 150th order which can be easily eliminated using low pass filter with cut-off frequency of 7500Hz. Filter size gets reduced and compact inverter module is possible with reduced loss.

Since SVPWM provides higher DC voltage utilization and it eliminates the problem of unbalanced output voltage caused due to disturbances in reference signal, it is one of the best PWM technique for three-phase inverters. Level of inverter and switching frequency are functions of switching losses, filter loss and also economics of losses and filter requirement. This paper concludes that the cascaded H- bridge multilevel inverter topology works well and shows hope to reduce the THD, compare to diode clamped multilevel inverter (Jeyraj Selvaraj et al, 2009) . Number of levels of the CHB inverter increases, the number of switches used is less compared to the other topologies.

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