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Regular paper

An Experimental and Investigation on Asymmetric Modular Multilevel Inverter an Approach with Reduced Number of Semiconductor Devices

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The super-lift method has made numerous remarkable contributions to DC/DC transformation technology. Positive output super-lift LUO converters can simply raise the DC input voltage directly into a greater stage DC output voltage. The new approach of Asymmetric Super-Lift Multilevel Inverter (ASLMLI) DC/AC technology proposed with reduced number of components compared to the asymmetrical type of MLI. The comparison is made for open loop and closed loop control PI and Fuzzy controller used to reduce the harmonic content significantly with vary of modulation index. This architecture to design single phase 7-level ASLMLI is put forth for solar application with incorporating intelligent technique. This circuit uses a single MOSFET switch with less switching stress and single DC source. It generates low distortion output uses through the harmonic band of the FFT window by utilizing MATLAB/Simulink software and a hardware implementation. As a result, minimum THD valid through seven level cases compare with Traditional MLI.

Keywords: Asymmetric Super-lift multilevel inverter (ASLMLI), Proportional integral (PI), Fuzzy logical control (FLC), Total harmonic distortion (THD), Modulation Index (MI).

1. Introduction

The absence of fossil fuels and the greenhouse effect, the need for sustainable energy has increased dramatically over time. Pulse width modulation (PWM) and multilevel modulation (MLM) are the two forms of DC/AC conversion techniques. For high voltage and high energy good quality applications, each kind has become numerous circuits that will use modulation [1]. Multilevel inverters use a different method than PWM, in which a reference waveform is vertically routine to produce a corresponding output waveform (e.g., a sine wave). Various inverter topologies are offered for DC/AC conversion in solar PV (SPV) systems, with the multilayer inverting technique horizontally collecting levels to attain the waveform [2-3]. Unlike the conventional inverter, Multi-Level Inverters (MLI) could be applied for harmonic reduction since these converters are on the basis of the line connection of one phase multilevel inverters and commonly placed on interface renewable power sources [4]. Neutral point clamped (NPC), flying capacitor (FC), and cascaded H Bridge multilevel inverter (CHBMLI) are three forms of classical MLI structures that are very useful for increasing the output voltage level [5]. AC drives and FACTS devices are coupled for commercial and industrial applications [6]. Many levels are generated from numerous clamping diode, clamping capacitor, and DC sources, which is a disadvantage of this converter design. All of the DC sources voltages have a unique quality in the

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asymmetrical approach, which ensures tremendous versatility. The quality of the end result voltage has been improved as a result of the multiple voltages with the use of the fewest semiconductor devices possible. Besides, this may expand the installation area, expense of the converter and intricate control circuits. ASLMLI strategy uses single switch are required because of various dc sources voltage extent, this may produce high number of output voltage. As a results proposed Super-Lift MLI increase the output voltage gain in a modulation index limitation which is relatively higher than that of the asymmetrical MLI [7- 8].This system design with 7-level single phase ASLMLI and optimization control techniques such as PI and Fuzzy based control for reduce THD has been further analyzed improvement of power quality using MATLAB/Simulink and a hardware implementation.

2. Asymmetric Super-Lift Multilevel Inverter

A method using a modified Super-lift Luo (DC/DC) converter and a super-lift multilevel inverter. Because MLI is dependent on DC sources, there are two types of MLI: 1) symmetrical type MLI 2) asymmetric type MLI. The maximum number of levels can be obtained with symmetric MLI [9]. This paper presented reduces multiple source asymmetrical type of modified super lift MLI [10]. In this regards number of levels increased by using multiple capacitors. The advantage of this proposed topology needs to less number of switch and minimized voltage stress across the capacitor.

2.1 Modified ASLMLI

This module basically consists of only one MOSFET Switch, two Freewheeling diodes and four parallel switching capacitor to generates seven level output (+3E 0 & -3E), (+2E 0 & -2E), (+ E 0 & -E,). Whereas traditional MLI NPC, FC and CHB [11] requires twelve to Twenty two switches generate the seven level of output in Table 1. By increasing the number of levels and employing several capacitors to obtain maximum voltage. In this regard, ASLMLI was formulated as follows:

2 diode (3 capacitor) +1 switch = 7 level

2 diode (7 capacitor) +1 switch = 15 level

2 diode (10 capacitor) +1 switch = 21 level

2 diode (12 capacitor) +1 switch = 25 level

2 diode (17 capacitor) +1 switch = 35 level

2 diode (22 capacitor) +1 switch = 45 level.

Table.1 Comparaison of MLI

MLI	Number of stages	Number of DC source	Number of switches	Number of clamping diode	Number of clamping capacitor
NPC	7	4	12	22	7
FC	7	6	12	12	11
CHB	7	3	12	12	0
Proposed ASMLI	**7**	**1**	**1**	**2**	**3**

In the ASLMLI path, a conversion over switch (2P2T) and a three point band switch are employed. When the main switch S is turned on, the source voltage (V_{input}) charges the inductor (L_1) and capacitor (C_1) during the switching on period kT. V_{C1}=V_{input} in the steady state in Figure 1. When the main switch off duration (1-k) T decreases voltage level – (V_{out} – 2V_{input}), the end result voltage V_{out} is much raised from the source voltage aid of inductor L_1 and capacitor C_1. As a result, the inductor's ripple current i_L is provided below. In Equation (1-3), can be given as,

$$\nabla i_{L1} = (V_{input}/L)\, KT = [(V_O - 2V_{input}) / L]\, KT \quad (1)$$

$$\text{Voltage gain } V_{Output} = \left(\frac{2-k}{1-k}\right) V_{input} \quad (2)$$

Where k is the Duty cycle, Vo is output voltage

$$V_{output} = \left(\frac{2-k}{1-k}\right)^2 V_{in} \quad (3)$$

The ASLMLI uses three capacitors, C_2, C_3, and C_4, are used to divided the output voltage in 7 levels, When Duty cycle k = 0.5.the capacitor band switch Turn ON time (T_{on}) starting from 3E,2E,1E,0 and turn OFF time (T_{off}) -1E,-2E,-3E respectively in ASLMLI: Therefore, the operation status is as follows:

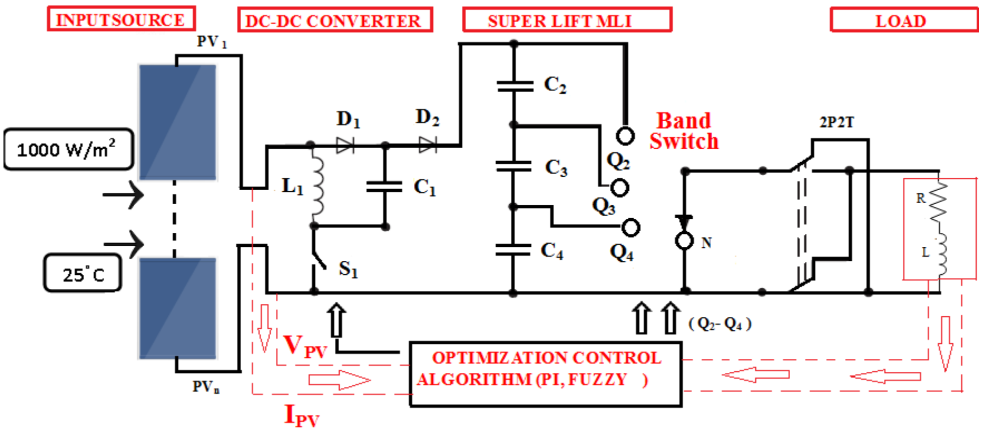

Fig.1 proposed seven levels Super-lift MLI

3. MODES OF OPERATION ASL-MLI

3.1 ON state:

- In Figure 2a, the voltage across the capacitor voltage (Vc2) is connected over band switch is on condition, and the switch is at point Q2.

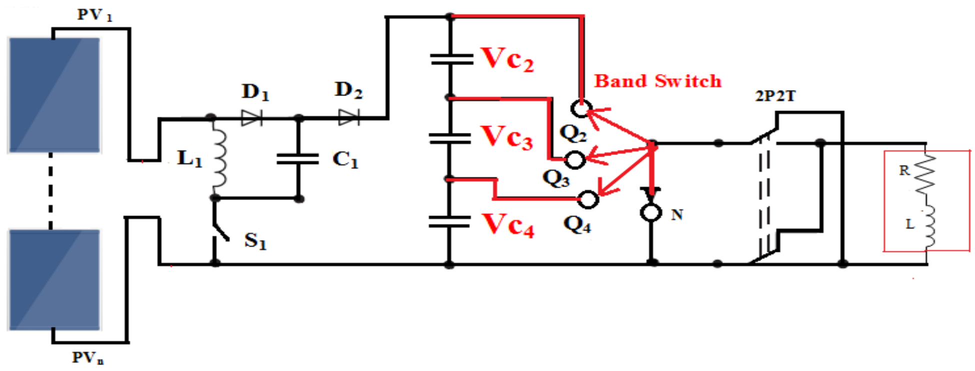

Fig. 2(a) ON state

➢ In Figure 2a, the voltage across the capacitor voltage (Vc3) is connected over band switch is on condition, and the switch is at point Q2. Next stage the voltage across the capacitor voltage (Vc4) is connected over band switch is on and the switch is at point Q4. Finally, the voltage across the capacitor voltage (neutral) is zero connected over band switch is on and the switch is at point N.

3.2 OFF state:

- ➢ In Figure 2b, the voltage across the capacitor voltage (-Vc2) is connected over band switch is off condition, and the switch is at point Q2.
- ➢ In Figure 2b, the voltage across the capacitor voltage (-Vc3) is connected over band switch is off condition, and the switch is at point Q3.
- ➢ In Figure 2b, the voltage across the capacitor voltage (-Vc4) is connected over band switch is on and the switch is at point Q4. Finally, the voltage across the capacitor voltage (neutral) is zero connected over band switch is on and the switch is at point N. asymmetric Super-lift MLI Switching methods as shown in Table 2.

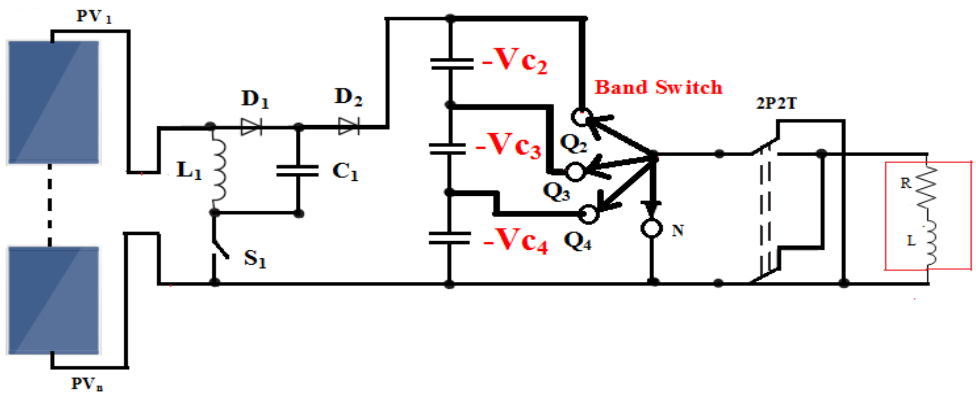

Fig. 2(b) OFF state

Table 2 Inverter Switching Method of ASLMLI

S.No	Band Switch Point	Conversion over Switch point	
		Switch on state	**Switch off State**
1	Q2	3E	-3E
2	Q3	2E	-2E
3	Q4	E	-E
4	N	0	

4. Simulation of PI and Fuzzy Logic Control ASLMLI

To improve the stability associate with super lift Inverter under dealing with PI controller continues to be offered as being a good option towards control over switching electrical power inverters [13]. In this division evaluation is carried out a open and closed loop way. It may be any kind of operator, here we're utilizing PI controller [12-13]. The number of switches used here is one MOSFET switches, their gate signals are given by means of sorting algorithm as shown in Figure 3. The load used here is a Resistive load and their corresponding references are fed to the controller and their gate signals are given by means of PI controller scheme. The ASL output steps with least number of devices by utilizing proposed seven stages MLI. The PI controller scheme effect of K_p should be reduce a large part of the overall error and K_i reduce the final error in a system uses to designed in the work with Ziegler-Nicholas tuning techniques in Figure 4. The MOSFET gate signals are generated and fed to the inverter band switches. It provides the output of seven levels SSLMLI [14]. Digital computer assists a vital role in Fuzzy rationale strategy for making the process to simplify. FLC system can be providing an exact framework without usage of mathematical model. Through develop FLC expected SSL-MLI output. The explained detailed about Fuzzy logical control scheme in a symmetric super-lift inverter in Figure 5. FLC is divided in to five modules: fuzzifier, database, rule based, decision maker and defuzzifier [15-16]. The inputs Fuzzy operators are error (E)= $V_{reference} - V_{output}$ and the conversion of error (COE)= $E_n - E_n$-1. Where the V_0 is end result voltage of the ASLMLI, Vreference is the preferred output voltage and δ_{mn} is change of band switching position inverter by the FLC at the n^{th} sampling instant, using δ_{mn} update the band switching position signal ms is obtained and fed to the asymmetric super-lift MLI which provides the appropriate conversion over switch signal in Figure 6.

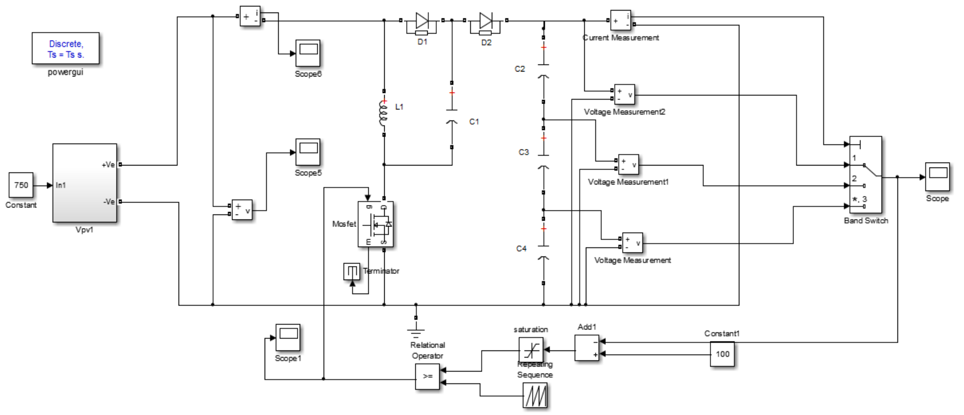

Fig 3 Proposed closed loop PI Super-lift MLI

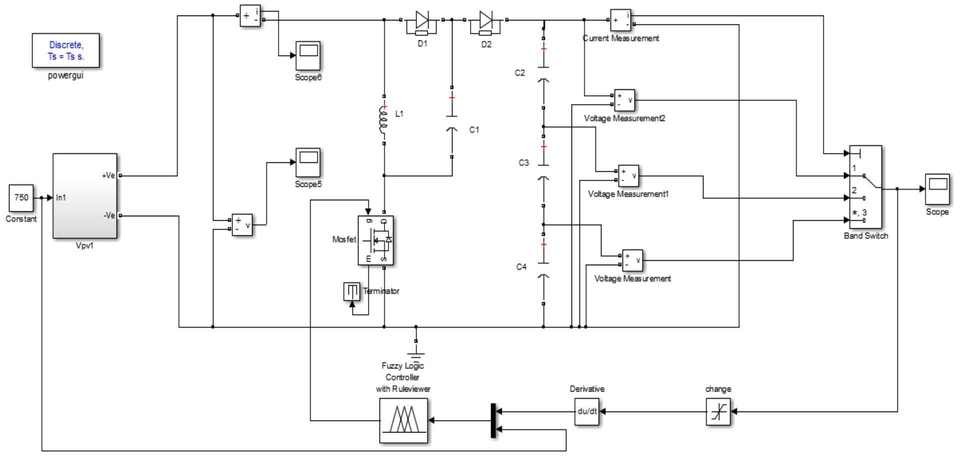

Fig.4 Proposed closed loop Fuzzy Super-lift MLI

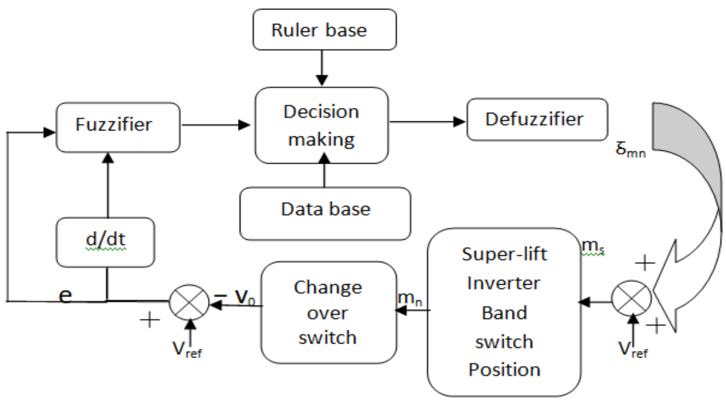

Fig.5.Fuzzy logic control scheme for ASLMLI

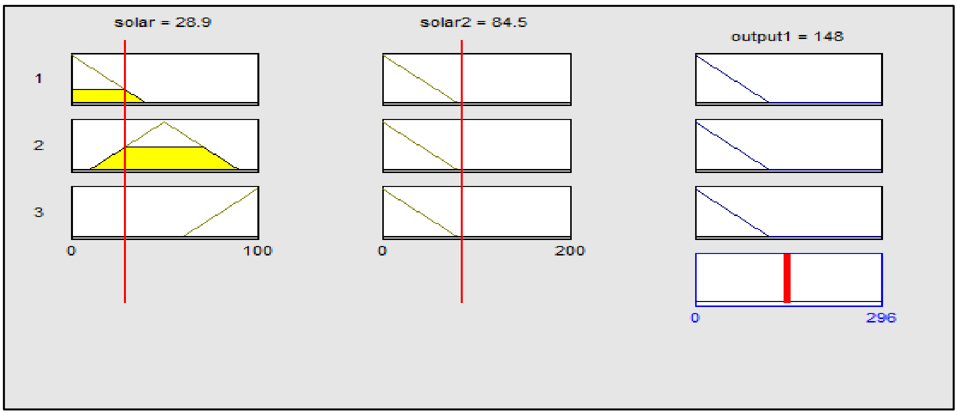

Fig.6. Fuzzy Ruler view scheme for ASLMLI

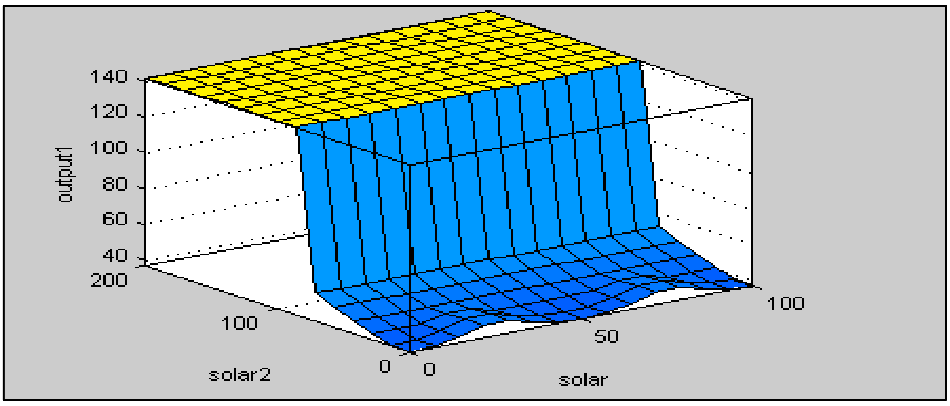

Fig.7.Fuzzy Surface viewer for ASLMLI

The Fuzzification to be directed record highlights for knowledge and profitability alongside standards are utilized. The crisp values of triangular membership function in Figure 6. To obtain correct productivity defuzzification is performed on Fuzzy ruler view. The principles are made from an inference system using mamdani algorithm [17-20]. The contributions inputs are joined to the fuzzification block using preprocessor. The RMS productivity voltage of seven level ASLML inverter is derive the fuzzy control rules created a based on the following criteria: i). At the point when the output of SLMLI diverges from the reference, the change of modulation index must be a big. ii). Once the end result of MLI is approaching the reference a little change of modulation index is essential. iii). Once the SLMLI output is higher than the reference the variation of modulation index must be negative and vice versa. The output of surface viewer from SLMLI in fig 7.this Result of the saturation block for limiting the most and minimal values of THD.

5. Result & Discussion

For a typical 7-level, asymmetric multilevel inverters have PV modules and only one switch operating under different Modulation index in Table 3. This proposed circuit of asymmetric SLMLI best choice of boosts the output voltage with a single DC source conversation in Figure 8. The output of ASLMLI is three time of DC input voltage (PV module). PI control is designed to ensure the specifying desired nominal operating point for SLMLI, it regulates inverter circuit, such that it keeps nearer to minimal functioning point in event of quick disturbances, collection point variations, modeling mistakes and modules variations. PI operator controls proportional gain (K_p) and integral gain (K_i) made in the applying Zigler-Nicholas tuning methods the developed values are 1.0 and 0.02 respectively [21-26]. The output voltage and current waveforms are shown in Figure 9 and their corresponding THD obtained here are 15.67%. It reveals the simulated closed loop active response of load voltage and load current of a PI controlled inverter full load voltage is performed by MATLAB using FFT evaluation to obtain is really a specific values. Total harmonics analysis of Fuzzy output voltage (V_{rms}) is 110.06V. The seven stage of MLI offers the maximum output result three times of the solar feedback voltage. The ranges from MI 1 to 0.3 for corresponding THD and V_{rms} are evaluating closed loop with different controller FLC in Figure 10.

Table.3.Simulation parameter of SLMLI.

S.no	Parameter name	Value
1	Irradiation	1000W/m^2
2	Open circuit voltage V_{oc}	70 Volts
3	Short circuit voltage I_{sc}	4.5 Amps
4	Inductor L_1	50 mH
5	Capacitor C_1	28μF
6	Switching capacitor C_2, C_3 and C_1	80μF
7	Output voltage from Fuzzy	148v
8	Output voltage Vo from PI	126v
9	Output current Io (Fuzzy,PI)	4.3-3.4A

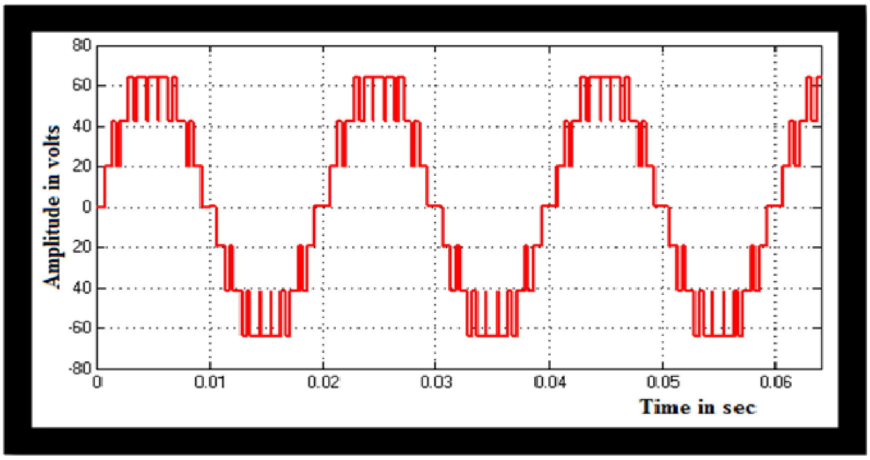

Fig.8 Output voltage waveform

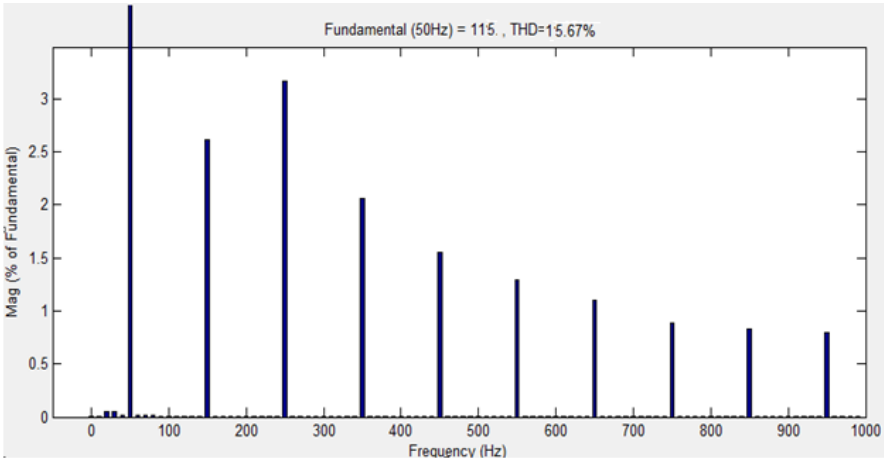

Fig.9 FFT Analysis of Closed loop PI Control

The PIC microcontroller kit with battery development platform is used to operate and connect the hardware model. The performance gate signal is provided by the PIC microcontroller kit's buffer, and the conversion over switch is turned on, with the band switch set to 3E, 2E, E, 0 & -E, -2E, -3E, respectively. The operational conditions used in the simulation are the same as those used in the Low-Power experimental model in Figure 11. The performance of the controller is tested and compared the result with simulation and experimental result as shows in Table 4 and Table 5 displays literature review of intelligent techniques.

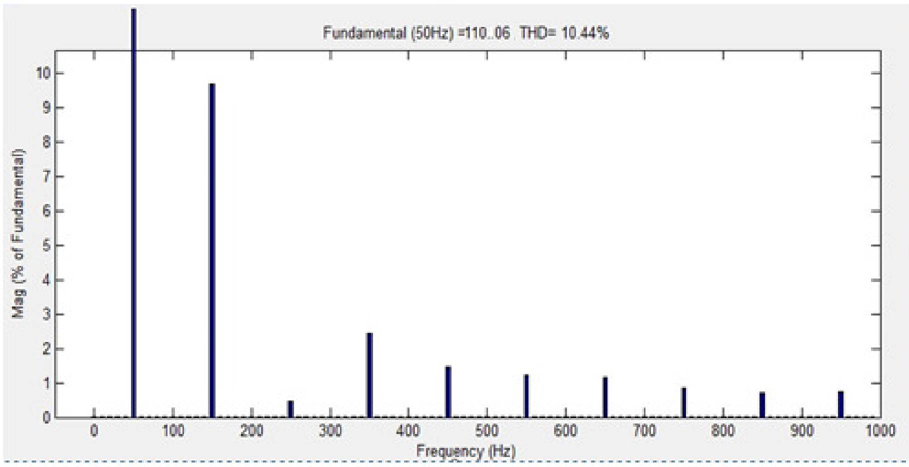

Fig.10 FFT Analysis of Closed loop FLC Control

Fig.11 Hardware setup

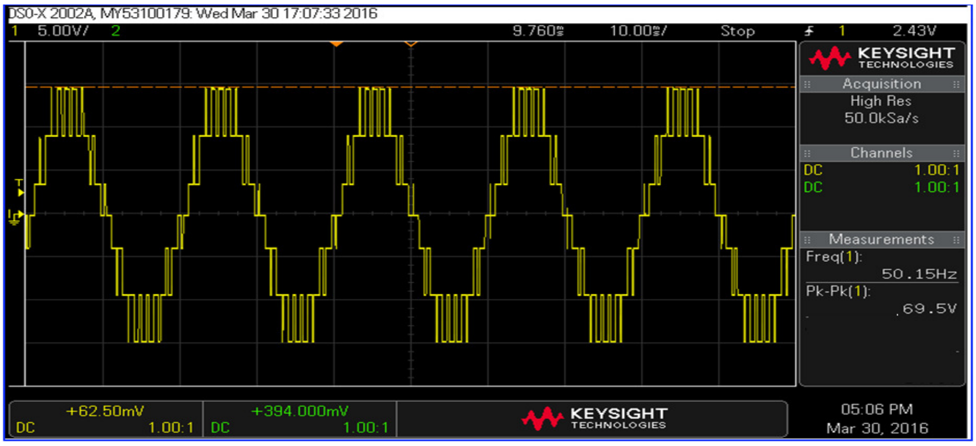

Fig.12 Output voltage of inverter

Table 4 Comparison of Simulation and Hardware Results

Intelligent Techniques	**Simulation**				**Hardware**			
	R Load		**Induction Motor**		**R Load**		**Induction Motor**	
	% V_{THD}	% I_{THD}	% V_{THD}	% I_{THD}	% V_{THD}	% I_{THD}	% V_{THD}	% I_{THD}
FLC	10.59	**10.44**	11.15	12.36	18.2	**17.4**	18.23	19.5
PI	16.32	**15.67**	17.52	17.82	21.98	**10.4**	19.52	25.52

The design specifications of this super-lift output voltage are as follows: solar power 70V, 3.5A SLMLI was operated with an output frequency of 50 Hz, and a carrier switching frequency of 1 kHz, and a resistive load of 100 ohms. The ASLML inverter stage control with respective standalone mode to provide a standard output voltage of 128 V_{rms}/50HZ and current of 2.5 A in Figure 12. The performance of controller is a feasible operation system which is verified for comparison the experimental result in Figure 13 and 14. The main impact of the proposed control scheme is to reduce harmonics of the proposed inverter.

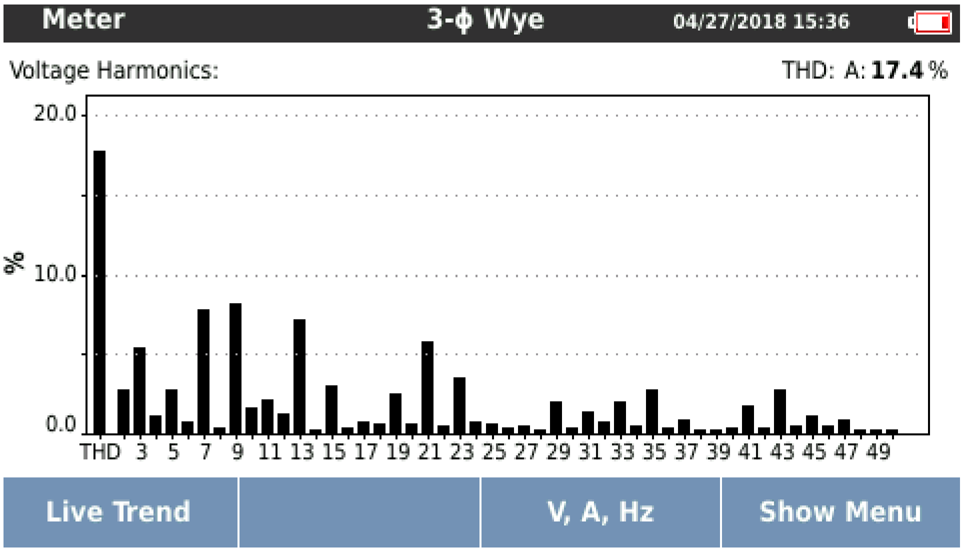

Fig.13 Hardware FFT anlaysis of PI Controller (Closed Loop Controller)

Table 5 Literature Review of Controller

Intelligent Techniques			
Azeem *et al.* (2019)	FLC	7	20.27%
Elbarbary *et al.* (2018)	FLC	7	20%
Proposed FLC	FLC	7	10.44%

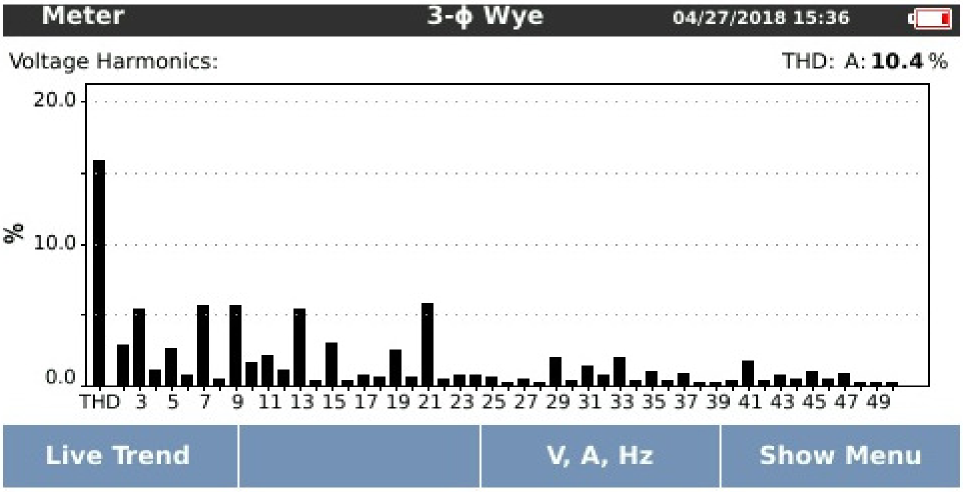

Fig.14 Hardware FFT analysis of FLC Controller (Closed Loop Controller)

6. Conclusion

In that research, PI, Fuzzy get a handle on approach in simulation, and equipment with least distortion productivity voltage with power quality priority are used to apply seven level asymmetric form of super-lift MLI. The performance measures of the asymmetric multilevel productivity voltage waveform, such as harmonic distortion values, are studied, and contrast is made by appropriate values. Asymmetric multilevel inverter minimum harmonics presence is 10.44% simulation and 10.4% in hardware. Hardware single stage seven level prototypes with less switching stress and low distortion output is used to test the validity of the simulated results. In the coming decades, the ASLMLI concept will be a great choice for power electronic frameworks, particularly for photovoltaic and wind power applications.

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