International Journal of Electronics

ISSN: (Print) (Online) Journal homepage: www.tandfonline.com/journals/tetn20

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To cite this article: V. Thamizharasan & N. Kasthuri (2024) FPGA implementation of proficient Vedic multiplier architecture using hybrid carry select adder, International Journal of Electronics, 111:8, 1253-1265, DOI: 10.1080/00207217.2023.2245194

To link to this article: https://doi.org/10.1080/00207217.2023.2245194

Published online: 10 Aug 2023.

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INTERNATIONAL JOURNAL OF ELECTRONICS
2024, VOL. 111, NO. 8, 1253–1265
https://doi.org/10.1080/00207217.2023.2245194

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FPGA implementation of proficient Vedic multiplier architecture using hybrid carry select adder

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ABSTRACT

Nowadays, the application of computations and communications is needed for high performance, reduced size and lower power utilisation. The multiply and add functions are one of the frequently used operations in digital signal processing. Various types of multipliers are available in digital Various types of multipliers are available for various Signal processing applications.. Among these multipliers, Vedic multiplier is one of the most optimised multipliers used in a signal processing module. In the existing method, the Vedic multiplier is designed with conventional adders, which is having higher area utilisation, lower speed and higher power consumption. Hence, the modified Vedic multiplier is proposed to improve the speed of multiplication using hybrid technology. The partial products of the proposed multiplication are added using 2×2 Vedic multiplier and hybrid carry select adder (binary to excess one converter (BEC), Han-Carlson adder and Multiplexer). The critical path delays of hybrid 4×4 Vedic multiplier are the summation of 2×2 Vedic multiplier, two full adders, two multiplexers and two BECs for producing the final product. The proposed hybrid Vedic multiplier is operated at high speed with reduced size as compared to the existing multiplier techniques. The proposed hybrid Vedic multiplier is designed and simulated using Verilog HDL and implemented in Spartan 6 field-programmable gate array device. The implementation results showed that the delay of the proposed multiplier gets ameliorated as compared to array multiplication (30.84%), Wallace tree multiplication (29.52%), multiplication based on compressor (23.71%), Vedic multiplication by carry look-ahead adder (22.91%), Vedic multiplication by ripple carry adder (14.45%), revised booth multiplication (15.42%) and Vedic multiplication by Han-Carlson adder with BEC (13.95%) and hybrid multiplier (11.37%).

ARTICLE HISTORY
Received 30 January 2023
Accepted 2 July 2023

KEYWORDS
Adder; multiplier; hybrid Vedic multiplier; XILINX ISE 14.1; Verilog HDL

1. Introduction

At present, higher operation speed is required for most of the applications. In signal processing applications (modulation, demodulation, CPU, filters and image and signal processing), multiplication is an essential operation in arithmetic computation (Heng

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et al., 2019). Also, arithmetic operations such as additions and multiplications determine the speed of the signal processing applications.

In any digital system applications, the utilisation of power consumption, size and speed are the major parameters to compute the performance of the whole system. The speed of these applications depends on the performance/speed of a multiplier. Thus, there is a need to investigate the size, power and speed of the multiplication for optimising the computation speed of the signal processing applications (Hussain et al., 2019). Optimisation of area, delay and power of building blocks in signal processing has become a challenging assignment.

There are various types of multipliers available for the multiplication of two binary numbers. They are array multiplication, multiplier using carry save adder, pipeline-based multiplier, serial/parallel multiplication, 2's complement multiplier, booth multiplication, Wallace tree multiplication, etc.

The organisation of this communication is as follows. A survey of additions and review of multiplication are discussed in Sections 2 and 3. In Section 4, the proposed Vedic multiplication using hybrid adder is addressed. The performance analysis of the proposed multiplier with comparisons of existing multiplications is addressed in Section 5. Finally, the conclusion of the proposed work is addressed in Section 6.

2. Review of additions

In signal processing modules, the adders play a major role in determining their performance. In many signal processing applications, the additions are not only used as an arithmetic operation. They are used in an address of the memory location calculation, to determine the number of instructions fetching/executing/decoding of microprocessor and microcontroller, etc. Different types of adder techniques are available for performing the addition of two binary numbers. These techniques are Ripple Carry Addition (RCA) (Heng et al., 2019), Carry Look-ahead Addition (CLA) (Balasubramanian & Mastorakis, 2018), Carry Save Addition (CSA), Carry Select Adder (CSELA) (Balasubramanian & Mastorakis, 2018; Jeevan & Sivani, 2018), Brent Kung Addition (BKA) (Neha & Greeshma, 2019), Carry Increment Addition (CIA) (Neha & Greeshma, 2019), Han-Carlson Addition (HCA) (Neha & Greeshma, 2019), Ling Adder (Suganya & Meganathan, 2015), Carry Select Adder using Weinberger Adder (Suganya & Meganathan, 2015), etc.

RCA is a basic fundamental adder. The main pros of this adder is minimum hardware components. However, it has less speed, as each output carry has to wait till the input carry propagates to the output of each full adder module (Heng et al., 2019). To overwhelm this trouble, CLA is introduced. The main advantages of this addition are increased the speed of operation due to the final output carry bit is depended only on input carry bit. However, it increases the area due to separate circuits for producing the carry and sum bits (Balasubramanian & Mastorakis, 2018).

For few signal processing designs, the in-between carry bits are not required, thereby introducing a carry skip logic circuit. The main advantage is improvement in speed and area utilisation. The cons of this adder is the use of limited application only.

To further ameliorate the speed of addition, a new technique is introduced by assuming the value of input carry bits (carry input '0' and '1') before the start of operation. It is

called a carry select adder. The advantage of this adder is improvement in operation speed which is double the speed of RCA. However, the utilisation area is high (Balasubramanian & Mastorakis, 2018; Jeevan & Sivani, 2018).

Another addition logic was introduced to improve the delay of operation further based on the concept of parallel prefix addition. It is called Han-Carlson adder. The pros of Han-Carlson adder is an excellent tradeoff between the fanout and the number of logic gates. The disadvantage of this adder is a longer path to the output (Neha & Greeshma, 2019). In order to minimize the size and further improve the speed of CSELA by replaced RCA (Cin = 0) to BK Adder. This type of structure is called Linear Brent-Kung CSELA (LBKCSELA) (Udaya Kumar et al., 2017). Further to improve the speed of LBKCSELA, pattern of the input is slightly changed in each stage. This structure is called Square Root BKCSELA (SQRTBKCSELA).

In order to optimize the power consumption, D-latch-based CSELA is introduced. In BKCSELA/LBKCSELA, the RCA (for cin-0) was changed by D-latch (Natarajan et al., 2017). CSELA area is further improved by the introduction of a common Boolean logic. In this technique, some portion of previous output will be shared as present input. Hence, the number of logic cells was reduced and the consumption of power was also minimised as compared to the Modified CSELA (Kishore Kumar & Balaji, 2017).

Furthermore, the speed of CSELA is improved by applying the Weinberger principle/recurrence to CSELA. The BK adder is exchanged with Weinberger adder in LBKCSELA. This adder has a minimum area (only few numbers of gates needed to design a BEC) as compared to RCA. Also, the utilisation of power is less as compared to other addition techniques (Udaya Kumar et al., 2017).

3. Review of multiplication

Multiplication is one of the most important and fundamental operations in signal processing transforms, digital fitters (FIR, IIR, adaptive), DSP processor (MAC operation), communication systems (modulation and demodulation technique), multimedia compression techniques and cryptography applications (Hussain et al., 2019). In recent days, there is a need to design high-performance system/modules for portable devices. In that, the arithmetic operation decides the performance of the system. Hence, it is to enhance the

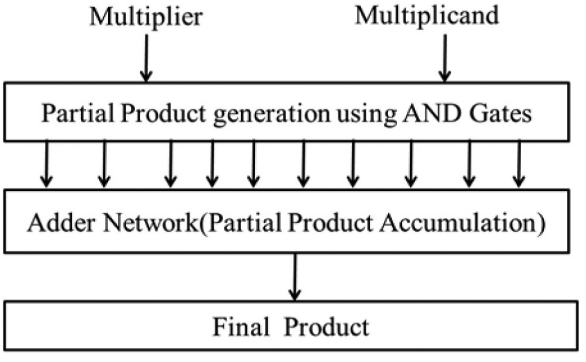

Figure 1. General structure of multiplier.

speed and area of the arithmetic operation. The multiplication operation mainly depends on the addition operation. The general structure of multiplier is displayed in Figure 1.

The multipliers were classified with respect to reducing the partial products, and they are array multiplication and tree-based multiplication (Hussain et al., 2019).

Array multiplier is an efficient design for combinational multiplication. Pros of array multiplier are less design complexity, ease of scalability and regular structure. Cons of array multiplier are high power consumption and requirement of more number of gates (Hussain et al., 2019).

To reduce the delay of multiplication, Wallace tree multiplier is introduced. The advantage of Wallace tree multiplier as compared to array multiplier is the minimisation of delay, but it increases the memory requirement and power consumption.

Speed of multiplication is further increased by booth multiplier technique. The pros of this multiplier are increase in the operation speed and reduction in design complexity of multiplication. However, the area utilisation was increased due to the recoding process (Boppana et al., 2019).

To reduce the power consumption by introducing another technique for multiplication is bit serial array multiplier. This method achieves high clock rate. Shift and add multiplication was introduced as a multiplication method. The advantages of this method are simplicity and relatively small area requirement. However, the speed of this multiplier is slow and it requires more number of clock cycles.

For improving the speed of multiplication further, the Vedic concept was introduced. This Vedic multiplication is implemented using sutra (Urdhva Triyakbhyam) as vertically and crosswise product. The product generation time of integer multiplication is reduced while using these Vedic principles as compared to other multiplier techniques. The same principle is applied to the binary multiplication (Sivanandam & Kumar, 2019).

The advantage of this multiplier is that it is the fastest method compared to other multiplication techniques. The delay of multiplication is significantly reduced as compared to other multipliers (Edavoor et al., 2020).

We presented a discussion on speed, area, power utilisation of various multiplier and their advantages and disadvantages. Investigation on the partial products accumulation minimization is essential to improve the performance of Multiplier. (Karri Manikantta et al., 2019).

In signal processing system modules, the high-speed adder and multiplier with low power and the minimum area play a crucial role. Hence, it is necessary to investigate the area, power and delay parameters of the adder and multiplier used in signal processing operations. Hence, the hybrid parallel adder-based multiplier and hybrid technology-based carry select adder (CSELA) are proposed to improve the speed of multiplication and addition as compared to the existing techniques.

4. Proposed multiplier

The various adders and multipliers are discussed in sections 2 and 3. Based on the above discussions, there is essential to deliberation on the partial products addition and minimisation for optimising the speed and size utilisation of multiplication. From above literature, the Vedic multiplier is one of the high-speed techniques of multiplication as compared to other multiplication techniques.

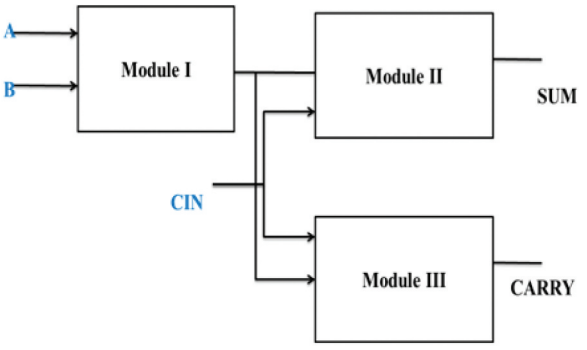

Figure 2. Architecture of hybrid adder.

Furthermore, a revised Vedic multiplication (VM) design is proposed to ameliorate the speed of multiplication. This proposed Vedic multiplier is designed using a hybrid adder instead of RCA.

4.1. Hybrid adder

The adder is designed with the help of various circuit structures, and it is named as hybrid adder. The general structure of hybrid adder is displayed in Figure 2. Let us consider an example of full adder. It consists of three modules: Module I, Module II and Module III. Each module is designed using different design methodology called hybrid full adder. The

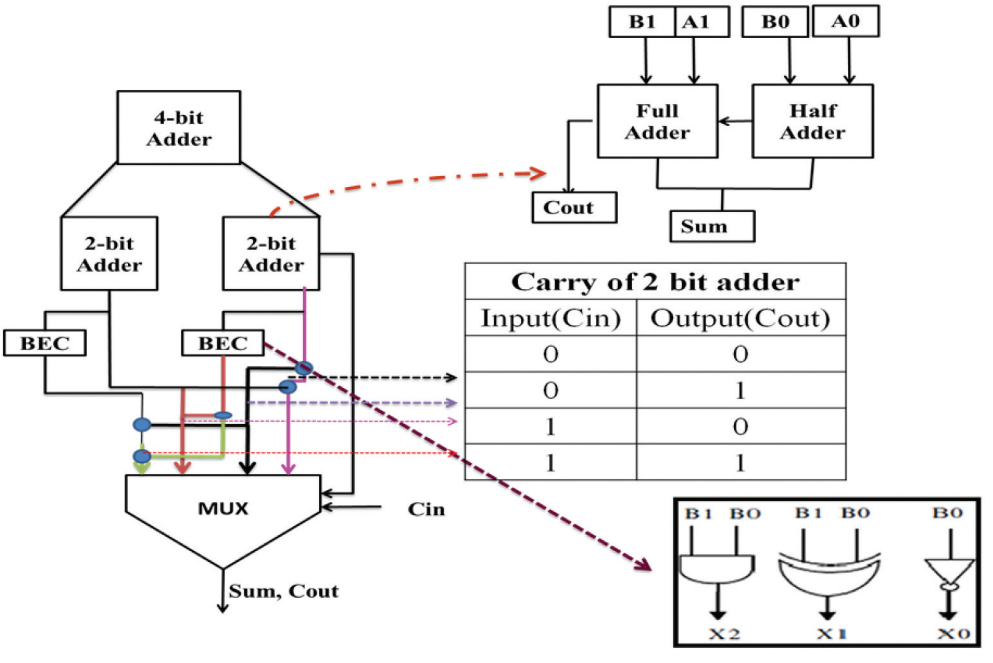

Figure 3. Architecture of proposed hybrid adder.

same principle is applied to 4-bit adder called hybrid adder. Also, this structure is displayed in Figure 3.

This hybrid adder performs the addition of two numbers in binary using CSELA. In this structure, the 4-bit adder is split into dual 2-bit adders consisting of two 2-bit adder, two BECs (3-bit) and one 4:1 multiplexer.

The sum (2-bit) and carry (1-bit) of this 2-bit adder are computed using one full adder and half adder. This 2-bit adders operate based on the assumption that the input carry is equal to zero, producing the output of sum (2-bit) and carry (1-bit). After that, the sum of 2-bit adder is passed to the BEC module. The BEC module performs the operation of sum+ '1'. The final output is selected using multiplexer with the help of input and output carry of the first 2-bit adder. The input of multiplexer is the output of 2-bit adder (sum) and BEC output. The final output is selected by the multiplexer by below-mentioned choice of first 2-bit adder input and output carry.

(i) If '00', multiplexer picks the sum (first and second 2-bit adder) as output sum and C_{out}.
(ii) If '01', multiplexer picks the sum (first 2-bit adder) and BEC (second) as output sum and C_{out}.
(iii) If '10', multiplexer picks the sum (second 2-bit adder) and BEC (first) as output sum and C_{out}.
(iv) If '11', multiplexer picks the sum BEC (first and second) as output sum and C_{out}.

The various adder's delays (critical path) are mentioned as follows:

(1) Ripple carry adder is four full-adders delay.
(2) Carry look-ahead adder is delays of four full adders, 4-bit AND gate and 4-bit OR gate.
(3) Conventional carry select adder is delays of four full adders plus four multiplexer (4:1) delays.
(4) CSELA-BK-BEC is delays of four full adders, BEC (4-bit) and four multiplexer (4:1) delays.
(5) CSELA-Han-Carlson using BEC is delays of four 2-input AND gate, four 2-input OR gate, one buffer, BEC (4-bit) and four multiplexer (4:1) delays.

Table 1. Critical path delays of several adders.

S. No.	Name of the Adders Techniques	Critical Path delays
1.	CSELA using Han-Carlson with BEC	4 AND Gates (2-input) + 4 OR Gates (2-input) + Buffer + BEC (4-bit) + 4 Multiplexers (4 to 1).
2.	CSELA using Brent-Kung adder with BEC	4 Full Adders + BEC (4 bit) and 4 Multiplexers (4 to 1)
3.	Ripple carry adder	4 Full Adders
4.	Carry look-ahead adder	4 Full Adders + 4 AND Gates + 4 OR Gates
5.	Carry select adder	4 Full Adders + 4 Multiplexers (4 to 1)
6.	Proposed hybrid adder	2 Full Adders + 1 Multiplexer (4 to 1) + BEC (3-bit)

The propagation delay (critical path) of the proposed adder is displayed in Figure 3, and it is encountered as double full-adders, BEC (3-bit) and multiplexer (4:1) delay for computing C_{out}. Hence, the delay of the proposed hybrid adder is ameliorated as compared to other existing adder techniques, and it is shown in Table 1.

4.2. Proposed hybrid Vedic multiplier

The structure of the proposed hybrid Vedic multiplier (4×4) is shown in Figure 4.

In this architecture, the multiplicand is (A0 to A3), multiplier (B0 to B3) and product (C0 Ro to R7). This architecture consists of four 2×2 Vedic multipliers and three 4-bit hybrid carry select adders. This proposed multiplier has three stages. The first stage has four 2×2 Vedic multipliers, and it generates the partial products. After that, the partial products are accumulated in second, third and fourth stages with the help of the proposed hybrid CSELA. The maximum path delay (critical path) of the proposed hybrid Vedic multiplier is encountered (from Figure 3) as one 2×2 Vedic multiplier delay and three 4-bit hybrid adder delays. The delay of the proposed multiplier is ameliorated as compared to other multiplier techniques.

The critical path delay of Vedic multiplier using conventional adder (ripple carry adder) is the delay of nine full adder delays, three half adder delays and one 2×2 Vedic multiplier delay. The critical path delay of the proposed hybrid Vedic multiplier is one 2×2 Vedic multiplier delay and three 4-bit hybrid adder delay. As per Table 1, the critical path delay of the proposed hybrid adder is two full adder delays, one multiplexer (4 to 1) delay and one BEC (3-bit) delay. Therefore, the critical path delay of the proposed hybrid Vedic multiplier is six full adder delays, three multiplexer (4 to 1) delays, three BEC (3 bit) delays and one 2×2 Vedic multiplier delay. Therefore, the delay utilisation of the proposed Vedic multiplier is improved as compared to conventional Vedic multiplier.

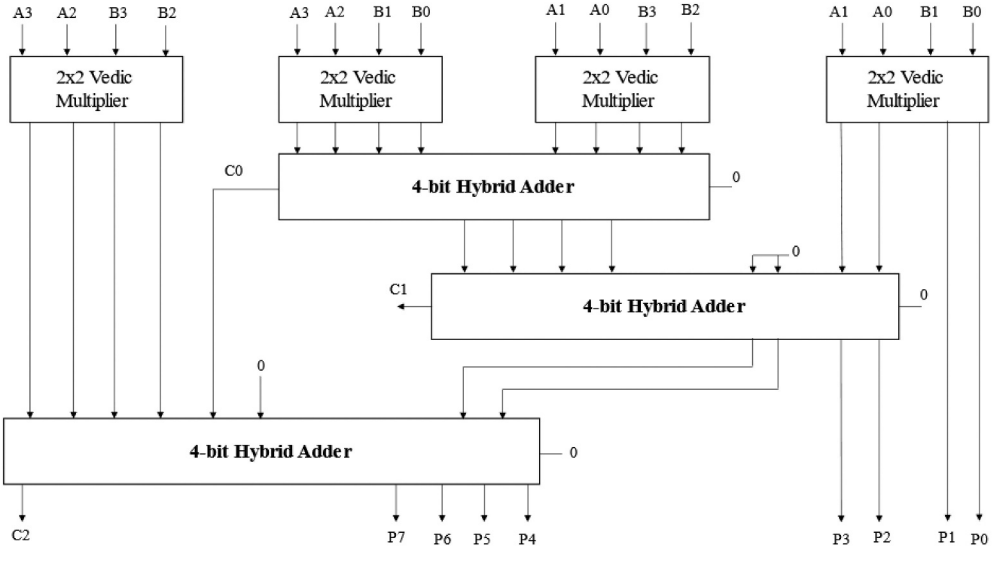

Figure 4. Architecture of proposed hybrid Vedic multiplier using hybrid adder.

Furthermore, the FIR filter (4-tap) is designed using the proposed hybrid Vedic multiplier and the proposed adder with field-programmable gate array (FPGA) implementation. Also compared with conventional FIR filter, the delay of conventional FIR filter using conventional adder and multiplier is 42.93 ns. The delay of the proposed FIR filter is 35.16 ns. This proposed FIR filter improved the delay by18.15% as compared to the conventional FIR filter.

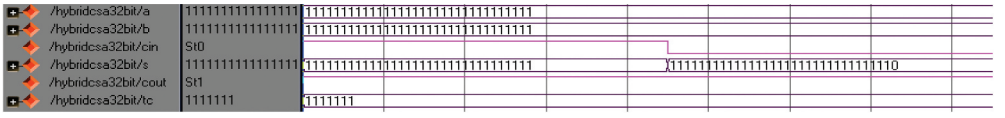

Figure 5. Result of proposed adder using hybrid technique.

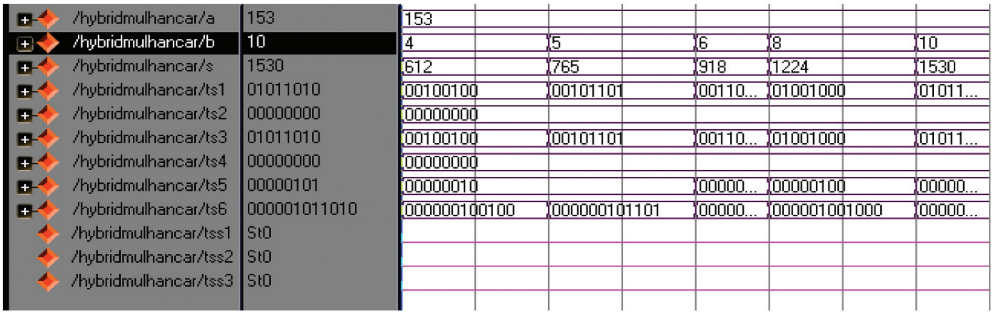

Figure 6. Result of proposed hybrid Vedic multiplier.

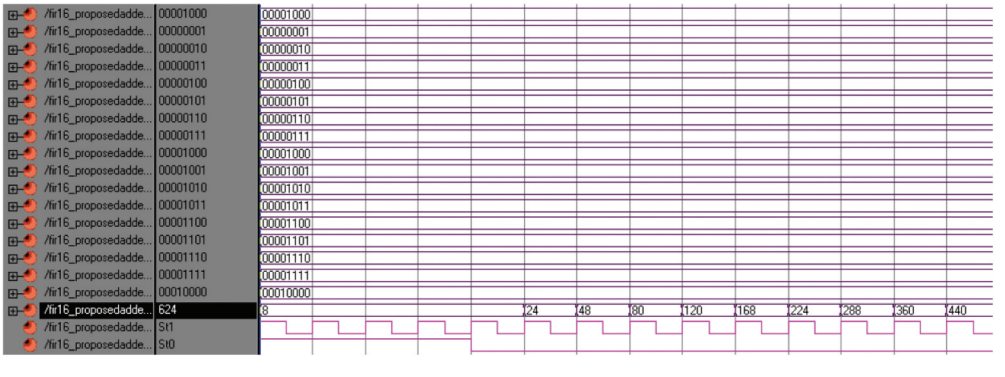

Figure 7. Result of FIR filter using hybrid Vedic multiplier.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	90	2400	3%
Number of fully used LUT-FF pairs	0	90	0%
Number of bonded IOBs	33	102	32%

Figure 8. Device utilisation for hybrid Vedic multiplication.

5. Performance analysis

Different multiplication and addition techniques are examined in sections 2 and 3, and the proposed multiplier and adder are explained in section 4. All addition and multiplication technique are simulated and synthesised in XILINX ISE 14.1 and implemented in Spartan 6 FPGA using Verilog HDL. All the adders and multipliers are simulated and functionally verified separately. Figure 5–8 show the simulation result of the proposed hybrid adder, simulation result of the proposed hybrid multiplier, simulation result of FIR filter and device utilisation report of the proposed hybrid Vedic multiplier, respectively.

Table 2. Delay and area utilisation of several addition techniques using Spartan 6 FPGA.

		16 bit		32 bit		64 bit	
S. No.	Method of Addition	Number of Slice	Delay (ns)	Number of Slice	Delay (ns)	Number of Slice	Delay (ns)
1.	Carry look-ahead adder	24	4.6	48	8.6	96	16.6
2.	Ripple carry adder	26	5.1	49	9.1	97	17.1
3.	Conventional CSELA	24	4.9	48	9.3	96	15.5
4.	CSELA using common Boolean logic	25	4.9	50	9.4	133	18.3
5.	CSELA using Weinberger with BEC	30	3.3	62	5.7	124	10.7
6.	CSELA using D Latch	42	4.2	84	7.6	168	14.5
7.	CSELA using Brent Kung	36	3.4	72	5.2	144	8.8
8.	CSELA using BK-RCA (Cin = 1)	24	4.9	48	9.3	96	15.6
9.	CSELA using Han-Carlson with BEC	36	3.4	72	5.2	144	8.8
10.	CSELA using Ling adder	27	7.2	57	15.7	114	30.6
11.	Proposed CSELA	24	2.9	48	4.7	96	8.7

Table 3. Delay and area utilisation of several multiplication techniques in Spartan 6 FPGA.

S. No.	Method of Multiplication	Delay (ns)	Number of LUT	Power (μW)	ADP	PDP
1.	Proposed Hybrid Vedic Multiplier (VM)	14.8	86	55.7	1272.8	824.3
2.	Hybrid Multiplier	16.7	90	53.5	1501.2	893.1
3.	Vedic Multiplier using HCA	17.2	126	55.9	2172.2	964.1
4.	Vedic Multiplication (VM) using Ripple carry adder	17.3	108	53.9	1867.3	931.2
5.	Modified Booth Multiplication	17.5	91	53.7	1587.9	937.4
6.	Vedic Multiplication (VM) using Carry Look-Ahead adder	19.2	113	54.9	2167.3	1052.4
7.	Multiplication based on compressor	19.4	120	53.5	2324.4	1036.7
8.	Wallace tree multiplication (WTM)	21.0	116	59.2	2431.4	1239.8
10.	Array Multiplication	21.4	84	52.5	1799.3	1125.2

ADP: Area delay Product, PDP: Power delay Product.

The utilisation of speed in terms of delay, size, power of several adders and multipliers is displayed in Table 2 and Table 3. The percentages of speed improvement in terms of delay for the proposed hybrid Vedic multiplier are displayed in Table 4 as compared to other multiplication techniques.

A comparison conveys that the delay of the proposed hybrid Vedic multiplier is ameliorated 30.84%, 29.52%, 23.71%, 22.91%, 14.45%, 15.42%, 13.95% and 11.37% as compared to array multiplication, Wallace tree multiplication, multiplication based on compressor, Vedic multiplication using carry look-ahead adder, Vedic multiplication based on ripple carry adder, improved booth multiplication, Vedic multiplication using HCA with BEC module and hybrid multiplier, respectively.

Similarly, the area delay product of the proposed hybrid Vedic multiplier is ameliorated by 29.26%, 47.65%, 45.24%, 41.27%, 31.83%, 19.84%, 41.40% and 15.21% as compared to array multiplication, Wallace tree multiplication, multiplication based on compressor, Vedic multiplication using carry look-ahead adder, Vedic multiplication based on ripple carry adder, improved booth multiplication, Vedic multiplication using HCA with BEC module and hybrid multiplier, respectively.

In the same way, a power delay product of the proposed hybrid Vedic multiplier is ameliorated by 26.74%, 33.51%, 20.48%, 21.67%, 11.47%, 12.06%, 14.50% and 7.70% as compared to array multiplication, Wallace tree multiplication, multiplication based on compressor, Vedic multiplication using carry look-ahead adder, Vedic multiplication based on ripple carry adder, improved booth multiplication, Vedic multiplication using HCA with BEC module and hybrid multiplier, respectively.

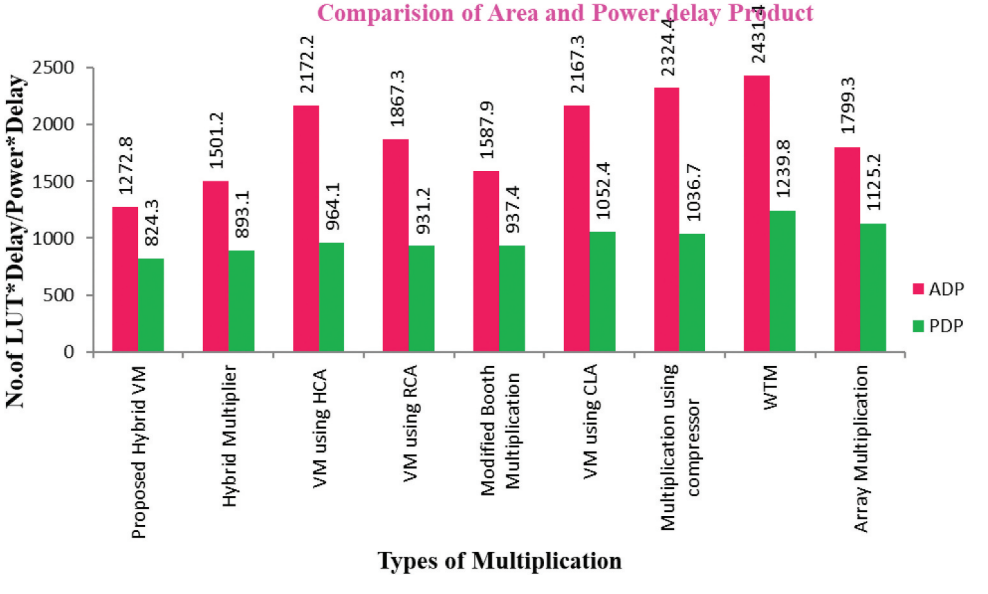

Figure 9. Comparisons of ADP and PDP of several multiplications.

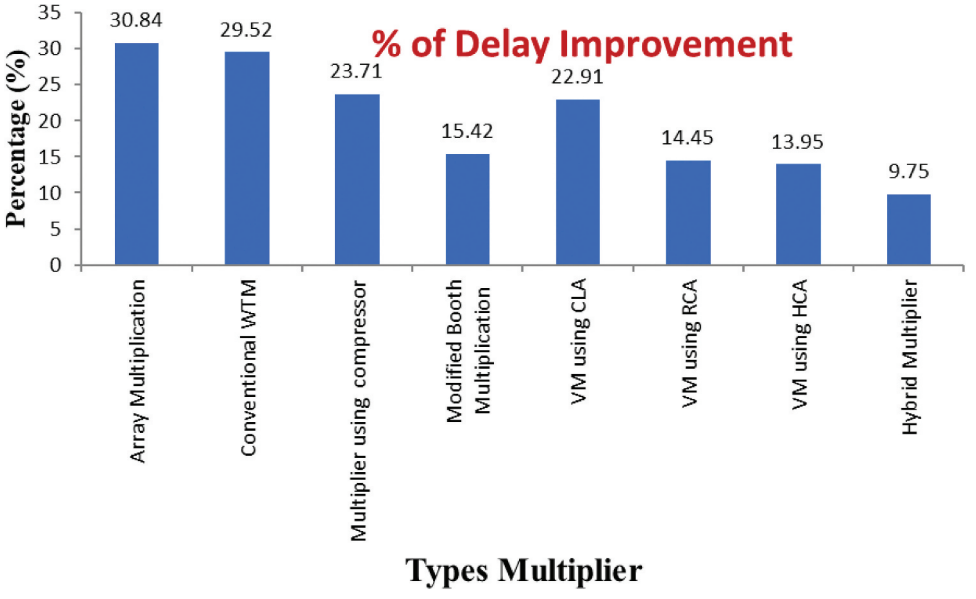

Figure 10. Delay improvement (%) of proposed hybrid Vedic multiplier as compared to other multipliers.

Table 4. Delay improvement (%) as compared to other multiplication techniques.

S. No.	Proposed Hybrid Vedic Multiplication as Compared To	Spartan 6 FPGA
1.	Conventional Array Multiplication	30.84
2.	Conventional Wallace Tree Multiplication	29.52
3.	Multiplier Based on Compressor	23.71
4.	Modified Booth Multiplication	15.42
5.	Vedic Multiplication Using Carry Look-ahead Addition	22.91
6.	Vedic Multiplication Using Ripple Carry Addition	14.45
7.	Vedic Multiplication Using Han-Carlson with BEC	13.95
8.	Hybrid Multiplier	09.75

Table 5. Comparison of 8×8 multiplication.

S. No.	8×8 Multiplication	Delay (ns)
1.	Hybrid Vedic multiplier	14.80
2.	Hybrid multiplier (Thamizharasan & Kasthuri, 2021)	16.68
3.	Modified Vedic multiplier Design I (Sivanandam & Kumar, 2019)	18.615
4.	Modified Vedic multiplier Design II (Sivanandam & Kumar, 2019)	18.39
5.	Modified Binary Multiplication (Shamim & Saurabh, 2019)	18.46
6.	High Performance Multiplier (Hussain et al., 2019)	20.7
7.	High Speed Vedic Multiplication (Inamul et al., 2014)	23.644

Figure 9 shows the power delay product and area delay product of various multipliers. The proposed multiplier has significant improvements in power delay product and area delay product.

A comparison chart for delay improvement percentage of the proposed hybrid Vedic multiplier as compared to other recent existing multiplication techniques is shown in Figure 10.

A comparison of the recent existing multipliers of various research articles is displayed in Table 5 with various performance parameters in FPGA implementation. From this table, it is observed that critical path delay is improved in the proposed hybrid Vedic multiplier as compared to conventional and existing techniques.

6. Concusion

In this research, a hybrid Vedic multiplication is proposed using a hybrid carry select adder (BEC, Han-Carlson adder and multiplexer). The critical path delays of hybrid 4×4 Vedic multiplier are the summation of 2×2 Vedic multiplier, two full adders, two multiplexers (4:1) and two BECs (3 bit) for generating the final product. The proposed work indicated that the hybrid Vedic multiplier operated at high speed with reduced area than the conventional Vedic multiplier. The simulation is done by XILINX ISE 14.1 using Verilog HDL and implemented in Spartan 6 FPGA. The implementation results show that the speed of the proposed multiplication is ameliorated 30.84%, 29.52%, 23.71%, 22.91%, 14.45%, 15.42%, 13.95% and 11.37% as compared to array multiplication, Wallace tree multiplication, multiplication based on compressor, Vedic multiplication based on carry look-ahead adder, Vedic multiplication using ripple carry adder, improved booth multiplication, Vedic multiplication using HCA with BEC module and hybrid multiplier, respectively. This work can be further applied to high-speed signal (Liacha et al., 2018), image processing (Radhakrishnan & Themozhi, 2020) and cryptography applications.

Disclosure statement

No potential conflict of interest was reported by the author(s).

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