Proceedings of the International Conference on Multi-Agent Systems for Collaborative Intelligence (ICMSCI-2025)
IEEE Xplore Part Number: CFP25VH0-ART; ISBN: 979-8-3315-0982-8

Nine Level Double Boost Inverter with Modified PWM Control

C.Ramakrishnan
Department of Electrical and Electronics Engineering,
SNS College of Technology, Coimbatore-641035, Tamilnadu, India
ramramki.krishnan@gmail.com

Gobi Mohan Sivasubramanian
Engineering Department,
College of Engineering and Technology, University of Technology and Applied Sciences, Nizwa. OMAN,
sgm2kx@gmail.com

P.Veena
Department of EEE,
K.S.R. College of Engineering, Tiruchengode-637215,
Tamil Nadu, India,
veena_gce@yahoo.co.in

P. Karuppusamy
Department of EEE,
Erode Sengunthar Engineering College, Erode, Tamilnadu,India.
eee_k1983@yahoo.co.in

Arun V
Department of Electrical and Electronics Engineering
Mohan Babu University,
Tirupati, India
varunpse@yahoo.com

Karthikeyan N
Department of ECE,
Velalar College of Engineering and Technology
Erode - 638012, India
florakarth1988@gmail.com

***Abstract*— The switched capacitor topology has become more prevalent in multilevel inverters in recent years. Without the need for additional voltage sources, the structure generates the necessary voltage levels through the distribution of voltage across the capacitors. The purpose of this article is to employ a single DC input to produce a double-boost inverter containing nine voltage levels. In comparison to traditional inverter topologies, the article provides a nine-level double boost inverter (NDBI) design that employs less capacitors, switches, and diodes. Furthermore, the NDBI's capacitors are self-balancing. The output waveform quality of switching pulses for NDBI is enhanced through the use of variable frequency Alternative Phase Opposition Disposition (VF-APOD) approaches. A comprehensive evaluation of the performance of the proposed configuration at different modulation indices is provided by the study's MATLAB/SIMULINK simulation findings.**

***Keywords*—MLI, NDBI, PWM, THD, VF-APOD.**

I. INTRODUCTION

In [1] presents a pioneering and effective method of pulse width modulation (PWM) in power converters. It proposed [2] the 9-level Reduced Switch Asymmetrical Cascaded H-Bridge Multi-Level Inverter designed to address challenges prevalent in MLIs. Common issues, such as elevated Total Harmonic Distortions (THD) with higher switching losses and lower voltage levels due to a surplus of switches, are specifically targeted. The proposed system is structured with a reduced device inverter technology [3]. The presented configuration [4] indicates a single-phase grid-connected Multi-Level Inverter topology crafted to incorporate renewable energy sources into the utility grid [5-8]. The principal aim of the suggested inverter is to surmount the constraints linked with traditional MLIs [9]. Particularly the production of output sinusoidal waveforms. The inception and verification of an innovative Multi-Level Inverter hierarchy in a single phase. Modified inverters with reduced blocking voltage (BV) are presented in [10]. This presents a novel control concept to produce modulation patterns tailored for inverters. This strategy streamlines the synchronization of carrier signals, effectively tackling issues associated with sampling complications, memory limitations, and computational delays in the real-time digital implementation process described in [11]. In [12] proposed topology is meticulously crafted to address the elevated voltage stress encountered by switches in the second stage, a common drawback observed in traditional two-stage exchanged capacitor-based inverters. The proposal brings forth an innovative multi-level inverter design founded on a switched capacitor approach, facilitating the generation of multi-level distinct in the inverter. These levels are attained through the interconnected arrangement of switched capacitor cells, presenting a clear, uncomplicated, and easily implementable structural framework demonstrated in [13]. In [14] delves into the examination and assessment of a more appropriate multi-level inverter model with fault-tolerant features. A meticulous comparative analysis is carried out, drawing a precise evaluation between the proposed multi-level inverter It is dedicated to the design of a Multilevel Inverter (MLI) technology, utilizing a pulse width modulation strategy. The proposed method involves the use of lower switches to control the fundamental and carrier frequencies within the multilevel inverter presented in [15]. This presents a thorough exploration into enhancing power quality through multilevel inverters, specifically concentrating on applications with low and medium power requirements [16-18]. The primary objective is evaluating the effectiveness of Harmonic mitigation using a variety of multi-carrier PWM techniques in an asymmetric multilevel inverter demonstrated in [19]. Emphasizing the advantages of a multi-level inverter in enhancing efficiency, the study specifically delves into the loss characteristics inherent to the machine type proposed in [20]. In [21] intricately explores and examines a modular multilevel inverter, emphasizing the enhancement of performance, power quality, and the optimization of component count. The novel introducing the hybrid control technique aims to improve the performance of a multilevel inverter. This explores the performance assessment of integrated with a multilevel inverter [22-24]. It highlights the robust characteristics, high torque capabilities, and versatile applications of the Induction Motor, positioning it as a compelling choice for diverse control mechanisms described in [25, 26].

From the above literature, the paper proposed a novel nine-level double boost inverter (NDBI) which includes 1 input source and fewer components with VF-APOD PWM technique to achieve double boost 9-level resultant voltage.

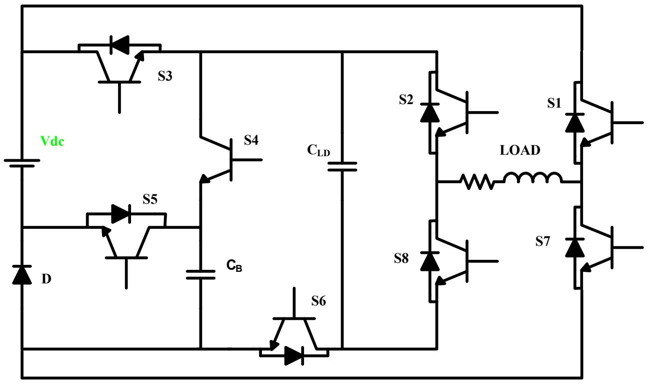


Fig. 1 Circuit topology of NDBI

II. Proposed Nine-Level Switched Capacitor Inverter

In the proposed nine-level inverter configuration depicted in Fig. 1, a singular DC source is employed, showcasing a hybrid circuit design that incorporates both a flying capacitor and a switched capacitor. This innovative arrangement utilizes capacitor CB to enhance the output voltage and capacitor CLD to effectively Increase the output levels by twice. Remarkably, the nine-level inverter design presents a total of nine distinct voltage levels (±2Vdc, ±1.5Vdc, ±1Vdc, ±0.5Vdc, and zero) utilizing just eight switches. Notably, two switches only are subjected to a 2 Vdc maximum voltage. The CB and CLD capacitors are charged to Vdc and 0.5Vdc, correspondingly. The charging and discharging process of capacitor CB employs a series-parallel method, obviating the need for an additional voltage balancing technique. In contrast, capacitor CLD undergoes discharge during the output voltage waveform's half-cycle that is positive and charge during the half-cycle in negative. Consequently, the technique used to generate the required output voltage levels is sensorless control, ensuring a sophisticated and efficient operation of the proposed nine-level inverter circuit.

TABLE I. Output Level And Corresponding States Of Switches

O/P Level* Vdc	S1	S2	S3	S4	S5	S6	S7	S8	CB	CLD
+2	1	0	0	0	1	1	0	1	D	-
+1.5	1	0	0	1	1	0	0	1	-	D
+1	1	0	0	0	0	1	0	1	-	-
+0.5	1	0	1	1	0	0	0	1	C	D
0	1	1	1	0	0	0	0	0	-	-
-0.5	0	0	1	1	0	0	1	1	C	C
-1	0	1	1	1	0	0	1	0	C	-
-1.5	0	0	1	0	1	0	1	1	D	C
-2	0	1	1	0	1	0	1	0	D	-

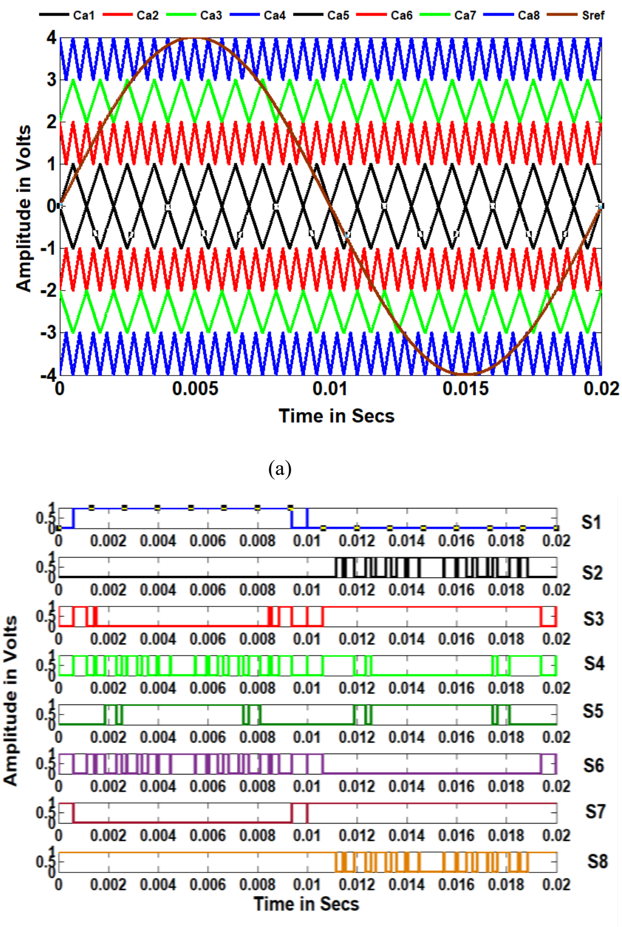
Table I provides a comprehensive enumeration of the distinct switching modes linked to the states of charge and discharge for capacitors within the suggested nine-level inverter converter. In this context, the corresponding switch's ON and OFF states are indicated by the submissions "1" and "0". Additionally, the symbols "D," "C," and "−" indicate a capacitor's discharging, charging, and no-effect states, respectively.

III. VF-APODPWM Technique

The proposed approach employs a bipolar sine reference in tandem with a triangular carrier to generate triggering signals for an inverter. In the context of an m-level inverter, (m-1) carriers with distinct frequencies (fc1 & fc2) and an identical magnitude carrier, denoted as Ac, are utilized. The amplitude of the modulating waveform is represented by Am, with a zero-frequency denoted as fm. Continuous comparisons are conducted between each carrier signal and the reference wave. Whenever a reference wave surpasses the magnitude of a carrier signal, all switches associated with that carrier are activated [27]. In such instances, the primary pulses are produced.

Numerous alternative approaches are available, and this paper delves into the exploration of a VF-APOD for a comprehensive investigation.

In the VF-APOD technique, carriers of identical amplitude are strategically arranged, each carrier positioned 180 degrees apart from the carrier next to it. This organization is consistently maintained in the VF-APOD technique, as illustrated in Figure 2.



(a)

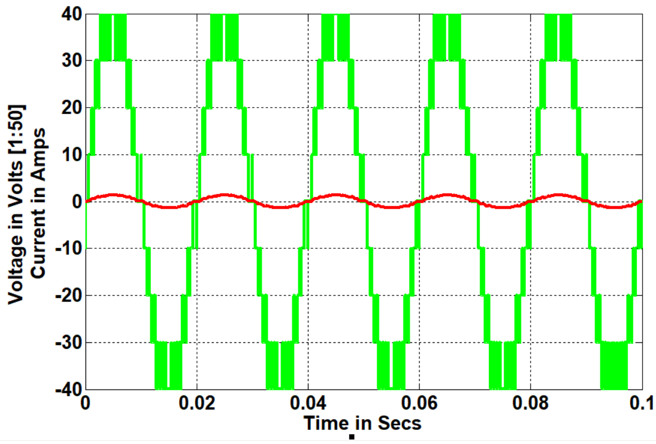
(b)

Fig. 2 Use of the VF-APOD Technique for the proposed topology (b) Multi-Carrier Waveform (c) Pulse Waveform

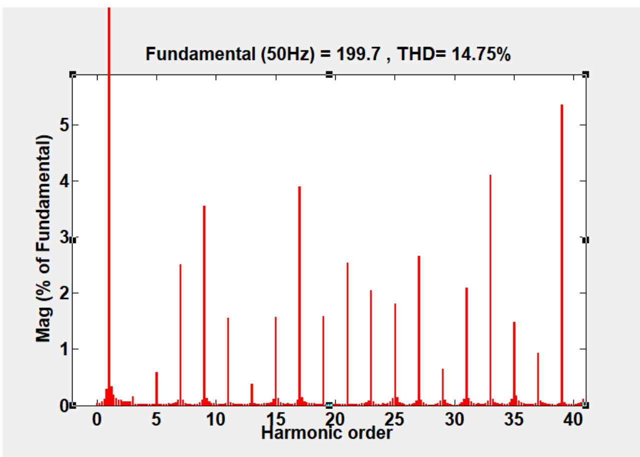
IV. SIMULATION RESULT

Performing the essential verification of the NDBI configuration using the VF-APOD method and conducting simulations in MATLAB/SIMULINK is a pivotal undertaking. The nine-level waveform that resulted is characterized by voltages of 0, ±50V, ±100V, ±150V and ±200V. In this simulation study, the given parameters consist of V=100Vdc and an RL load of 150 ohms. Figures 3(a)-(c) depict the NDBI generating a 9-level waveform with accompanying harmonic spectra at a 1 for the modulation index (MI). The voltage waveform that is produced has a maximum fundamental voltage of 199.7V and a Total Harmonic Distortion (THD) of 14.75%. Dominant harmonic orders are observed at the 21st, 33rd, and 41st positions.

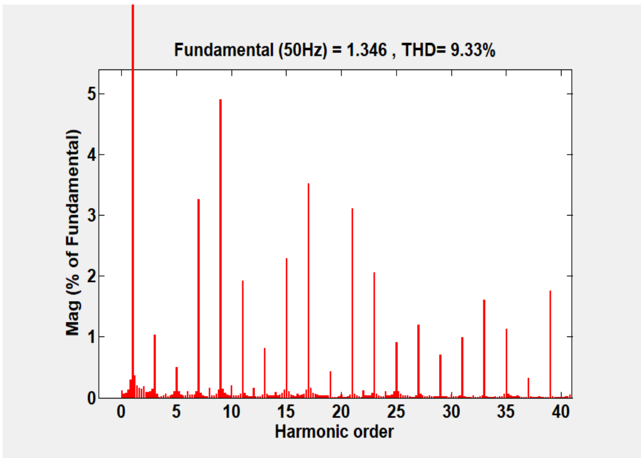
Transitioning to Figs. 4(a)- (c) for MI 0.95, the NDBI waveform and spectral response display a peak voltage magnitude of 189V and a THD of 16.79%. The 21st, 33rd, and 41st harmonic orders remain prominent. Figures 5(a)- (c) illustrate NDBI outcomes for MI 0.9, achieving a maximum fundamental voltage of 178.7V with a THD of 17.09%. Notably, the 33rd and 41st harmonics dominate. Continuing to Figs. 6(a)-(c) for MI 0.85, the NDBI generates a peak voltage of 169.4V with a THD of 15.85%, emphasizing the dominance of the 33rd and 41st harmonic orders. Finally, Figs .7(a) –(c) showcase results for MI 0.8, revealing a peak voltage amplitude of 159.1V and a THD of 16.72%. Once again, the 33rd and 41st harmonics take precedence.



(a)

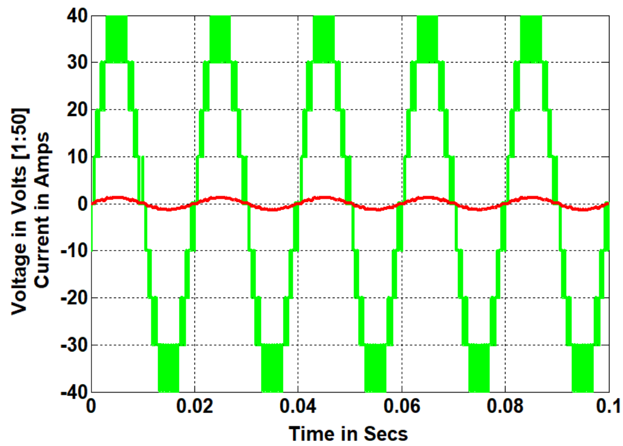


(b)

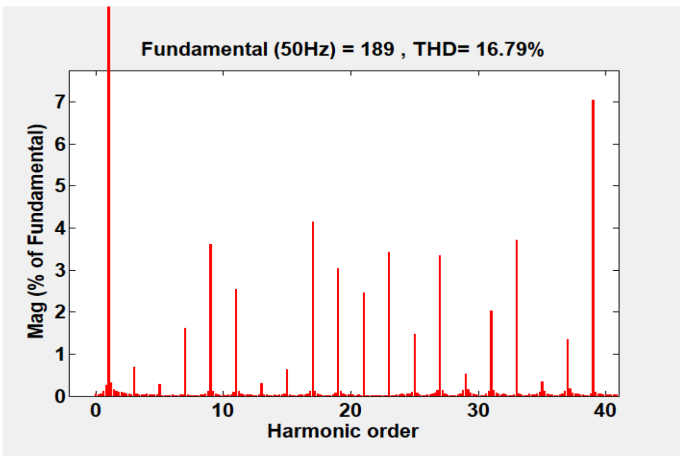


(c)

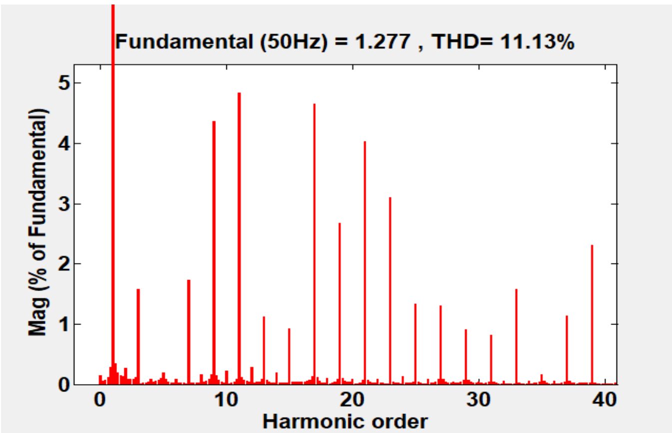
Fig 3. (a) Waveform of the current and output voltage (b) FFT analysis for the voltage (c) FFT Analysis for the current(with modulation index 1)



(a)

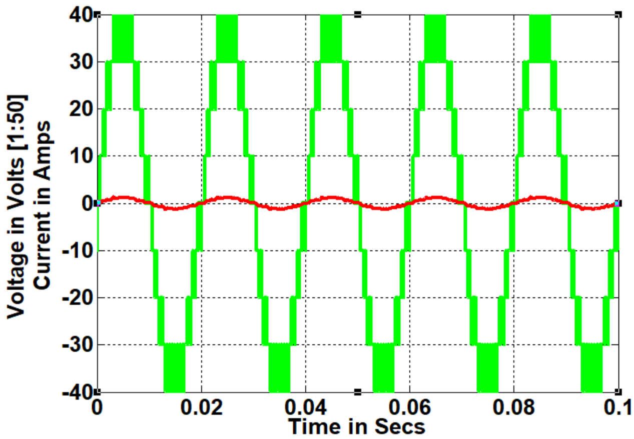


(b)

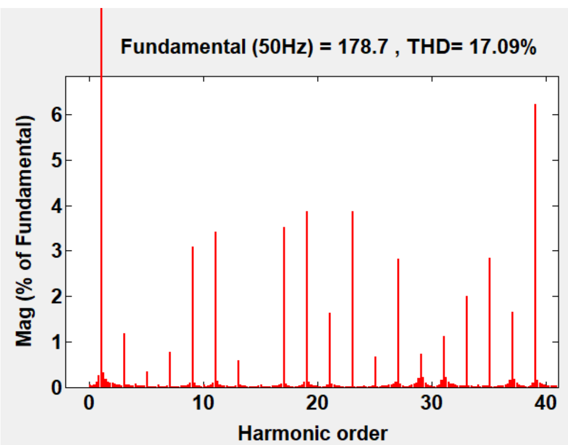


(c)

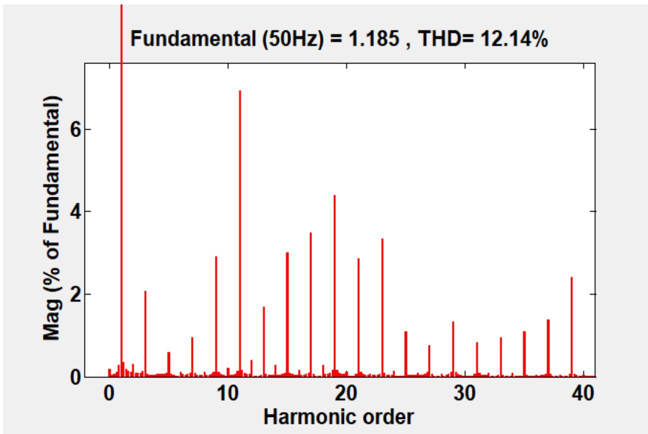
Fig 4. (a) Waveform of the current and output voltage (b) FFT analysis for the voltage (c)FFT Analysis for the current(with modulation index 0.95)



(a)

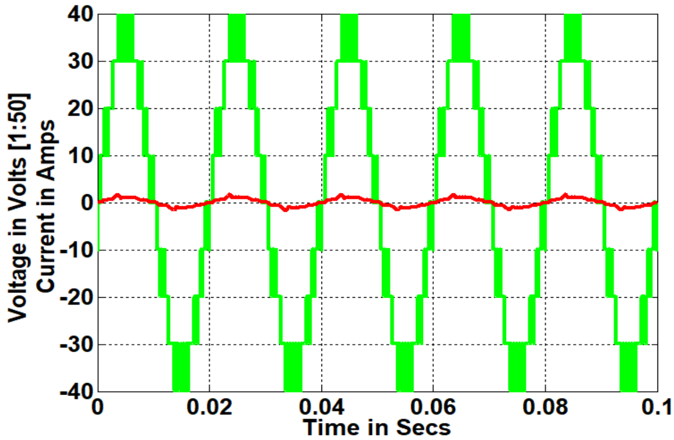


(b)

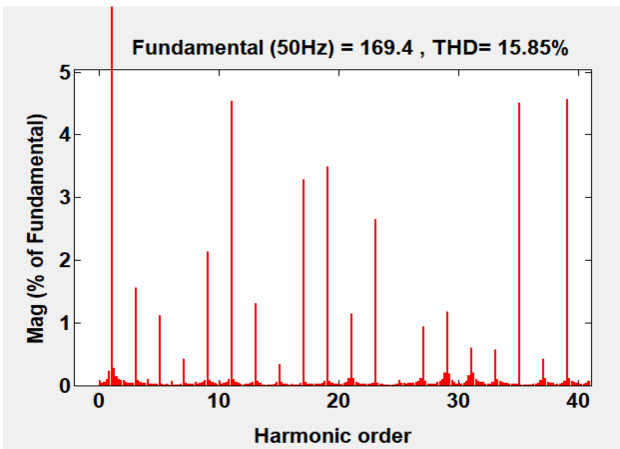


(c)

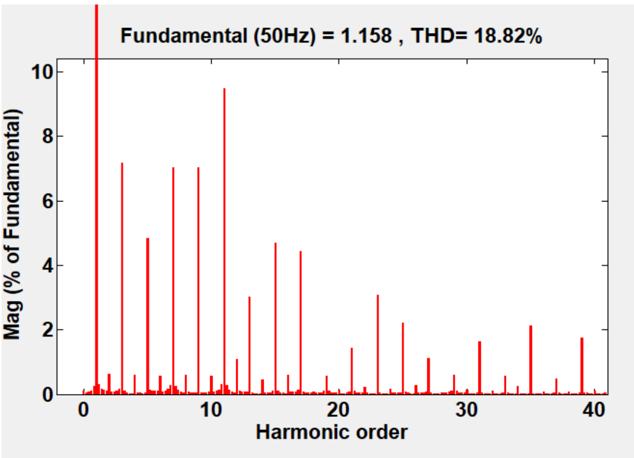
Fig 5. (a)Waveform of the current and output voltage (b) FFT analysis for the voltage (c) FFT Analysis for the current(with modulation index 0.9)



(a)

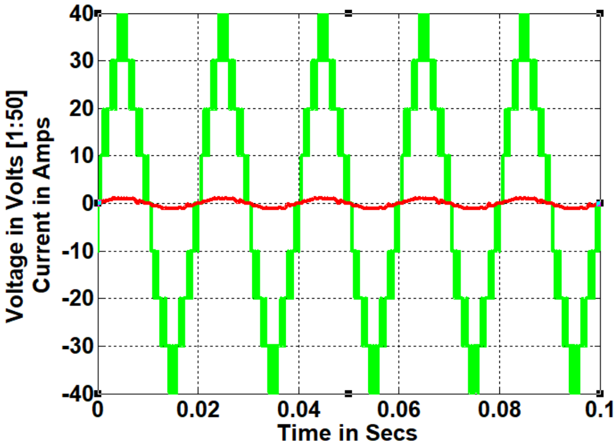


(b)

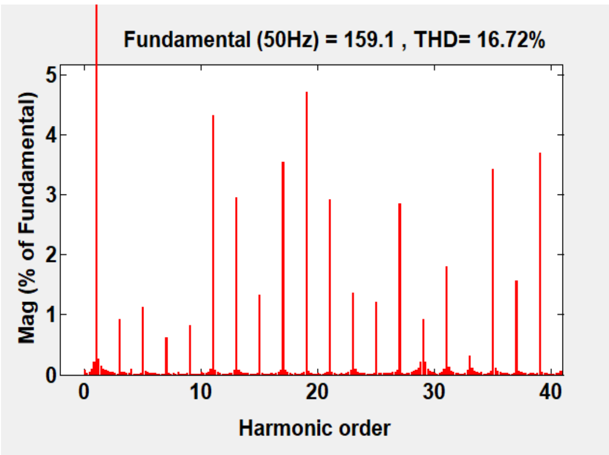


(c)

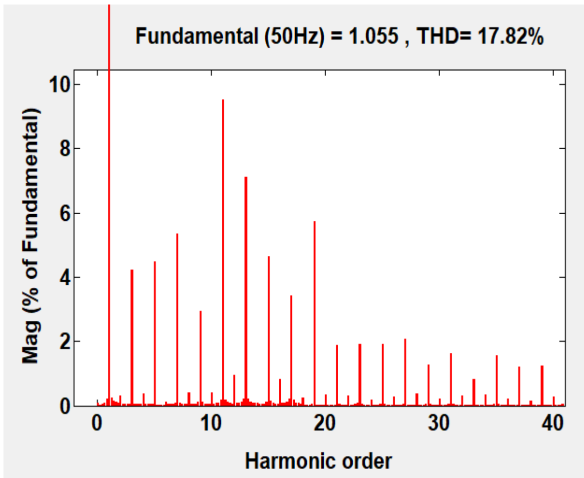
Fig 6. (a)Waveform of the current and output voltage (b) FFT analysis for the voltage(c) FFT Analysis for the current(with modulation index 0.85)



(a)



(b)



(c)

Fig 7. (a)Waveform of the current and output voltage (b) FFT analysis for the voltage (c) FFT Analysis for the current(with modulation index 0.8)

TABLE II. CALCULATING VARIOUS PARAMETERS FOR A VARIETY OF MODULATION INDICES FOR THE CURRENT LOAD OF VF-APOD

Ma	%THD$_I$	I_{rms}	I_{peak}	DC COM.	DOMINANT HARMONICS (>=3%) Hertz
1	9.33	0.952	1.346	0.001521	350(h7) 850(h17) 1050(h21)
0.95	11.13	0.903	1.277	0.001738	1150(h23)
0.9	12.14	0.837	1.185	0.002016	750(h15) 850(h17) 1150(h23)
0.85	18.82	0.818	1.158	0.001031	1150(h23)
0.8	17.82	0.746	1.055	0.0007591	850(h17)

TABLE III. CALCULATING VARIOUS PARAMETERS FOR A VARIETY OF MODULATION INDICES FOR THE VOLTAGE LOAD OF VF-APOD

Ma	%THD$_V$	V_{rms}	V_{peak}	DC COM.	DOMINATION HARMONICS (>=3%)
1	14.75	141.2	199.7	0.08211	450(h9) 850(h17)
0.95	16.79	133.6	189	0.0948	450(h9) 950(h19) 1150(h23) 1350(h27) 1650(h33)
0.9	17.09	126.3	178.7	0.1037	450(h9) 550(h11) 850(h17) 950(h19) 0.2(h23)
0.85	15.85	119.8	169.4	0.1234	850(h17) 950(h19)
0.8	16.72	112.5	159.1	0.1172	850(h17) 1750(h35) 1950(h39)

V. CONCLUSION

The presented nine-level double boost inverter offers a thorough circuit description and operating principle. This investigation introduces tailored VF-APODPWM strategies for an NDBI. The design of the NDBI aims to enhance the output voltage while concurrently minimizing the count of switches and the generation of harmonics. Various performance metrics, encompassing RMS, PEAK, Total Harmonic Distortion Values of Voltage and Current, and Dominant Harmonics, have been comprehensively examined, presented, and analyzed. The study emphasizes that the VF-APODPWM approach results in a significant decrease in the percentage of the total harmonic distortion (THD). Exactly, the VF-APODPWM technique with Modulation index 1 provides THD_V of 14.75% and THD_I of 9.33%. The simulation outcomes vividly illustrate the overall performance enhancement achieved through this approach.

REFERENCES

[1] V. Madhaiyan et al., "Nine Switch Dual Input 9- Level Inverter (NSDI9LI) with Inherent AC Voltage Generation Ability," *2023 First International Conference on Advances in Electrical, Electronics and Computational Intelligence (ICAEECI), Tiruchengode, India*, 2023, pp. 1-5, doi: 10.1109/ICAEECI58247.2023.10370814.

[2] V. Arun, A. etal., "Advanced PWM Scheme For 15 Level Binary Source (1:2:4) Inverter," *2023 9th International Conference on Electrical Energy Systems (ICEES)*, Chennai, India, 2023, pp. 408-412, doi: 10.1109/ICEES57979.2023.10110078.

[3] V. Madhaiyan et al., "Sixty Degree PWM Controlled 7-Level Inverter Utilizing Binary Input," *2023 First International Conference on Advances in Electrical, Electronics and Computational Intelligence (ICAEECI)*, Tiruchengode, India, 2023, pp. 1-7, doi: 10.1109/ICAEECI58247.2023.10370833.

[4] V. Arun et al.,"Design of Novel Structure Nine Level Trinary Source Inverter," 2023 *9th International Conference on Electrical Energy Systems (ICEES),* Chennai, India, 2023, pp. 175-178, doi: 10.1109/ICEES57979.2023.10110112.

[5] Ramesh et al., "Evaluating the Effectiveness of the TAR Pulse Width Modulation Strategy for a 7-Level Inverter with Non-Uniform Source Voltages," 2023 First International Conference on Advances in Electrical, Electronics and Computational Intelligence (ICAEECI), Tiruchengode, India, 2023, pp. 1-6, doi: 10.1109/ICAEECI58247.2023.10370857.

[6] Raja et al., Solar Photovoltaic Interconnected ZSI-Unified Power Quality Conditioner to Enhance Power Quality. Bull. Pol. Acad. Sci. Tech. Sci. 2022, 70, e140015, DOI: 10.24425/bpasts.2022.140015.

[7] Kanagaraj et al., "Energy Management and Power Quality Improvement of Hybrid Renewable Energy Generation System Using Coordinated Control Scheme," in IEEE Access, vol. 11, pp. 93254-93267, 2023, doi: 10.1109/ACCESS.2023.3299035.

[8] M. Vijayakumar and S. Vijayan, "PV based three-level NPC shunt active power filter with extended reference current generation method", Int. J. Electr. Energy, vol. 2, no. 4, pp. 258-267, 2014.

[9] V. Madhaiyan, R. Murugesan, S. Sengottaiyan, V. Muniyan, A. Vijayakumar and P. Sundaramoorthy, "Analysis of Performance for Multilevel Inverters Utilizing Different Pulse Width Modulation Techniques," 2023 First International Conference on Advances in Electrical, Electronics and Computational Intelligence (ICAEECI), Tiruchengode, India, 2023, pp. 1-7, doi: 10.1109/ICAEECI58247.2023.10370780.

[10] S. Prabhu et al., "Electromagnetic Analysis on Interior Permanent Magnet Motor for Electrified Transportation Systems," *2023 9th International Conference on Electrical Energy Systems (ICEES)*, Chennai, India, 2023, pp. 163-168, doi: 10.1109/ICEES57979.2023.10110040.

[11] S. Iderus et al., "Performance Evolution of Switched Capacitor Boost Nine Level Inverter with Variable Frequency APOD Technique," *2024 International Conference on E-mobility, Power Control and Smart Systems (ICEMPS)*, Thiruvananthapuram, India, 2024, pp. 1-6, doi: 10.1109/ICEMPS60684.2024.10559329.

[12] V. Arun and N. Prabaharan, "Induction Motor Drive with Trinary DC Source Asymmetrical Inverter," *International Journal of Recent Technology and Engineering*, vol. 8, no. 2, pp. 5484-5490, 2019. DOI: 10.35940/ijrte.B2527.078219

[13] K. Likhitha et al., "Modular Seven Level Inverter (M7LI) with Level Shifted Variable Frequency Control," *2023 9th International Conference on Electrical Energy Systems (ICEES)*, Chennai, India, 2023, pp. 509-513, doi: 10.1109/ICEES57979.2023.10110094.

[14] V. Arun et al., "Modified Structure 9-Level Inverter (MS9LI) With Reduced On-State Switches," in *IEEE Canadian Journal of Electrical and Computer Engineering*, vol. 46, no. 1, pp. 15-23, winter 2023, doi: 10.1109/ICJECE.2022.3222215

[15] V. Arun et al.“A hybrid reference pulse width modulation technique for binary source multilevel inverter,” International Journal of Power Electronics and Drive Systems vol. 13, no. 2, p. 980, Jun. 2022, doi: 10.11591/ijpeds.v13.i2.pp980-987.

[16] Madhaiyan, V., and Subramaniam, V., “Experimental verification of photovoltaic-based three-phase four-wire series hybrid active power filter,” Electr. Power Compon. Syst., Vol. 42, No. 13, pp. 1356–1370, 2014.

[17] Vijayakumar M. and Vijayan S., “Photovoltaic Based Three-Phase Four-Wire Series Hybrid Active Power Filter for Power Quality Improvement,” Indian Journal of Engineering and Materials Science 21, no. 4 (August 2014): 358–370.

[18] Parthiban, S., & Madhaiyan, V. (2021). Experimental validation of solar PV sustained ZSI based unified active power filter for enrichment of power quality. Automatika, 62(1), 137–153. https://doi.org/10.1080/00051144.2021.1908013.

[19] N. Prabaharan et al., “Reconfiguration of a Multilevel Inverter with Trapezoidal Pulse Width Modulation,” *Energies*, vol. 11, no. 8, p. 2148, Aug. 2018, doi: 10.3390/en11082148.

[20] N. Prabaharan et al., "Analysis Of Symmetric Multilevel Inverter Using Unipolar Pulse Width Modulation For Photovoltaic Application", *Comptes rendus de l'Acad'emie bulgare des Sciences*, vol. 71, no. 2, pp. 252-260, 2018.

[21] A. Vijayakumar, et al., “Dual source novel nine level inverter (DSN2LI) design with minimum active devices and inherent polarity generation,” *IET Power Electronics*, Jun. 2023, doi: 10.1049/pel2.12533

[22] Kanagaraj et al., "Energy Management and Power Quality Improvement of Hybrid Renewable Energy Generation System Using Coordinated Control Scheme," in IEEE Access, vol. 11, pp. 93254-93267, 2023, doi: 10.1109/ACCESS.2023.3299035.

[23] K. N, R. M, V. M and O. Aldosari, "Design of an Extendable High Boost Multi-Port Z-Network Converter for Small Power Grid-Connected PV Applications," in IEEE Open Journal of Power Electronics, vol. 5, pp. 534-553, 2024, doi: 10.1109/OJPEL.2024.3386023.

[24] Nallaiyagounder, K.; Madhaiyan, V.; Murugesan, R.; Aldosari, O. 2024. "Photovoltaic-Based q-ZSI STATCOM with MDNESOGI Control Scheme for Mitigation of Harmonics" Energies, vol. 17, no. 2: 534. https://doi.org/10.3390/en17020534

[25] S. Iderus et al.,"Performance of Modified Structure Asymmetrical Multilevel Inverter with Multicarrier PWM Control Strategies," *2023 5th International Conference on Inventive Research in Computing Applications (ICIRCA)*, Coimbatore, India, 2023, pp. 1846-1851, doi: 10.1109/ICIRCA57980.2023.10220770.

[26] A.Vijayakumar, et al., “ Power quality enhancement in asymmetrical cascaded multilevel inverter using modified carrier level shifted pulse width modulation approach:, *IET Power Electron*. 00, pp. 1–13 , 2022) https://doi.org/10.1049/pel2.12429

[27] Vijayakumar M, Vijayan S. A comparative study and implementation of controller for UPQC in single-phase to three-phase system. Int J Eng Tech. 2013;5:3846–3857.