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A Low Noise Switched Dynamic Comparator with Offset Calibration for High-Speed Applications in 45 and 65nm Technology

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Abstract

A Low noise, high speed, low input capacitance Switched Dynamic Comparator(SDC) for high speed application in 45nm and 65nm is presented in this paper. The comparator design occupies less area and consumes lesser power is suitable for the input stage of a Flash ADC. The proposed dynamic comparator eliminates the stacking issue related with the convention comparator and reduces the offset noise further. The need for low noise, low-power, area efficient, and high speed flash ADCs required in many application today made the work to progress in designing a comparator for analog-to-digital converter. In this paper, the analysis and design of new dynamic comparator is proposed, where the circuit of a conventional switched doubletail comparator is modified. The regenerative feedback is strengthened to reduce the delay time. The rail to rail output swing is also improved. The input capacitance is reduced by using shared first stage technique. The comparator is designed with constant Id/gm biasing to suppress the environmental drift. The simulation results in a 45nm and 65nm CMOS technology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced. The maximum clock frequency of the proposed comparator can be increased to 3.5 and 2.2 GHz at supply voltages of 1 and 0.6 V. The simulation is carried out using predictive technology model for 45nm and 65nm in HSPICE.

Keywords: Double-tail comparator, Switched dynamic clocked comparator, low noise, stacking, CMOS technology, Flash ADC.

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Introduction

In flash ADCs Comparators is the basic building block which transfers the differences of the input voltage and reference voltage to the next stage. The design of the comparators should meet the requirements based on the applications. In biomedical applications where data acquisition units are present the comparators should be fast and less noise. They should provide sufficient gain to the difference of inputs. Nowadays latched comparators play vital roles in all ADCs due to the controllability through a clock signal. But the features like high speed, low offset voltage, huge output swing made dynamic comparators to be dominant in the field. This work focuses to design a Dynamic Comparator with less noise for the flash ADC used in System On Chip application. A vast survey is made on different comparators. In literature several comparators are designed and utilized. Masaya Miyahara *et al.,* [1] proposed a low offset voltage, low noise dynamic latched comparator using a self-calibrating technique. The method eliminates the use of amplifiers. The reported offset voltage measured is 1.69mv without calibration. In compared to relaxation comparators this circuit uses only one phase clock against the formers two phase clocks. But above 250MHZ the power dissipation increases.

Jun He *et al.,* [2] analyzed the random offset voltage in static and dynamic comparators. The reported offset sources of noise are the internal positive feedback and transient response. As the gain and CMRR are referred to the input the random output noise is a function of gain and input-referred random offset voltages. The input referred noise depends on the operating points of transistors which are time varying. The authors analyze the operating point using balanced method using explicit expression for offset voltage which are due to static offset voltages from the mismatch of transistor parameters, threshold voltage and mismatch in the parasitic capacitances. The proposed topology for offset analysis reduces the offset by 41% after the optimization while maintaining the same silicon area. A lower setup + hold time is reported by Daniel Schinkel *et al.,* [3] in the design of a double tail latch type voltage sense amplifier. The reported design provides better optimization in speed, offset, power and common mode voltage. Due to better isolation between the input and output the design provides lower offset voltages.

Heung Jun Jeon and Yong-Bin Kim [4] presented a novel dynamic latched comparator with lower offset voltage. The reported design provides higher driving capacity when compared to the conventional dynamic comparators. The work is focused on the improvement in the regenerative latch stage with two additional inverters inserted between the input- and output-stage of the conventional double-tail dynamic comparator. The work was done in 90nm CMOS technology and a 19% less offset voltage is reported maintaining the same area and power consumption. A clocked low power comparator is reported in the literature [5]. A dynamic latch comparator with high speed and low power is presented in the literature [6]. Noises are important issues in comparators [7]. Pedro M. Figueiredo and Joao C. Vital [8] presented a existing solutions to minimize the noises present in the latched comparator. The demonstration was done using 180nm CMOS technology. Two methodologies were proposed for the removal of noise based on sampling switches and asynchronous reset. The understanding of the comparator towards its amplification and noise removal is one of the problems addressed in literature [9]. A high precision comparator with tuned offset cancellation was proposed in literature [10] by Junjie Lu and Jeremy Holleman. The reported time domain based bulk tuned offset cancellation technique reduces the input-referred noise. For the noise removal additional power is consumed. A similar analysis of comparator with respect to noise is presented by Chi Hang Chan *et al.,* [11].

Mohamed Abbas *et al.,* [12] in their work proposed a clocked comparator in 65nm technology for high speed on-chip application. The comparator has only 10 transistors having amplification and regenerative stages. The less number of transistors helps the design to work fast but the offset cancellation is not taken care in the design. A comparator is designed with minimum delay in 65nm CMOS by Bernhard Goll and Horst Zimmermann [13] working with a supply voltage below 0.65V. Chung Hsun Huang *et al.,* [14] proposed a priority encoder based high-Performance and Power-Efficient CMOS Comparator featuring multiple output domino logic. The paper presents a post-format recreation result demonstrating a 64-b comparator. The proposed work is implemented in a 3-V 0.6-m CMOS technology and is 16% quicker, half littler, and 79% more power proficient. Y. Jung *et al.,* [15] proposed a low-power and low-balance hooked comparator utilizing dynamic balance cancelation and a lock burden. In most of the ADCs the offset values are so troublesome which needs a comparator of less offset. For a 7-bit, 1.4 GS/s ADC Yuji Nakajima *et al.,* [16] proposed a Offset Drift Suppression Technique. The ratio between the transconductance and drain current is kept constant to suppress the offset drift. A bulk driven based dynamic comparator is been proposed in [17] which reduces the threshold voltage. The comparator is designed using a preamplifier and latch. The problem with the design is the proper transistor sizing is required else it will lead to offset errors in the input stage. Samaneh Babayan *et al.,* [18] have proposed a Low-Voltage Low-Power Double-Tail Comparator utilizing the regenerative principle and current boosting. The authors investigated the comparator delay and the tradeoffs in element comparator outline. In addition the paper proposes a traditional double tail comparator for low-power and quick operation even in little supply voltages. The reported post-format reproduction results in a 0.18-µm CMOS innovation affirm the examination results.

A switched dynamic comparator is proposed by Yongsheng Xu *et al.,* [19] which eliminates the limitation on the maximum operating speed due to regeneration time. The design consists of a dynamic amplification stage with a NAND gate for switching operation. Only one extra transistor is used in this proposed design. In [20] the corruption of input signal by large kickback noise is addressed by Stefano D'Amico st al. The increase in the size of transistors will reduce the kickback noise but increases the large parasitic capacitances. The proposed double tail comparator presents a fixed bias current in the first stage eliminating the kickback noise. Sebastian Zeller *et al.,* [21] proposed a dynamic latched comparator with complementary input stage for large input common-mode range and short decision time at small differential input voltages. The work reported presents that there are no static currents and all internal nodes are discharged during the low clock phase to avoid offset that depends on previous decisions. Daiguo Xu *et al.,* [22] proposed an element comparator which works in lower voltage and rapid low-power.

Clocked Regenerative Comparators

Clocked regenerative comparators are used in high speed ADCs due to its advantages of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch. Due to the strong positive feedback the decision making is done so fast. The comparator is normally implemented using CMOS technology. The comparator is used in circuits where speed requirement are higher. But the mismatches between the transistors and circuit parameter deviations leads to large input offset current. The large input offset current limits the resolution to about 5b. The offset voltage can be overcome by preceding the dynamic latch using linear amplidier. This can increase the feasibility of medium resolution comparators (8bits). The offset can be reduced by designing the comparator with differential input stage. This paper discusses the

detailed analysis of 4 existing comparators. The dynamic behavior of the CMOS latch is presented and a technique to reduce the input-referred offset is proposed. In recent years, several dynamic comparators have been widely employed in ADCs offer high operating speed while consuming no static power.

Conventional Dynamic Comparator (CDC)

The conventional dynamic power is shown in the figure. The operation of the comparator has reset phase and comparison phase. In the reset phase the reset transistors (*M*7–*M*8) pulls the output nodes Out*n* and Out*p* to *V*DD when CLK = 0 and *M*tail is off. This defines the initial condition.

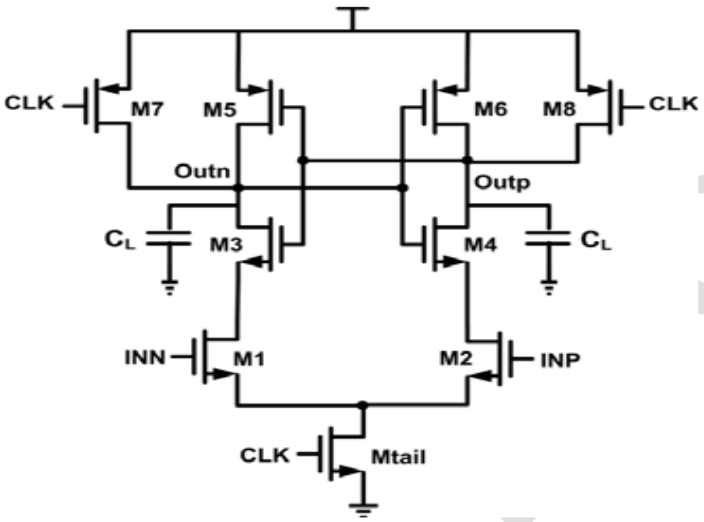

Fig. 1: Schematic diagram of the conventional dynamic comparator (CDC).

The reset phase stabilizes a valid logical level through the reset transistors. During comparison phase, when CLK = *V*DD, *M*tail is on and transistors *M*7 and *M*8 are off. Based on the input values (INN/INP) the precharged output voltages (Out*p*, Out*n)*, start to discharge with different discharging rates. When *V*INP > *V*INN, Out*p* discharges faster than Out*n*, and If *V*INP < *V*INN, the circuits works vice versa. The circuit suffers from parasitic capacitances of input transistors which can be eliminated by designing large transistors for the input stage. The other tradeoff is the need of high supply voltage due to several stacked transistors. The circuit also suffers from only one current path.

Double Tail Dynamic Comparator (DTDC)

The draw back of the conventional comparator is rectified by the double tail comparator shown in figure 2. The double-tail dynamic comparator topology reduces the transistor stacking and operates at lower supply voltages compared to the conventional dynamic comparator shown in figure 1.

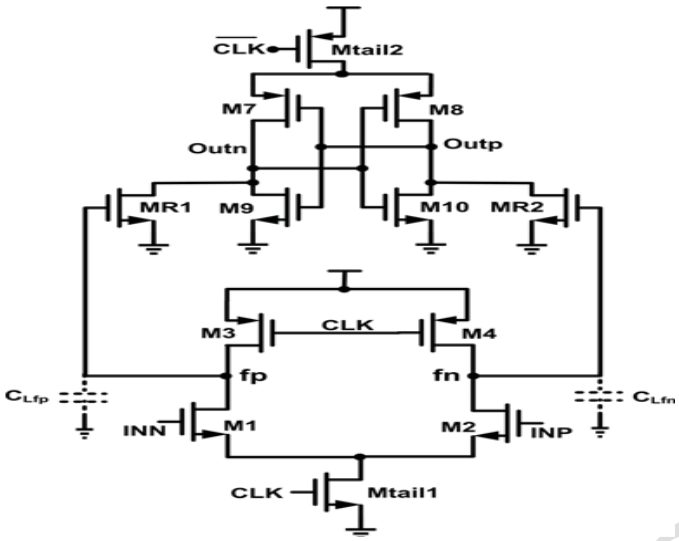

Fig. 2: Schematic diagram of the conventional double-tail dynamic comparator(DTDC).

The double tail enables both a large current in the latching stage and wider *M*tail2, for fast latching independent of the input common-mode voltage (*V*cm), and a small current in the input stage (small *M*tail1), for low offset. The operation of this comparator in figure 2 is as follows. During reset phase (CLK = 0, *M*tail1, and *M*tail2 are off), transistors *M*3-*M*4 pre-charge fn and fp nodes to *V*DD, which in turn causes transistors *M*R1 and *M*R2 to discharge the output nodes to ground. During decision-making phase (CLK = *V*DD, *M*tail1 and *M*tail2 turn on), *M*3-*M*4 turn off and voltages at nodes fn and fp start to drop with the rate defined by *I*Mtail1/*C*fn(p) and on top of this, an input-dependent differential voltage $\Delta V_{fn(p)}$ will build up. The intermediate stage formed by *M*R1 and *M*R2 passes $\Delta V_{fn(p)}$ to the crosscoupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise. The circuit suffers from few disadvantages they are delay issues and power consumption. Sufficient output voltages at stage one is required to reduce the delay and power consumption. To eliminate this draw back two control transistors (*M*c1 and *M*c2) have been added to the first stage in parallel to *M*3/*M*4 transistors but in a cross-coupled manner. This configuration increases the $\Delta V_{fn/fp}$ by which the latch regeneration speed increases as shown in figure 3. This is the modified dynamic comparator structure whose performance is better when compared to the conventional Double tail Comparator.

High Speed Low Power Dynamic Comparator (HSLP)

The circuits given in figure 1,2 and 3 provide high input impedence , rail to rail output swing and less stacking but the speed of operation is limited. A high speed low power dynamic comparator is illustrated in Fig.4. The inverter input structure boosts the input common mode voltage. The input referred noise is reduced by keeping the transistors M3 and M4 in saturation state through clk2 which is the delayed version of clk1. (clk1=1 and clk2=0). Transistors M7 and M8 accelerate the latch.

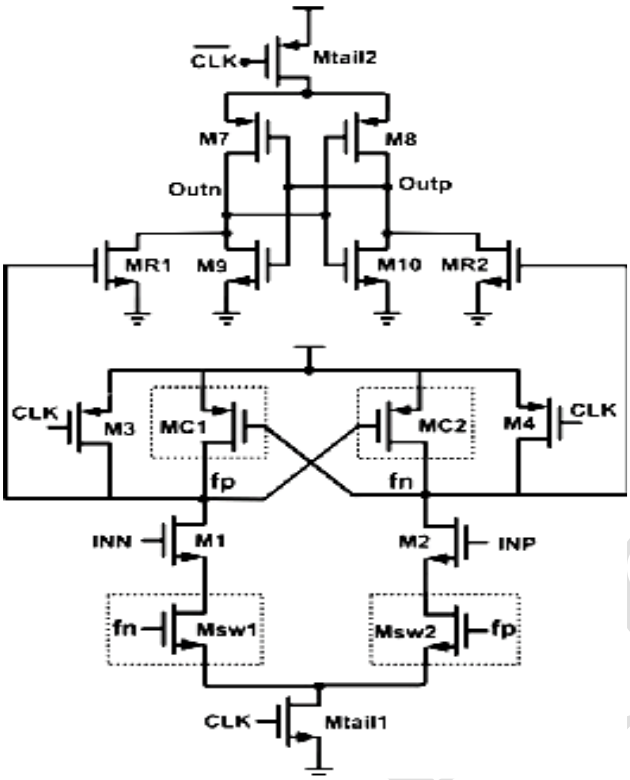

Fig. 3: Schematic diagram of the Modified dynamic comparator structure (MDCS).

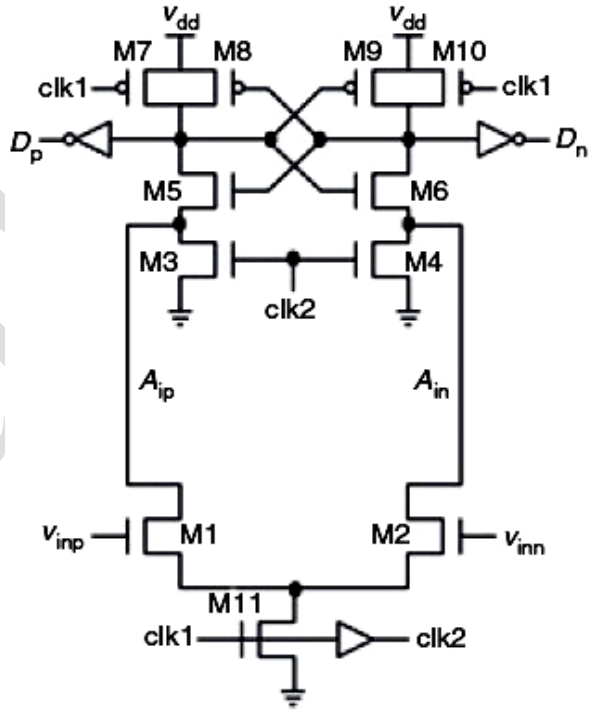

Fig. 4: High-speed low-power dynamic comparator (HSLP).

Materials and Methods

The proposed High speed switched dynamic comparator (HSDC) with constant I_d/g_m biasing is shown in figure 5. The double tail structure reduces the number of stacked transistors. For the analysis considering from left end in figure 5 consisting of the constant I_d/g_m biasing connected to the tail transistor M and M. This circuit reduces the enviroinmental drift. The constant I_d/g_m biasing circuit can drive other circuits in the ADC. For the purpose a differential unity gain buffer is included in the circuit which maintains the voltage level. The switched dynamic comparator is designed to drive two latches L1 and L2. The digital switching operation is carried out using NAND gate. The first stage is shared between the driving circuit which reduces the input capacitance. The input capacitance lowering reduces the power consumption. Three clock signals are used to operate the SDC.The dynamic amplifier block operates with full rate through CLK0. The latches L1 and L2 are controlled by CLK1 and CLK2. The offset calibration is taken care by the two capacitance C_{1L} and C_{1R}.

During reset phase LAT1 is rest by making Vck0 = 0, Vck1 = V_{DD}, the source nodes Vsp and Vsn are charged to V_{DD} while the nodes at Gate terminal V1p and V1n are discharged to ground, causing the outputs Vop1 and Von1 to be charged to V_{DD}. During sampling phase, Vck0= V_{DD} causing Vsp and Vsn to change its state depending on the inputs V1p and V1n. A differential signal ΔVspn=Vsn-Vsp is applied between Vsp and Vsn. Now LAT1 regenerates the final output when Vck1 = V_{DD} at which point Vsp and Vsn is in discharge state to pass the differential signal ΔVspn=Vsn-Vsp to LAT1. This is achieved by adding a delay t_{dl} to the Vck1 such that $t_{dl} > t_s+t$, where t_s and t_1 are charging and discharging of source and node 1 to V_{DD} and ground respectively. Worst case approximation is made so that the clocks Vck1 and Vck2 toggle only after the delay when Vsp and Vsn reach ground potential and V1p and V1n reach V_{DD}. This will eliminate the jitter and skew spurs in the system. In regenerative phase Vck1=0 and V1p=V_{DD} and V1n=V_{DD}, signal regeneration happens in the cross coupled inverters. The outputs of the latches are given to a second stage where the transistors M_{13} and M_{16} accelerate the values.

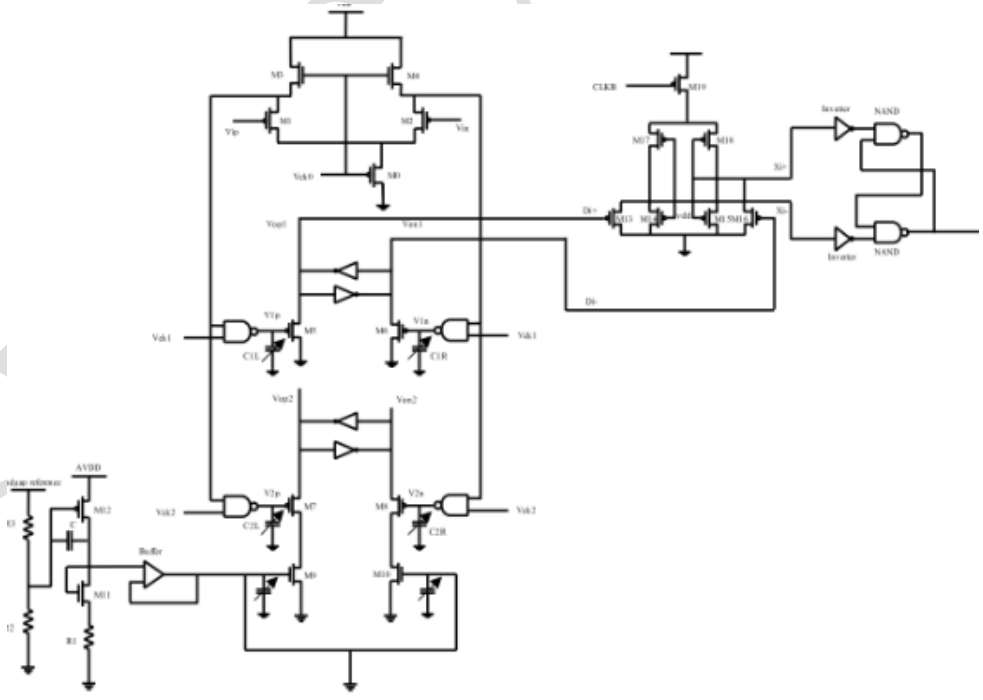

Fig. 5: Proposed high-speed low-power Switched dynamic comparator (HSDC).

The M_{19} transistor provides fast latching independent of the output voltage from latches LAT1 and LAT2. The transistors M_{13} and M_{16} passes $\Delta Vop2$ to cross coupled inverters formed by transistors M_{14}, M_{15}, M_{17} and M_{18} and provides the shielding between the latches and next stage.

Results and Discussion

A CMOS based comparators in figure 1-5 are implemented using predictive technology model for 45nm and 65nm. Table 1 provides the power analysis on average and peak power observed during the comparator operation. The clock frequency kept is 3GHz and the supply voltage is 1V. For the average power the proposed HSDC consumes lesser power when compared to other circuits. It saves power of about 28% compared to DTDC and 55% when compared to HSLP comparator. Eventhough CDC consumes less power but its slower in operation and have less noise immunity.

Table 1: Power analysis of different Dynamic comparators.

METHOD /PARAMETER	CDC	DTDC	MDCS	HSLP	HSDC
AVERAGE POWER (μW)	29.26	909	869	1450	650
PEAK POWER (μW)	191.82	181	1942	3105	2748

Table 2: Output voltage for different inputs.

Inputs		CDC		DTDC		MDCS		HSLP	
Input 1(V)	Input 2 (V)	OUT+(V)	OUT-(V)	OUT+(V)	OUT-(V)	OUT+(V)	OUT-(V)	OUT+(V)	OUT-(V)
0	0	0.044	0.044	0.050	0.050	0.050	0.050	0.051	0.050
1	1	0.490	0.490	0.999	0.999	1.000	0.997	0.998	0.996
0.5	0	1.000	0.055	1.000	0.034	0.999	0.043	0.998	0.042
0.25	0	0.812	0.036	0.817	0.050	0.878	0.050	0.877	0.050
0.26	0	0.917	0.032	0.960	0.050	0.963	0.050	0.967	0.050

The obtained output voltage is shown in table 2. The output voltage swing is about 97% of V_{DD} which is a 6% improvement in voltage swing when compared to the conventional method. The implemented circuit is shown in figure 6. Additional transistors are consumed for the I_d/g_m biasing block and latching stages but provides better noise immunity and driving cabability. Table 3 shows the performance comparison of the proposed circuit in 45nm and 65nm. Here the inputs are varied for different voltage combination. The inputs are varied from 0 to 1V since the V_{DD} is 1V. For the comparison purpose for both 45nm and 65nm the V_{DD} is chosen as 1V. The power consumed in 65nm for the proposed method is 7.8% more when compared with 45nm. The average current is nearly twice that of 45nm.

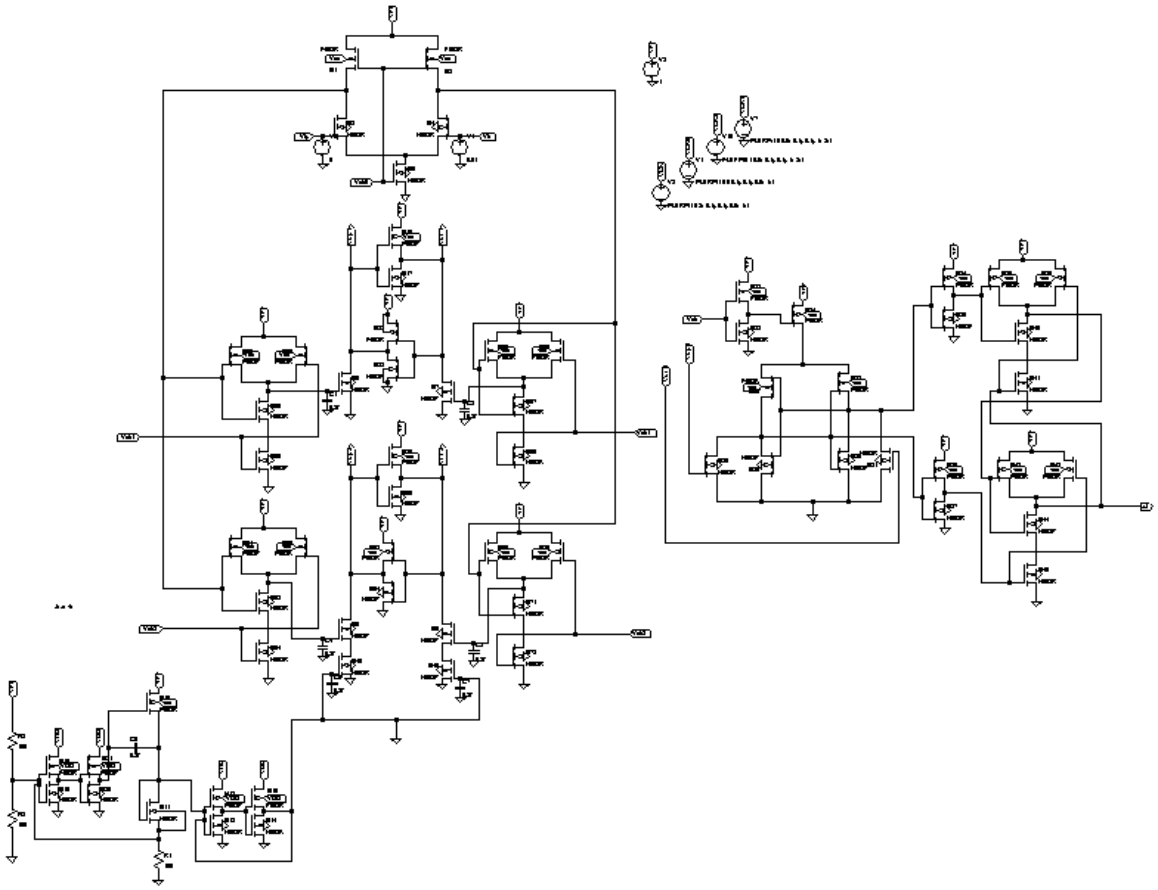

Fig. 6: Implementation of Proposed high-speed dynamic comparator(HSDC).

Table 3: Performance of the proposed high-speed low-power dynamic comparator for clock =1 GHz.

N(V)	P(V)	Average power(mW)		Average current(mA)		Peak power(mW)		Peakcurrent(mA)	
		45	65	45	65	45	65	45	65
0	0	0.006881	0.007129	0.006884	0.00679	0.19788	0.34788	9.1217	11.289
0	0.24	0.006881	0.007129	0.006884	0.00679	0.19788	0.34788	9.1217	11.289
0.24	0	0.006881	0.007129	0.006884	0.00679	0.19788	0.34788	9.1217	11.289
0	0.25	0.006899	0.007128	0.006654	0.006765	0.8667	0.38853	8.3733	10.478
0.25	0	0.006899	0.007128	0.006899	0.006765	0.8667	0.38853	8.3733	10.478
0	0.5	0.006881	0.007129	0.006884	0.00679	0.19788	0.34788	9.1217	11.289
0.5	0	0.006881	0.007129	0.006884	0.00679	0.19788	0.34788	9.1217	11.289
1	1	0.006881	0.007129	0.006884	0.00679	0.19788	0.34788	9.1217	11.289

Table 4: Performance of the proposed high-speed low-power dynamic comparator for clock =2 GHz.

N(V)	P(V)	Average power(mW)		Average current(mA)		Peak power(mW)		Peakcurrent(mA)	
		45	65	45	65	45	65	45	65
0	0	0.00691	0.00715	0.00714	0.00729	0.04941	0.01078	8.75160	11.08100
0	0.24	0.00695	0.00712	0.00710	0.00741	0.23036	0.01399	8.43610	10.96400
0.24	0	0.00695	0.00713	0.00709	0.00738	0.20927	0.01312	8.44380	10.96400
0	0.25	0.00695	0.00713	0.00713	0.00735	0.23866	0.01301	8.44830	10.95500
0.25	0	0.00695	0.00713	0.00713	0.00738	0.21139	0.01311	8.46410	10.96300
0	0.5	0.00698	0.00712	0.00699	0.00741	0.30565	0.01157	8.49510	10.93600

0.5	0	0.00698	0.00712	0.00686	0.00760	0.27624	0.01107	8.42130	10.95900
1	1	0.00683	0.00708	0.00741	0.00713	0.01860	0.01093	8.96270	10.78400

Conclusion

The paper presents the design of Low noise, high speed, capacitance Switched Dynamic Comparator (SDC) for high speed application in 45nm and 65nm. The dynamic comparator proposed in this project not only eliminates the offset voltage but reduces the area occupied and is suitable for flash ADC applications like Biomedical systems, communication etc. The proposed methodology eliminates the staking issues and provides a improved maximum output voltage swing of 96%. When compared with the conventional method the proposed method saves power by 25% when compared to the existing double tail comparator. The delay issues are rectified by the regenerative feedback and the sharing of first stage minimizes the input capacitance. The simulation results in a 45nm and 65nm CMOS technology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and output swing are significantly improved. The maximum clock frequency of the proposed comparator is increased to 3.5GHz at supply voltage of 1V. The circuits in 45nm and 65nm are tested with various supply voltage ranging from 0.6V to 1V and frequency of operation from 1GHz to 4GHz. The simulation is carried out using predictive technology model for 45nm and 65nm in HSPICE.

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