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A Symmetric Solar Photovoltaic Inverter to Improve Power Quality Using Digital Pulsewidth Modulation Approach

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Abstract
A symmetric multilevel inverter is designed and developed by implementing the modulation techniques for generating the higher output voltage amplitude with fifteen level output. Among these modulation techniques, the proposed SFI (Solar Fed Inverter) controlled with Sinusoidal-Pulse width modulation in experimental result and simulation of Digital-PWM results is verified under the lowest THD level. There are three intelligent techniques proposed in SFI, among these intelligent controllers the MPP (Maximum Power Point) based controller gives better results. An open loop, close loop control system is implemented for the different operating load conditions (R and RL load). In the proposed system the Solar-PV array using SPR305W is maintained constant power by implementing an MPP approach to the (DC–DC) Double-lift Converter. The DC–DC converters are fed with SFI inverter circuit. The proposed structure for analysis and implementation for simulated with MATLAB/Simulink (R2020a) software. Experimental setup is carried out with Field Programmable Gate Array based processor to generate the switching sequences based on the proposed methodologies. The performance of the SFI operating with load connected system is analysis with output voltage/current, reactive power, and minimized harmonics level.

Keywords Solar Fed Inverter · Sinusoidal-PWM · Digital-PWM · Double-lift Converter · Maximum Power Point

1 Introduction

The MLI or electrical DC voltage source inverters leads in two cases: (i). Symmetrical, and (ii) Asymmetric model [1, 2]. The asymmetric model of the inverter has been designed a high number of voltage level achieved with more number of bulky switches, and driver circuits for generating various levels. Here, the symmetrical model inverter minimum number of voltage levels is to achieve the maximum number of output. At present a symmetrical MLI topologies, DC powers are contained an equivalent output voltage which guarantees

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equal magnitude and it is the same magnitude of voltage that is forwarded into a series-connected inverter circuit [3]. The multilevel power converter has been introduced as high power to medium power applications. Even though the conventional and modular multilevel PWM inverters are widely used in industrial applications. NPC fifteen level power circuit topology was developed by Nabae, Akagi, and Takahashi in 1981 is utilized bulky of a series capacitor to split the DC bus voltage as shown in Fig. 1a [4]. A diode transfers a limited amount of voltage, thus reducing the stress on other electrical devices. The NPC inverter is also referred to as a diode clamped inverter, which is the first time used in a three-level inverter. The mid voltage in the multilevel inverter is defined as a neutral point. The switching devices are connected in series to enhance the desired voltage and power output levels. The switching devices (N-level) are required blocking voltage level denoted by V_{DC}/(N-1). The inner voltage points are clamped by two extra diodes, clamping

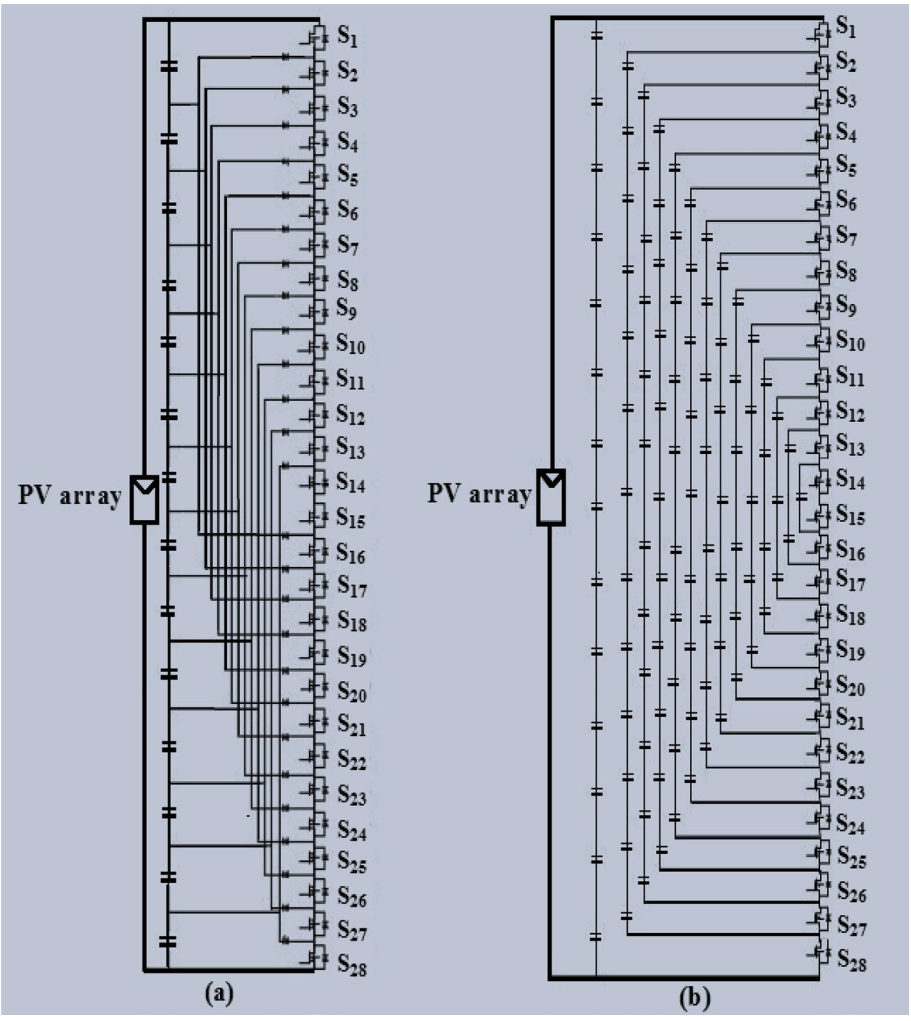


Fig. 1 **a** Fifteen level neutral point clamped power circuit and **b** fifteen level flying capacitor power circuit [4, 5, 7, 9]

diodes, or one high-frequency capacitor, it needs to different voltage ratings for different inner voltage levels.

In fifteen level power circuits, DC voltage or PV input splits into seven series-connected bulk capacitors. The diode clamp switch voltage is half the level of the DC bus voltage. The disadvantages of NPC are: (1) the converter requires a higher number of diodes and the device is inefficient, (2) the reverse blocking voltage in NPC cannot be maintained as per the selected switching pattern and it needs of separate voltage rating, (3) due to capacitor unbalance issues, it's difficult to control the active power switch of each converter stage, due to overcoming the process to minimize the frequency of the switching, (4) an additional neutral point voltage balancing control circuit is required for converters of more than three levels, and (5) one particular drawback is the high number of power semiconductor switches are required. Even though low rated voltage inverter switches are connected in the gate drive and buffer circuit. That's the way to complicate the overall NPC inverter system for more overpriced.

The clamping diodes are replaced by FC called as capacitor clamped or ladder structure of DC side capacitors. The voltage of the capacitors floats concerning earth potential. Where the voltage on each capacitor differs from that of the next level of the capacitor voltage. The number of levels depends on the number of required switches in each limb. The reactive and real power flow can be controlled by the constant capacitor voltage with the selection of an accurate switching combination. The increment of the capacitor voltage between the two adjacent capacitor legs is provided the size of the voltage steps waveform in multilevel output. The phase redundancy is available for balancing the voltage levels of the capacitors.

The FC multilevel inverter power circuit is illustrated in Fig. 1b [5, 7, 9], it shows an output of fifteen level voltages. The disadvantages of FC-MLI are: (1) the switching combination and output efficiency are poor for real power transmission, due to high frequency switching needed compare to fundamental level, (2) inverter control circuit is required to maintain the voltage balance of the capacitor and rating of the capacitor is difficult to design, (3) it can control both the active and the reactive power flow. However, due to high-frequency switching, switching losses occurs, and large size of the DC bus voltage, (4) a large number of capacitors are bulky and more expensive than the clamping diodes used in the multilevel inverter.

The concept of CH-B multilevel inverter topology was introduced with three-level converters patented by Banister and Baker in the year of 1975 [6]. The CH-B inverter uses different DC sources or capacitors. It consists of switches and capacitors pair combination in series connection of power conversion cell. The output voltage is added by the sum of all voltages generated by each H Bridge cell. One particular drawback is found out from CHB inverter, a large number of power semiconductor switches, and each switch is connected into a gate driver circuit that adds more complexity of the circuit as shown in Fig. 2, which makes the overall system is going to be more expensive [9].

Among the various multilevel inverter topologies, an investigated cascade inverter that are ideal for connecting non-conventional sources with the N-LL, because of the need for separate DC sources. A single-phase CH-B converter for a PV grid-connected module. This consists of several series-connected H-bridge cells in each bridge connected to a PV module string, and each DC connection voltage is allowed to be regulated independently. These CHB converters are controlled by adding maximum power point algorithms with a configuration consisting of two cells and two PV panels. It has been shown that the converter can function properly even under conditions with different string radiation and generates a sinusoidal output waveform.

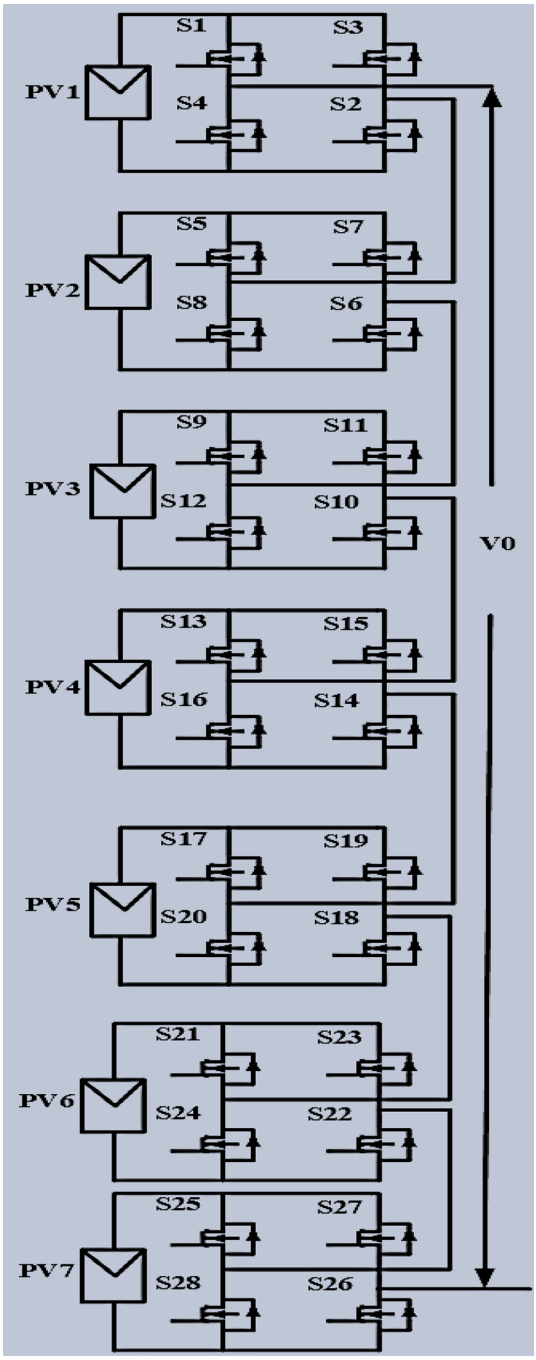


Fig. 2 Fifteen level cascade H-bridge power circuit [9]

Table 1 Compare and implementation requirements in Traditional MLI

S. no.	Implementation and specific requirements	NPC [7]	FC [8]	CH-B [9]	MMC [10]
1	Design and complexity	Low	Medium (capacitors)	High	Low
2	Modularity	Low	High	High	Medium
3	Control scheme	Voltage balance	Voltage setup	Power share	Voltage share
4	Fault tolerance	Difficult	Easy	Easy	Easy

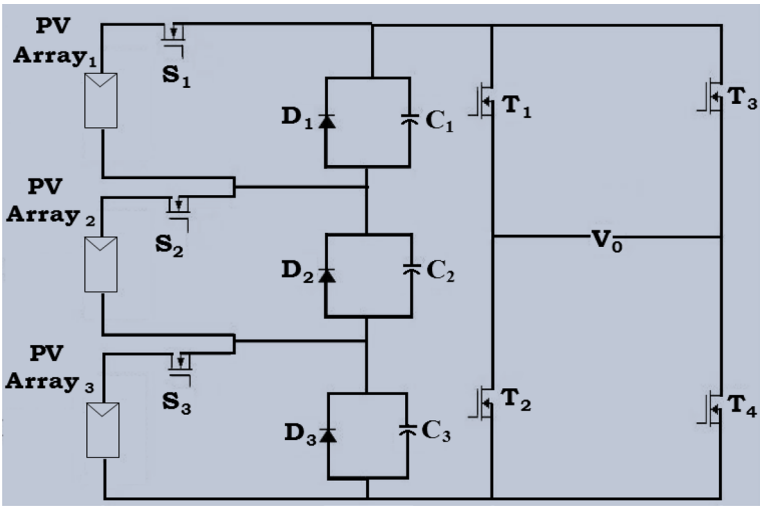


Fig. 3 Fifteen level modular multilevel converter [10]

CH-B inverter is an extra advantage of fewer components to achieve the same number of output voltage rates across the traditional multilevel inverters. One of the drawbacks of CH-B multilevel inverters is the increased number of power semiconductor switches required, which increases the voltage drop across the switch and EMI problem. The most common multilevel converters are NPC, FC, and CH-B MLI are used high-medium and low voltage multilevel level inverters. A CH-B inverter is used for high power output with an easy way to fault tolerance power sharing control scheme, and it depends on the modulation scheme of the inverter unit. The comparison of implementation and specific requirement factors as shown in Table 1.

The conventional MLI topology integrates multiple levels using for several semiconductor equipment's. It may establishment zone because of increases cost of the converter, and poor control complexity circuits. The conventional solar fed fifteen level multilevel inverter requires 28 switches, the advantage of this converter is in the reduction of THD by increasing level. But the Multilevel Modular Converter (MMC) methods only 7 switches are employed to achieve 15 level output as shown in Fig. 3 [10]. In general, this type of

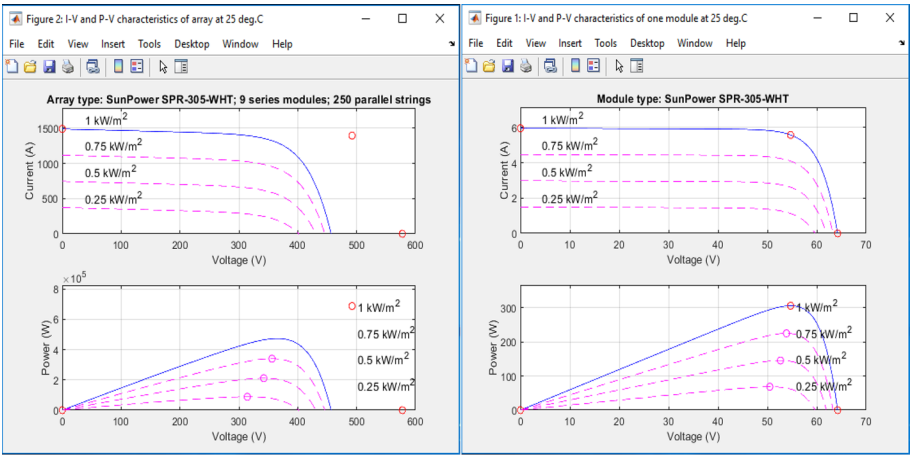


Fig. 4 Solar array output characteristics **a** volts verses current **b** volts verses power

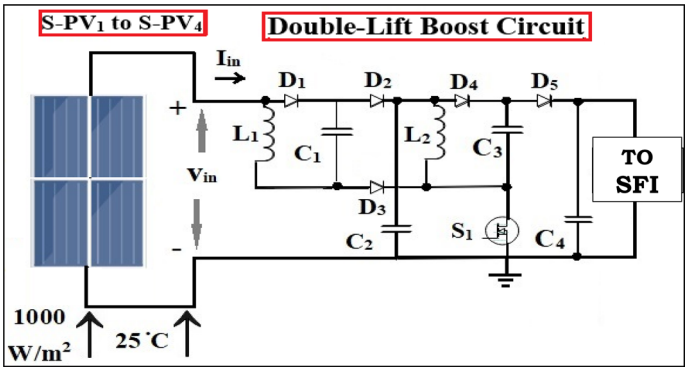


Fig. 5 Proposed circuit module

BSE is used to the off-grid mode of operation like rooftop mounting, R, RL, and motor load connected system. The BSE encompasses all equipment of a PV system, and it is connected in a series of converter power circuits, load etc.

The BSE consists of wires, switches, capacitor battery bank, a battery charge regulator, and one or many solar multilevel inverters, etc. This type of installation frameworks is incorporate in MLI attachments on both AC and DC links. The over current protection devices, intersecting boxes, and potentially circuit-combiner boxes are combined in system equipment. The BSE refers the minimum equipment combination system, which is used to moves the DC energy produced by S-PV panel, which will be wired in series through power conversion turn into an AC electricity with the help of MLI. The

proposed solar multilevel inverters have special functions for adapted, which is used to PV array with includes in an MPP tracking output as shown in Fig. 4.

The DLC is modified from a step-up boost converter. A modified the DC–DC boost circuit, it consists of a coupled inductor, filters, charge pump capacitor, and active clamper circuit. These all components are more complexity of the control and complicated in the power circuit. Here, the (DC–DC) same method is revised so far, show that the output voltage is two times higher than the input voltage source V_1, but the requirement is much needed to reduce in module structure. Therefore, the proposed DLC is presented with the minimum number of devices shown in Fig. 5. The input voltage source (V_{in}) for the converter is roughly around 64.2 V, 5.96A. The performance of DLC yields the output voltage is roughly around (V_{out}) 128-130V_{dc} calculated for both theoretically and practically in Eq. (1). This was improved by two significant parameters as namely inductors (L1, L2) and capacitors (C1, C2 and C3).

The Solar input sources are wired in series through a DLC, which operates and raises voltages are generated to Symmetric SFI. Solar panels are versatile energy technologies that can help electrical customers of all kinds of their electricity needs. Renewable energy systems like PV are undergoing major technological developments, and large scale deployment in the integration of linear, non-linear load connected systems [11]. The proposed MLI technology is attractive for PV applications since the several sources on the DC side of the converters are to make difficulty of the power circuit. In this regard, a low voltage commercial inverter, it can offer the solar fed standalone (off-grid) Balanced System Equipment's (BSE) to minimize cost, reduce the common-mode voltage, and EMI problems.

$$V_1 = \frac{2-K}{1-K} V_{in} \tag{1}$$

Here, $K = 0.5$,

$$V_1 = \frac{2-0.5}{1-0.5} \times 22.1 = 66.3\text{V}$$

2 Literature Study

In this literature survey generally focused and its attention towards under the area of a multilevel inverter with the various control topologies are included. (1) solar-PV installation, (2) reduced semiconductor devices, (3) capacitor voltage balancing and RPC, (4) modulation strategies, and (5) modified classical-MLI with different R load and L load. These works are reported medium power circuits with reduced switches levels. The FPGA experimental validation is also limited to medium or low voltage levels. The integration of MLI for renewable energy sources is also considered, but the implementation is carried out with low and medium power PV application.

In this literature survey related to Solar-PV installation. It has been focused on the solar-PV array modules installation, BSE equipment, and MPP system. In the demand for solar energy total power produced recommend in India. Due to the rapid reduction of fossil

fuel minimization to improve the performance of PV panels examine in different types of faults are discussed; (1) bypass module (2) blocking diodes under partially shaded condition (3) unified modules. The conventional techniques such as Perturb & Observe (P&O), incremental conductance, and Partial Swarm Optimization (PSO) algorithms are comparatively studied. A high-quality Silicon Dioxide (SiO_2) films with excellent surface passivation capabilities produced by thermal oxidation and plasma-enhanced chemical vapor deposition. In recent, the solar cells such as Czochralski Silicon (CZ-Si), and Aluminum-Passivized Emitter Rear cells Al-PERC) are more attentive in the worldwide market. The Industrial silicon di-oxide (Si–O_2), *p*-type CZ-Si- PERC's have an excellent output with an average of 21.9%, and the absolute improvement of 1.3% is compared to traditional (Al-BSF) solar cells [11, 12].

An investigated different environmental factor of partial shading conditions in the solar-PV module. In addition to the efficiency of parameters are tracking by the P&O-MPP, and PSO-MPP techniques. The MLI is chosen from a traditional type of inverters due to many advantages such as (1) improvement of P-Q in PV generation, (2) reduction of filter-size requirements, and (3) the increase in many voltage levels etc. [13]. An established in solar–wind based hybrid system using a power management strategy. This kind of energy system can be operated only ON/OFF the grid. The power management unit is performing either grid-connected or autonomous measurement from various point and it provides an effective energy transfer from battery equipment to various load or grid. A recommended a novel asymmetric CH-B inverter introduced voltage ratio 14:7:2:1. The electricity is fed into the utility at varied solar-irradiance conditions, one main source can be provided by a PV array conditions and the other 3-sources can be supplied by separate converter sources [14].

In this literature, surveys are related to reducing semiconductor devices such as (1) number of switches (2) number of main diodes (3) number of clamping diodes (4) number of DC bus capacitor (5) number of balancing capacitors. The chapter deals with examining the reduction of semiconductor devices in multilevel inverters such as Switched-Capacitor (S-C), Ladder and Traditional inverters [15]. The literature review of multilevel inverter topologies is briefly described of reduces components such as a capacitor, power switch, diode, and DC source, etc. The sustainable energy technologies such as Solar-Photovoltaics (S-PV) and wind power have a key role to play for electricity generation. To minimize the pollution with low-cost interface multilevel inverters are increased to continuous power development. As one of the most critical problems is the electric input stage into a consumer stage, the consistency of the voltage should be taken as a good quality output level. As a result, a lot of investigation based on their attention to MLI, and it has been increased the electrical power efficiency by the way to reduce the harmonics level [16].

A study of Diode-Clamped (D-C) MLI topology with a voltage resistance problem of power element in the high and medium power situation. It consists of a maximum 8-power switch, 14-diode, 4-capacitor, and one DC voltage source to generate five level multilevel output voltage, the implementation of the D-C topology has been accompanied by the development of modulation scheme. At the same time, the 3rd harmonic injection method is implemented to reduce the harmonics level in the multilevel output waveform [17]. A single-phase Switched Capacitor (S-C) units. It will increase the DC power voltage at

the input without using the transformer by parallel and serial operation of the capacitor. Therefore, 17 levels S-C unit is developed by two isolated DC-source, ten semiconductor switches, two power-diode, and two capacitors, and 49 levels S-C unit is developed by three isolated DC-source, fourteen semiconductor switches, three power diode, and three capacitors. The proposed topology is compared with conventional architectures in terms of the maximum number of switches, diodes, and DC supply needed.

Two-leg ladder topology of MLI. The Ladder topology is required 14 -IGBT switches, 10-Driver circuits, 4-DC source, which can produce a large number of levels with a minimized number of electronics components compared to the other classical converters [18]. The magnitude of the voltage stress is blocked with reduces number of switches. The two methods are presented in 25 level and 9 levels output multilevel waveform investigated for selecting the DC voltage sources. Two PWM control strategies of FC using single-phase MLI. It consists of 15 level and 33 level inverter control with sinusoidal multi carrier PWM and triangular multicarrier PWM. The fifteen level FC inverter is consisting of 28-bulky switch, 13-clamping capacitor, 2-balancing capacitor, and single DC voltage source. It will be produced an output voltage of 200 V and less THD level 4.06% in Sinusoidal PWM. A proposed emerging fifteen level MLI topology required eight switches for generating output waveform. The new modified inverter topology that can synthesize with a reduced number of switch count, driver circuits with all possible addition and subtractive combinations of both source and load. The simulation result is presented THD 4.5%, and prototype model load voltage/current THD are 5.4% and 2.0% [19].

The RPC with the help of Capacitor Voltage Balanced (CVB) technique was implemented in 4-level inverter. The single-phase load in transient and steady-state conditions are evaluated by balancing FC voltage. The proposed T-type, NPC inverter is compared with classical and modified NPC [20]. Proposed MMC is made by three high-frequency isolation-transformer. In this topology consist of inter-arm CVB strategy, in each arm are comprised of multiple half sub-bridge modules and added some clamping diodes. Which is controlled by the two arms in one phase CVB of power transmission and the direction in between two modified sub-bridge modules. The drawback of MMC, two voltage sensors in each arm are required for the proposed CVB technique, and it takes very little time for the control and monitoring system [21].

FC clamped inverter circuit is controlled by a multicarrier PWM method [22]. The self-CVB results are obtained from FC clamped circuit, which is generated quality output voltage waveform enhanced without any auxiliary circuits. A MLI fed with the Solar-PV system. The structure should be attractive for high power solar CH-B multilevel converter and the RPC is applied in a grid-tie integrated PV system. The 5 KW Solar-PV converter module with an MPP control algorithm has been developed to minimize the DC-link capacitance and eliminate over modulation by an unsymmetrical power circuit. Clamped inverter circuit, which is an increased voltage level with CVB in a parallel switching circuit. Based on the MLI topology, there are several DC links in parallel chopper circuit, and it consists of more number of storage capacitor with a single switch operation in each interval time. The capacitor charging process is directly charged up by using DC source. Therefore, the lack of charging and extra charging time is avoided. A chopper based FC employed with capacitor voltage equalization by using NPC converter [23]. The CVB methods are

propounded with three and four-level chopper topology. It's required more multiple capacitors and power semiconductor devices but reduces in voltage rating compared with a conventional chopper. There are two possible solutions to the voltage imbalance problems:

(1) Install CVB circuit in DC side of the MLI.
(2) Modify the inverter switching pattern with a respective control strategy.

The hardware and simulation circuits have been verified in CVB condition, and results are obtained in transient state conditions. The review of the modulation strategy has been analyzed based on the input and output load conditions. These are all modulation methods are applied in converter or inverter switches, it can be controlled by two strategies [24, 25] (1) SPWM, (2) DPWM. The proposed modulation scheme is intended to describe carrier, reference, and digital signals. It will apply towards the symmetric converter switches to minimize the THD level across the load. An emphasized half and full-bridge inverter with the SPWM strategy. Which can more complicate to adopt with unipolar and bipolar semiconductor devices, but it is helpful to reduce the harmonics level and maximize the output with varied frequency lower level up to higher-level range. In this recent decades a DPWM for different switching patterns using for a single counter-based PV inverter. These can implement with 3 AN-Spartan hardware kits through Xilinx software. The digital sinusoidal pulses were generated by the FPGA prototype, and it has been able to control reactive and active power control with least the number of computational resources.

The NPC three-level SPWM inverter, it is compared with Space Vector Modulation (SVM) scheme [26]. The proposed SPWM scheme is achieved high output voltage instead of SVM, and it can be accomplished by low Modulation Index (MI) in a different open switch fault. A renewable source MLI with various modulation strategies using R, R-L, and motor load applications. It has been discussed with various control and MI. These strategies are focused on P-Q development in different load and THD value measurement. Reviewed on PWM scheme for voltage harmonic reductions in a three phase two-level inverter. The common mode PWM strategies have been classified and comparison with the conventional PWM method such as phase shift PWM, SPWM, SVM, and DPWM. Based on the common voltage reduction study, both software and hardware model is suggested to reduce the cost and control in converter circuits [27].

FPGA based SPWM controller for CH-B single phase inverter, which is fed with adjustable AC motor drive. The proposed control circuit is adopted by using the FPGA trainer kit to generate gate pulses to the inverter circuit. Which has pointed out the SPWM using to control the cascade inverter with a balanced voltage source, and it can furthermore voltage range progress with 5, 9, and 17 levels. The output voltage of the minimum THD level has been presented at both nine and seventy levels respectively 9.2% and 22.75% [28]. The FPGA controller is adopted for generating pulses with a gate driver circuit, the pulses are multi-carrier SPWM [29]. It can control and access the permanent magnet generator. The 3-level NPC back to back converter circuit is proposed with low computational requirement both simulation and experimental study. A unipolar SPWM with a minimum number of CH-B switches. The 5-level inverter, which is generated less THD value 37% and 38% under the 2 modulation scheme such as unipolar SPWM, and improved SPWM. The experimental results are under R-L load condition with a variable frequency of 3 kHz in a DSP platform.

A CH-B with 7 and 11-level switched capacitor, the modulation scheme is implemented in H-Bridge [30], where the modulation frequency is significantly less than the carrier

frequency. It has been implemented phase shift SPWM modulation to minimize THD level 24% in seven-level inverter, and 14% is eleven level inverter respectively. A single carried SPWM method, it has been developed in a Fourier integral applied in an MLI, and it operates under R-L load conditions with minimum harmonics in a motor or grid application. In the literature survey related to the DC/DC converter, it has been mainly focused on constant voltage get from an input source (PV). It is regulated fed into the next stage of the series DC/DC converter. These converters aim to boost up the voltage, and it is passing through the next level of MLI. A single end inductor based DC–DC converter applicable for the S-PV system [31]. The merits of the proposed model minimize voltage ripple across the solar panels. The steady-state analysis is validated both continuous and discontinuous approach provided the output with the help of the duty cycle incremental, and it can minimize the conduction losses, switching stress of the devices. A preferred PV energy applied medium power push–pull (DC/DC) converter, it has been controlled by FL-PI tuned controller to generate the pulses into DC motor. The settling time and efficiency of the model have been compared with classical PI and fuzzy controller.

Solar technology is a system of DC–DC converters for efficient conversion and control of electricity with various modulation arrangements [32]. The rapid growth of solar-PV installations worldwide has been motivated by a variety of environmental factors such as, including renewable portfolio requirements, lower deployment charges, and net metering required by governments or feed tariffs. A single switch DC–DC voltage lift converter for solar-PV application. It is proposed reduced voltage stress and provides better utilization factor compared to other renewable solar converters. The lifting converter is comprised of switched inductor and capacitor structure, additionally integrated with boost capacitors using for improved voltage gain process.

The prescribed tracking the current or voltage by using various MPP algorithms that are carried out for DC/DC-based converter. The overall system performance is made by a non-isolated converter, which is used for MPP of the solar-PV system. The FPGA controlled solar-based two stage converter using for S-PV application [33]. A DC–DC converter is provided the isolation in between the (PV) source and load. A Quasi Z-source modified cascade converter that is comprised of high DC power interaction of the solar system. It's included the model of series isolated bridge converter, and the post-stage of H-bridge connect in series with DC/DC converters are fed into electrical utility load. Fuzzy controller based MPP algorithm using boost converter for applying in PV application. The PV simulator (Terra-SAS/DCS80-15) is produced maximum power with the help of MPP (P&O) method, and the MPP based fuzzy controller generates the gate pulse to converter switch (both symmetric and Asymmetric method), and the low-cost experimental and simulation model has generated the output power with the different irradiation level.

Recently, enormous publications are discussed MLI technology [34], and it can increase the importance of MLI using for medium and high power applications. To better realization and the analysis of the multilevel technology, it's should be reviewed and studied in a classic multilevel converter. These works are survived the literature study in depth of traditional multilevel topologies, such as the CH-B, NPC, and FC. The prescribed a summary of MLI circuit technology developed in the area of medium and high power control. The fundamental principle of different MLI like as D-C inverter or (NPC), Capacitor Clamped or (FC), and CH-B with separate DC sources are introduced systematically [35]. A reviewed the different emerging topologies like symmetric/asymmetric topology, hybrid clamped topology, Z-source multilevel, mixed multilevel, and reduced MLI parts are discussed. The major drawback of MLI topology, the inverter circuit more complex,

and several components are used. In recently, MLI's are evolved as a major role played power industry in an N-LL, and it's have been established by work utilization a small number of components with RE growth in power electronics technologies.

An expanded the CH-B converter based on the series connection of multiple BU proposed, it consists of five DC voltage sources and twelve switches to create a twenty-seven level output voltage waveform [36]. The hardware results for the 27-level multilevel converter represent the asymmetric DC voltages that are 10 V, 20 V, 100 V. The value of fundamental frequency is 50 Hz and the R-L load is selected as 5 Ω and 0.1 H, which is acts as a low pass filter across in MLI. The maximum cascade inverter output voltage is 130 V. The investigated new CH-B, the same level of DC voltage (Symmetric) is fed with submodule converter and also different levels in (Asymmetric) voltages are 10 V, 20 V and 40 V is a series-connected inverter. The proposed R-L load across the 15 stage output was verified in asymmetric mode of operation and compared with modifying traditional and conventional MLI's.

A formulated symmetric, hybrid, multi-cell, and asymmetric CH-B inverter proposed, the software has been implemented in MATLAB-Simulink, and DSP prototype model were investigated proposed R-L load conditions with minimum semiconductor devices [37]. The double network circuit, which is combined with CH-B (full bridge) inverter used in 12 switches and 3-DC sources essential for fifteen level output, but conventional MLI are required twenty-four switches needed for same level output. The cascade double network circuit comparison statement is made by both simulation and experimental (R-L load). The results are presented as fewer harmonics levels with the help of varied in a MI value.

Addressed NPC, there is only one DC source with a modified Z-source network for generating required voltage level [38]. The suitable value of capacitances and inductances are designed with different modes of operation such as voltage ripple of a capacitor, voltage stress across the capacitor, and steady-state condition. The FPGA model of SPARTAN-6 is provided the gate signal through S-PWM scheme. The prototype model is verified with R load the rating of 60 W (Lamp load), 230 V output, and 85% efficiency maintain in proposed NPC (Z-SI). An estimated 3 level NPC inverter fed induction motor using to find best switching angle value by varying the MI. The minimum THD level is present RL load by using DSP controller. A utilized a topology, which is consists of inner FC unit and 10-active switches is similar to forming the topology of NPC. The experimental model is proposed different load (R-L) conditions with the rating of 10 Ω–100mH, and 50 Ω–100 mH. The self-voltage balancing FC is less voltage stress on the inverter switches. Therefore, the merits of proposed FC units are,

(1) No feedback control sensor for balancing the FC unit.
(2) The proposed inverter DC-link full utilization voltage level compared with traditional NPC, FC, and CH-B inverter.
(3) High voltage gain.
(4) The proposed inverter can operate both lagging and leading power factor.

The input (200 V) DC-voltage fed with proposed MLI is investigated with the help of desired FPGA switching pulses and optimum MI value [39]. The dynamic performance of the MLI non-linear (R-L) load conditions are produced output Root Mean Square (RMS) voltage 214 Vrms, and current 2.3 Arms with the minimum harmonics presented. A dealt with two-stage cascade-switched diode inverter using for in renewable energy applications. The simulation and experimental methods are verified multilevel output across in R-L load

by using DS1104-real-time simulator. Anew D-C inverter, which can excellently balance the capacitor voltage of DC source. The proposed structure of MLI is required inductor connected in between the switch and as well as diodes. The inverter performance has been verified with R load with the least THD level.

An improved a double FC topology uses a single DC voltage source. The two cells, 23-level proposed structure are added a three high-frequency switch rating while varied up to 700 Hz, and the self-balanced output voltage (220 V) of FC is developed by without any feedback loop [40]. The 2-cell topology can generate 23 level simulation output waveform across the R load (15 Ω), and L load (30 mH). An experimented five-level FC and stacked multi-cell converter to employ in the model of TMS320F2837D. The proposed FC converter is operating MI (0.9) with the output voltage of 200 V. The RMS value of the output current is 2.85 A, and it can low ripple output due to the high inductance at the load in a steady-state condition. FC inverter model both verified in parameters both simulation and hardware circuit, it explores the implementation of the PWM strategy as a control technique for providing pulses to proposed FC inverter. The analysis of the 2 levels, 3 levels, and 5 level inverter Simulink model is presented THD 48%, 42%, and 38%. The hardware demonstrates of 5 level FC inverter is used in a microcontroller, it generates the gate signal through buffer circuit produced the carrier frequency range 10,000 Hz and the resistance load of 100 Ω. The multilevel output is an almost sinusoidal waveform and produces the output voltage is 120 V with the minimum THD level at 18.9% [41].

A five-level reduced number of active switches in MLI compared with the same level of NPC and FC converter [42]. This multilevel converter topology operation is based on variable DC link, switched cell, six-switches, and one FC in the range of 330 μF. The DC cell capacitor is a purpose to balance and control exactly find the proper sinusoidal output voltage waveform. A 2 KW model of FC 7-level inverter proposed, the single-phase 240 V inverter is operated at 120,000 Hz the switching frequency applying for renewable and electric bike application. It can be operated at 50 Hz and R-load inverter parameters are verified in half and full load conditions.

2.1 Problem Statement

The research work aims to develop a 15-level SFI modulation strategies to reduce the harmonics level. The carrier and reference modulation are incorporate with S-PV inverter. The majority of the industries used to generate the quality output voltage by adopting PWM, OLS-PWM, and D-PWM to generate the voltage output in quality. In the proposed method, the bipolar carrier and reference systems for various types of carrier arrangements such as D-PWM schemes are tested. The parameters like MI, switching frequency (f_s), and amplitude are regulated in D-PWM techniques. In a fifteen stages SFI, and DLC modulation approach is analyzed and verified in the following method.

(1) Open loop Digital-PWM.
(2) Closed loop Digital-PWM.

The comparison of open-loop and closed-loop manner in D-PWM methods are verified in the input and output state variable. The CLD-PWM control system of the state variable parameters depends on the multilevel output of the load parameters such as LL, N-LL. The OLD-PWM only depends on the input of PV Parameters. The strategy of

digital counter-based PWM signal depends on the clock frequency and switching frequency on the zero state detector. The comparator is compared to all parameters with duty cycle arrangements. It has been passing through to the logic circuits in the Set-Reset (S-R) flip flop.

2.2 Problem Formulation

The modulation signal is calculated into two various signals given by the Eqs. (2) and (3), there are 2 various signal in PWM the control scheme for high or medium frequency triangular, and low-frequency sinusoidal wave.

$$M_a = \frac{V_{sine}}{\frac{V_{triang}}{2}} \tag{2}$$

$$Y = mx + c \tag{3}$$

$$X \pm \left(\frac{\pi}{2M_f}\right) Y = \frac{r\pi}{2M_f} \tag{4}$$

where V_{sine} is a carrier sinusoidal modulation signal, and V_{triang} is a carrier triangular signal. X is the switching angle, and M_f—modulating frequency ratio. The values of switching angle (θ_1, $\theta_2 \ldots \theta_n$.) should take up to π. The condition of ith odd and even harmonics switching angles are calculated in Eqs. (5–7). Where, i = 1, 2, 3…….n.

$$M_a \sin X = \left(\frac{2M_f X}{\pi}\right) - 2i = 0 \tag{5}$$

$$M_a \sin X = \left(\frac{2M_f X}{\pi}\right) + 2i = 0 \tag{6}$$

The duty cycle can be determined easily by adding the width of the individual pulse of half-period, it's a one-half period of the reference wave signal. The width of each pulse can be found by subtracting from instant even and one odd harmonics, and also another method of harmonics determination is to find switching angle and MI (M_a) value presents in the Eqs. (7–9). The duty cycle and switching angles depend on the M_a and M_f. The RMS output of SPWM is present in Eq. (10).

$$Y = 1 - \sin(M_f X - \frac{\pi}{2}(i - 2) \tag{7}$$

$$M_a \text{Sin } q_i + \sin(M_f q_i \frac{\pi}{2}(i - 1) \quad i = 1, 3, 5 \ldots \tag{8}$$

$$M_a \text{Sin } q_i + \sin(M_f q_i \frac{\pi}{2}(i - 2) \quad i = 2, 4, 6 \ldots \tag{9}$$

$$\mathrm{Vo} = \mathrm{Vs}\sqrt{\frac{\mathrm{p}\partial}{2}} \tag{10}$$

D-PWM method is described as the reference clock- frequency (F_{clk}) given in the Eq. (11), and the modulating duty-cycle of the counter based D-PWM is given by the Eq. (12). Where, F_{PWM}—output frequency, T_{on}—ON time, and T_{PWM}—ON time of the PWM is controlled by the value of K given in Eq. (13).

$$F_{CLK} = 2^{n} * F_{PWM} \tag{11}$$

$$\text{Duty cycle (D)} = \left(\frac{T_{on}}{T_{PWM}}\right) \tag{12}$$

$$K = 2^{n} - 1 \tag{13}$$

where, K is the digital code setting and it has been compared and used to set the value in digital-counter. The counter is operated by a comparator, which is counts each negative to positive or positive to negative transformation in the reference clock. When the value of the K is greater than the counter. At once, the output of the system comparator is high until the context of the counter is larger or equal. Consequently, the output will be produced D-PWM equivalent to the digital (K) code setting for D-PWM model. According to that, the D-PWM method based on the counter is operated in a simple way of (n-bit) digital combinational of logical circuits implemented in the power electronics topology.

3 Proposed Modulation Techniques and its Implementation in SFI to Improve Power Quality

The adequate choice of switching sequences is to improve the P-Q in a multilevel inverter, the various modulation techniques have been used to control of multilevel inverter. The performance and analysis of each modulation technique have been investigated depends on the reduction of THD. Two main categories can be categorized according to the switching frequency of the multilevel inverter, such as fundamental switching frequency, and higher switching frequency. The fundamental switching frequency is called a lower switching frequency of a periodic waveform. In the case of a sinusoidal superposition, the fundamental frequency is the lowest switching frequency in the sum. There is divided into two main classifications; (1) Selective Harmonic Elimination (SHE). (2) Space Vector Control (SVC).

Formulated one commutation per cycle in a multilevel output voltage waveform to be eliminated in a lower order harmonic, and it has been verified in the output of the load. The higher switching frequency is defined as a large number of times the switches change in the state per second. As a result, the losses are proportional to the switching frequency. There is a divide into two main classifications; (1) Sinusoidal Pulse Width Modulation (SPWM). (2) Space Vector Modulation (SVM). An investigated the SPWM techniques in a single carrier signal modulation, it is adopted for reduced harmonics level compared to sine wave value larger than a triangular wave. The SVM technique is referred to as Multicarrier PWM

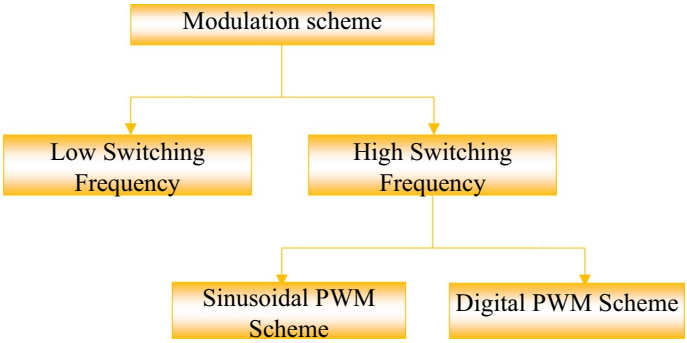


Fig. 6 Modulation control scheme of multilevel inverter [13]

(MC-PWM). SFI obtained MC-PWM using a single chip applied in single (or) three-phase solar fed MLI applications.

3.1 Types of Modulation Methods

These types of modulation have developed the quality of output voltage waveform using higher or medium fundamental switching frequency. Many of the industrial applications using S-PWM and D-PWM to produce switching pulses for several applications are suggested by [43–45], which is one among the high switching frequency with the least difficult process using digital FPGA switching pattern applied in CHB-MLI. They are three control methods used in proposed SFI such as:

(1) Open Loop PWM (OL-PWM).
(2) Open Loop Sinusoidal PWM (OLS-PWM).
(3) Proposed Digital PWM (D-PWM).

These are modulation technique uses with reference signals and related parameters such as MI (ma), switching frequency (fs), and proper signal setting. It is possible to enhance the output of DLC, SFI with variable frequency, and amplitude using for different carrier and reference signals. This strategy is more appropriate for reducing the THD level and

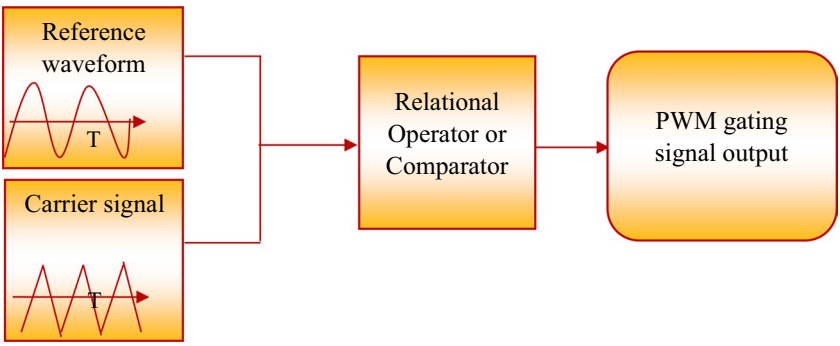


Fig. 7 Modulation control scheme of open loop PWM control [15]

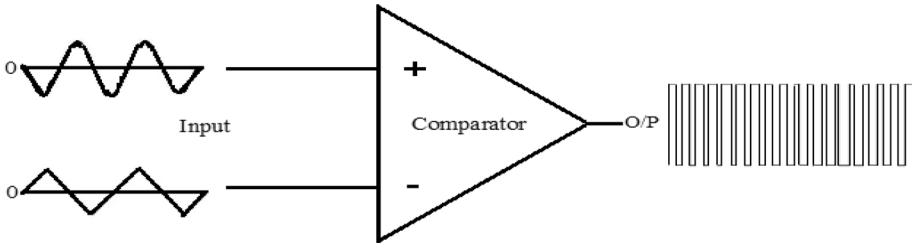
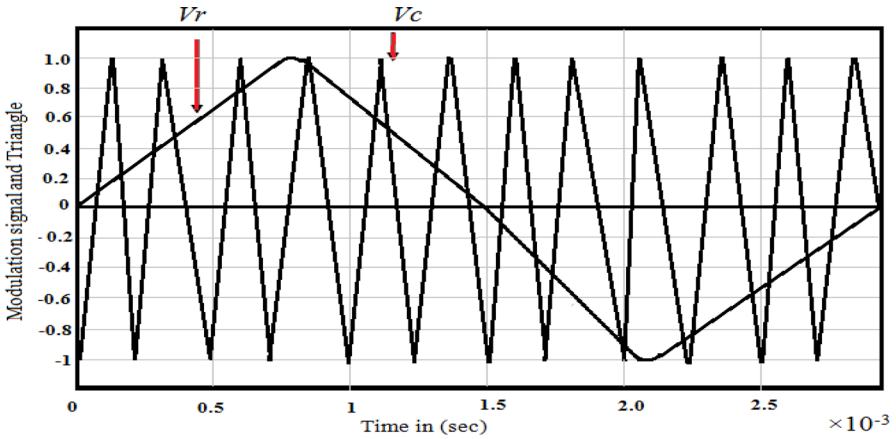
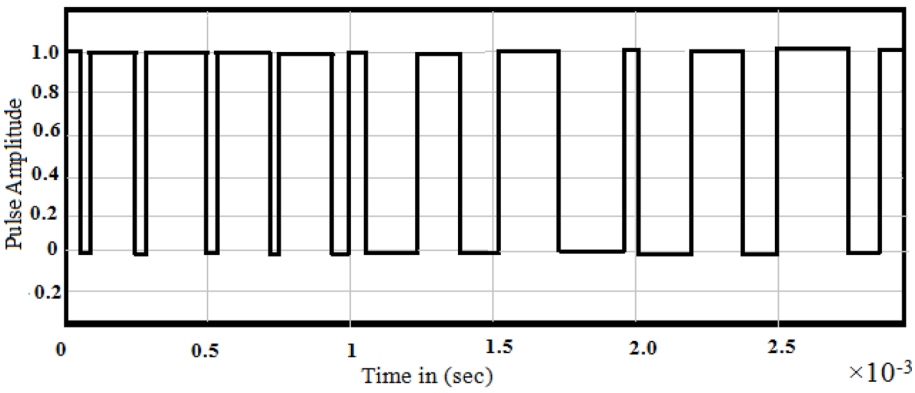


Fig. 8 Basic concept of OLS-PWM generation [18]



(a) Carrier signal



(b) Square wave signal

Fig. 9 **a** and **b** switching scheme of OLS-PWM generation [19]

Distortion Factor (DF) compared to other carrier arrangements techniques. The modulation control schemes of a multilevel inverter are shown in Fig. 6 [13].

3.1.1 Pulse Width Modulation

To optimize the stability of DLC and SFI under working with OL-PWM control, it has been presented as a high-quality analog PWM control signal of the switching multilevel inverter control with the carrier and reference signal. In this section, the comparison is carried out in an open-loop manner. It can be applied basic type of OL-PWM controller is obtained in SFI, the number of switches is used here one MOSFET switch for each converter, and their gate signals are given employing sorting algorithm as shown in Fig. 7 [15].

3.1.2 Proposed Sinusoidal PWM

SPWM is an open loop modulation technique presented in a proposed model. SFI is generating an output of AC voltage from a DC input with the help of switching pulse circuits to reproduce the sinusoidal waveform by generating a single switch per one pulse of voltage per half-cycle. A described the S-PWM, third term of the harmonics injection, and it's revealed that the modulation scheme of F–C MLI is compared to the performance level with equal switch utilization. It has been giving better performance to evaluate the S-PWM approach. The modulations are confirmed that the reference signals for high or medium frequency are applied in a repeating triangular wave. Therefore, that the operating pulses for a switching power circuit is generated in smooth manner. The basic concept of OL-SPWM generation and switching schemes is shown in Figs. 8 and 9 [18, 19].

3.1.3 Proposed Digital PWM

The D-PWM is one of the high switching frequency digital control system, which controls the switching circuit of multilevel converters. In recently digital controls are almost becoming leads in every power electronics applications such as LL, N-LL, washing machine,

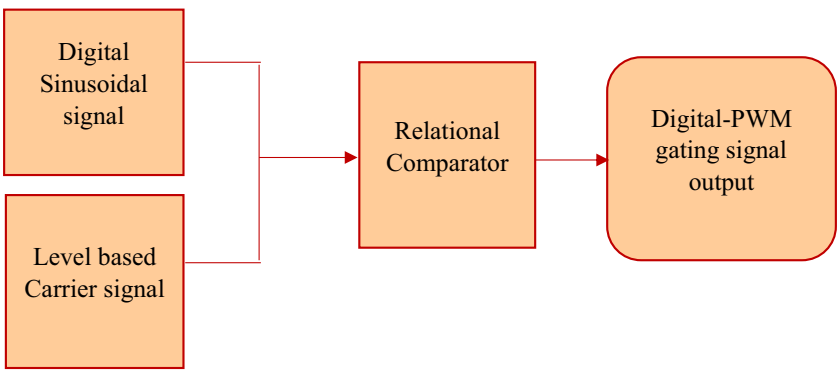


Fig. 10 Modulation control scheme for open loop DPWM control [22]

electric vehicle, etc. when compared to analog and digital controllers, the digital controller is more intelligent to control and potential improvement in power conversion efficiency in dynamic changes of load.

4 Types of Digital PWM

The D-PWM operating schemes are generally classified into two categories.

(1) Open Loop Digital-PWM (OLD-PWM).
(2) Closed Loop Digital-PWM (CLD-PWM.)

4.1 Open Loop Digital PWM

The OLD-PWM technique is a unit step response of transient condition. It can operate in a stable operation to complete in a certain switching period. The control scheme of the power electronics is required to a different carrier and sinusoidal signal into generates digital PWM gating signal output as shown in below Fig. 10 [22]. The carrier signals are used saw-tooth waveform generated by up-down counter devices using in MATLAB/Simulink platform.

4.2 Closed Loop DPWM

CLD-PWM is generally working under state variables due to interference of the load variation. They are dividing the implementation of the control scheme in 3 major categories:

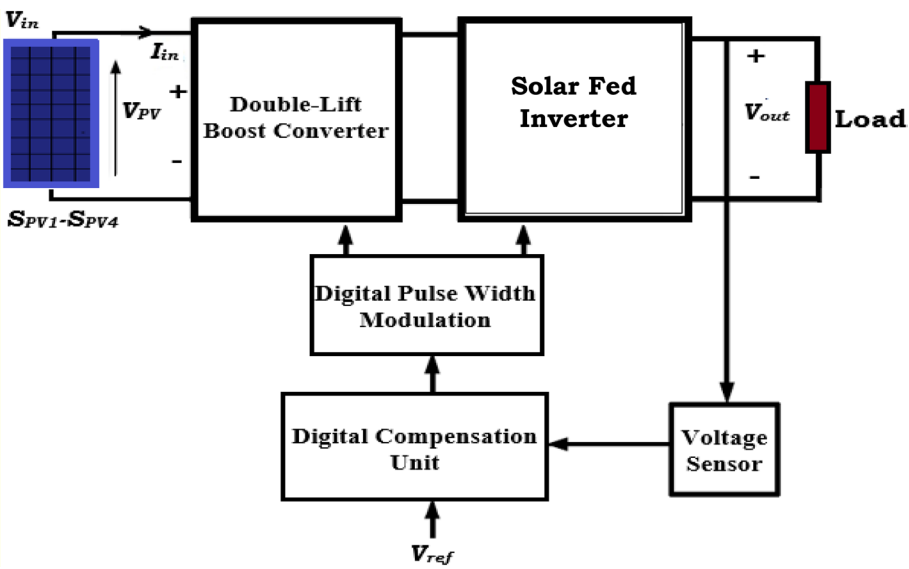


Fig. 11 CLD-PWM controller with switching up/down converters

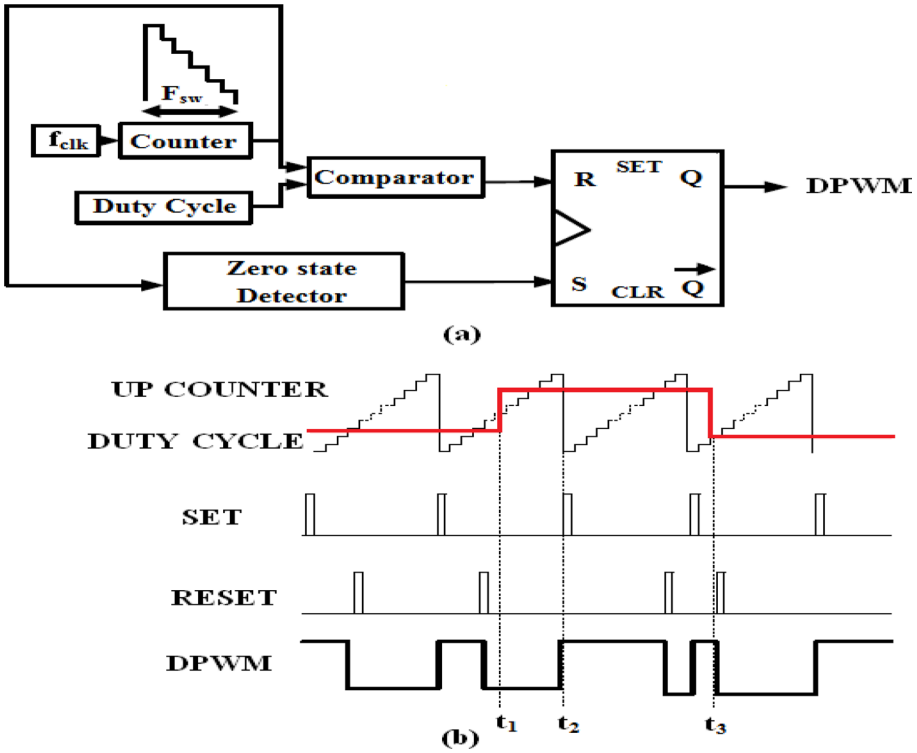


Fig. 12 **a** Negative half cycle DPWM **b** switching waveform

(1) Counter based D-PWM.
(2) Delay line based D-PWM.
(3) Hybrid based D-PWM.

The solar fed proposed SFI is a closed-loop system controlled by output variables of R-load as shown in Fig. 11. It consists of DLC, SFI, Analog to Digital Converter (ADC) unit, voltage sensor, and digital pulse generator/modulator unit. The counter based D-PWM is implemented in a proposed circuit that is increased resolution without unnecessarily increases in clock frequency. The SFI circuit is used in single switch multilevel inverter based on D-PWM which produces accurate results at a high computational speed. The delay line and hybrid-based PWM are not suitable for the single MOSFET switch using the proposed circuit in a multilevel output waveform.

4.3 Types of Counter Based DPWM Method

The counter based D-PWM are operated at three major categories:

(1) Down counter—Leading edge counter triggering DPWM.
(2) Up counter—Trailing edge counter triggering DPWM.
(3) Up/Down counter—Dual edge triggering DPWM.

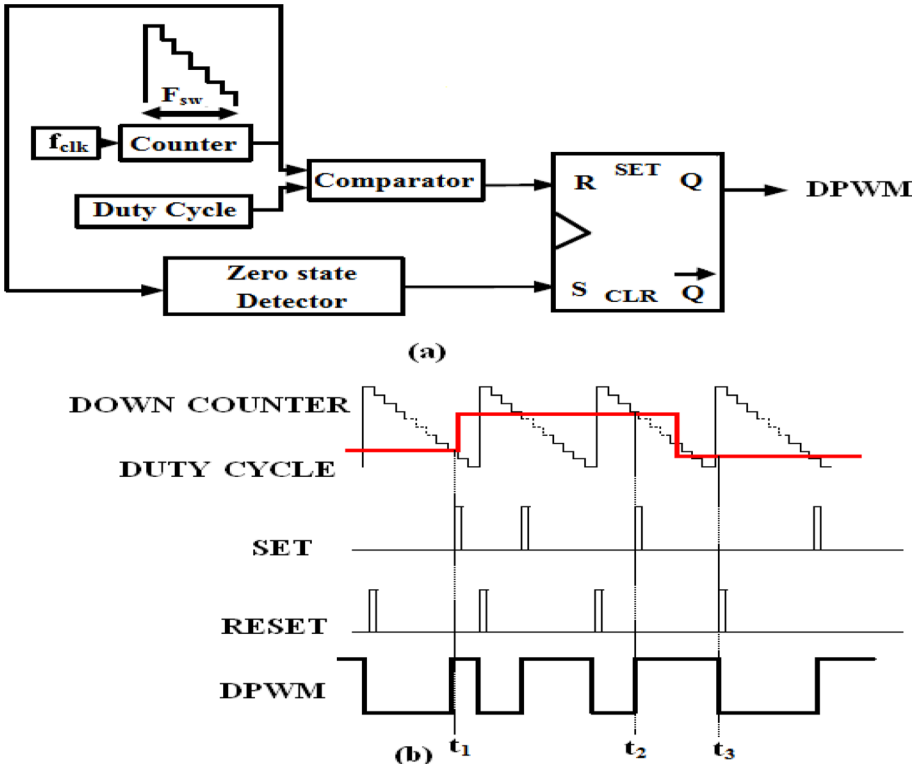


Fig. 13 **a** Positive half cycle DPWM **b** switching waveform

The change of positive/negative half cycle uses in delay-based hybrid triggering (Combination of counter and delay line D-PWM) are not suitable to produce in the form of AC output waveform, since the triggering the level is only varied in first or second quadrant i.e., a modified in D-PWM modulation in multilevel inverter circuit and it offers the continues duty cycle as per the dynamic change of load variations. Output voltage is regulated with the reduction of modulation delay. The D-PWM approach in leading-edge counter operates at a negative half cycle of the switching circuit as shown in Fig. 12. The second model of trailing edge or up counter triggering is operated at a positive half cycle of the switching a multilevel circuit as shown in Fig. 13.

The proposed model of the DLC and SFI is operated in a dual-edge or Up/Down counter as shown in Fig. 14. The first one is positive switching half cycle either up or down counter modulation, the second one is negative switching half cycle act as either up or down counter modulation scheme that means, the edge PWM output is either right-aligned edge triggering or another left-aligned edge triggering modulation scheme. These two output D-PWM are connected to the AND-NOR gate, which is generated the output as known as dual digital PWM edge trigger. The ON (1) and OFF (0) digital sequence of the state is starting from 0001 to 1111 in a positive (0°–180°) switching half-cycle triggering, and the negative (180°–360°) switching half-cycle triggering is started from 1111 to 0001. It has been a move towards the reverse direction of the state triggering. The switches are operated with dual counter-based triggering, it

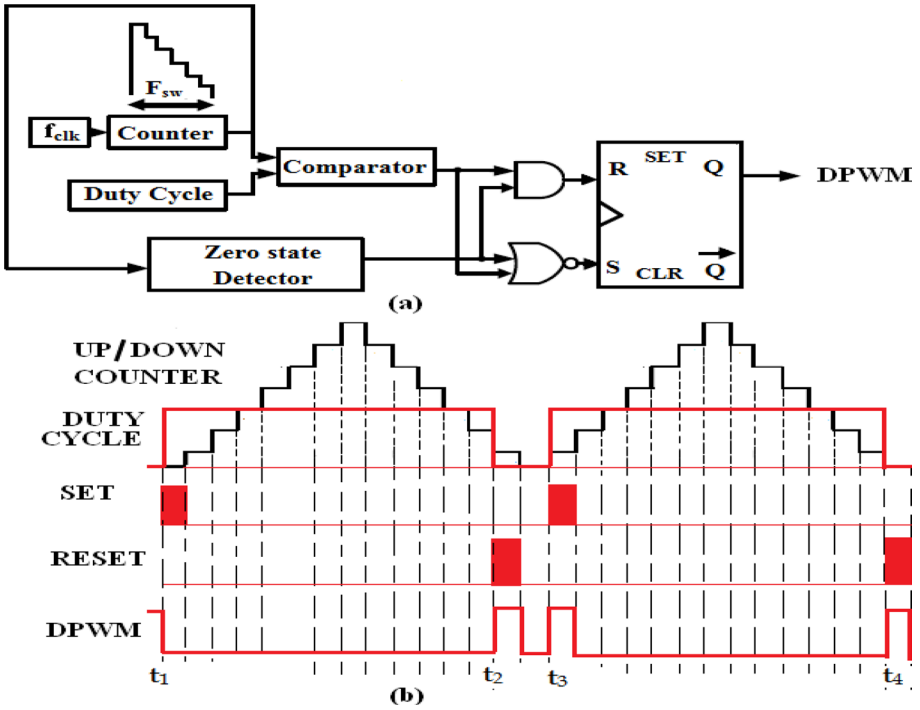


Fig. 14 **a** Proposed up/down counter DPWM triggering SFI **b** switching waveform

Table 2 ON and OFF state proposed triggering method

Positive triggering								Negative triggering							
Inverter switch (S_2)				Output voltage (V_{out})	Inverter switch (S_2)				Output voltage (V_{out})	Inverter switch (S_2)				Output voltage (V_{out})	Inverter switch (S_2)				Output voltage (V_{out})
0	0	0	1	15	1	1	1	1	225	0	0	0	1	−15	1	1	1	1	−225
0	0	1	0	30	1	1	1	0	210	0	0	1	0	−30	1	1	1	0	−210
0	0	1	1	45	1	1	0	1	195	0	0	1	1	−45	1	1	0	1	−195
0	1	0	0	60	1	1	0	0	180	0	1	0	0	−60	1	1	0	0	−180
0	1	0	1	75	1	0	1	1	165	0	1	0	1	−75	1	0	1	1	−165
0	1	1	0	90	1	0	1	0	150	0	1	1	0	−90	1	0	1	0	−150
0	1	1	1	105	1	0	0	1	135	0	1	1	1	−105	1	0	0	1	−135
1	0	0	0	120	1	0	0	0	120	1	0	0	0	−120	1	0	0	0	−120
1	0	0	1	135	0	1	1	1	105	1	0	0	1	−135	0	1	1	1	−105
1	0	1	0	150	0	1	1	0	90	1	0	1	0	−150	0	1	1	0	−90
1	0	1	1	165	0	1	0	1	75	1	0	1	1	−165	0	1	0	1	−75
1	1	0	0	180	0	1	0	0	60	1	1	0	0	−180	0	1	0	0	−60
1	1	0	1	195	0	0	1	1	45	1	1	0	1	−195	0	0	1	1	−45
1	1	1	0	210	0	0	1	0	30	1	1	1	0	−210	0	0	1	0	−30
1	1	1	1	225	0	0	0	1	15	1	1	1	1	−225	0	0	0	1	−15

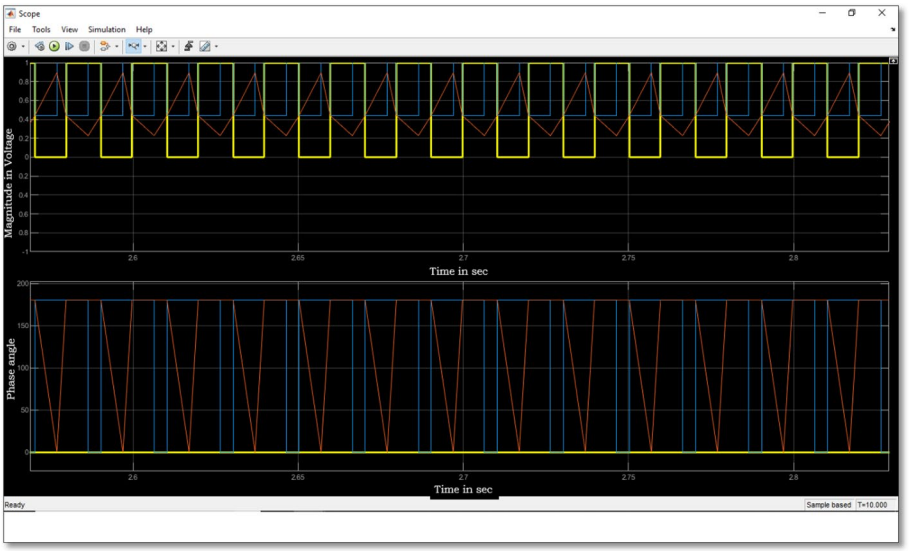


Fig. 15 OLP-WM signal

is triggered both positive and negative half-cycle as shown in Table 2, and it gives the triggering sequence requirement of the proposed counter design. The counter is working as a conventional model, which is an act at the logic circuits combination of up/down counter, and the sate variables depend on the load variations. Furthermore, the merits of the proposed D-PWM system is successfully minimized the duty cycle error from the capacitor error.

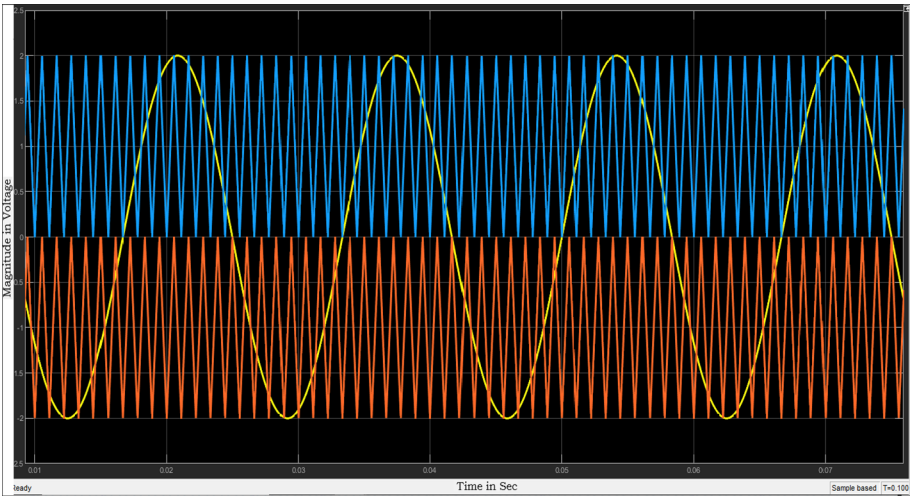


Fig. 16 OLS-PWM signal

5 Simulation Results

The simulation of S-PWM and D-PWM method has been verified by using MATLAB R2020a/R2019a-Simulink tool for all modulation schemes. The fifteen level SFI output voltage can be obtained by using the same value of DC output in a single PV module nominal voltage and current is $V_{dc} = 64$ V, and $I_{dc} = 5.96$ A. In general, there is 2 module voltage conversation presented in the proposed system, the first one is DLC, and SFI. In each converter are presented in a single switch, a total number of seven diodes, and twelve capacitors using for resistive load condition. The gate signals of the 2 switches have been generated both OL-PWM, S-PWM carrier reference signal using for in this simulation.

The parameters are used MI $(M_a) = 1$, $Mf_s = 1000$–5000 Hz, both DLC and proposed inverter. The output (O/P) frequency 50 Hz was applied across the dynamic changes of load ($R = 50\ \Omega$). The proposed S-R flip flop reference of the switching frequency is 1.5 MHz, and the clock frequency is 15 MHz respectively. A five-level cascade digital PWM control switching patterns that are compiled by FPGA unit. A described the symmetric 15–level inverter, the switching strategy was proposed in S-PWM method, which comprised the bipolar six-carrier signal for the same frequency level, amplitude, and phase disposition carrier arrangements strategy was employed. Figure 15 shows the OL-PWM, which is considered as a usual sine and triangular wave arrangements. The carrier arrangements are lower than reference sine wave signal with the range of 0.2 up to 0.8 amplitude, and 0 up to 1.0 amplitude with the range of phase value 180°. The OLS-PWM, single carrier sinusoidal 2.0 amplitude and carrier arrangement 2.0 amplitude references are switched across in a resistive load condition with the range of 180° phase value as shown in Fig. 16.

The D-PWM are operated in both conditions, (1) OLD-PWM, (2) CLD-PWM, which is tested and verified in the present model. The simulation of OLD-PWM is compared with a level based carrier signal and digital sinusoidal carrier signal amalgamated with reference arrangements. The first counter is saw tooth waveform stars from 0 to 2.0 V of a carrier

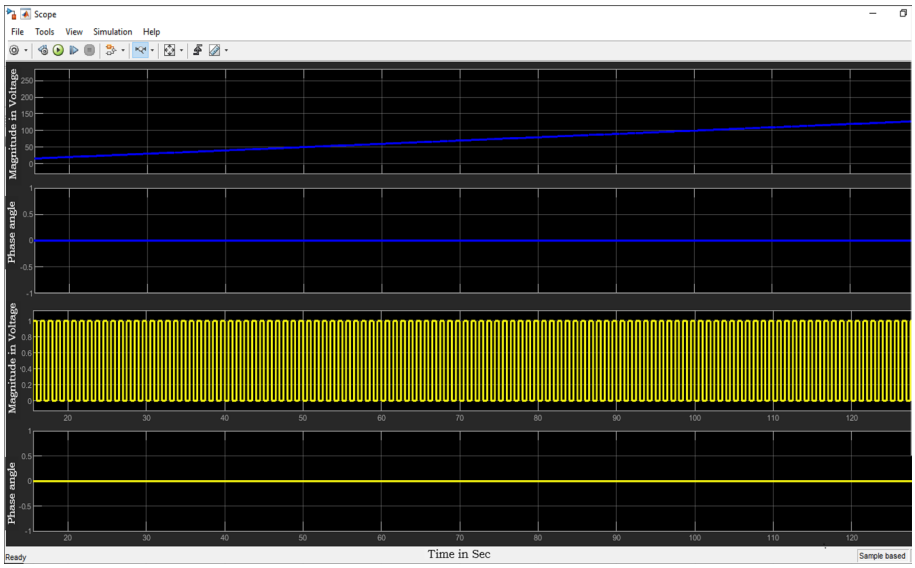


Fig. 17 OLD-PWM signal

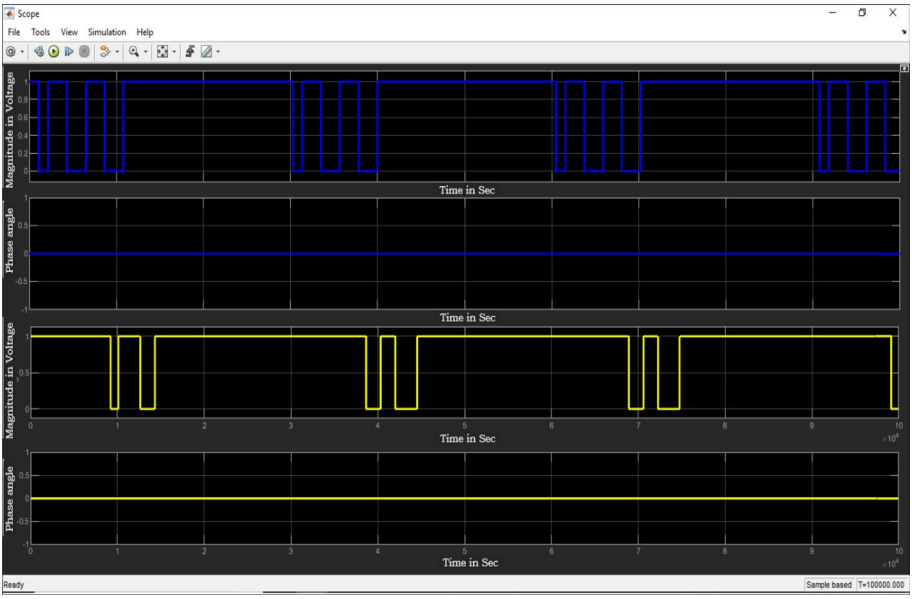


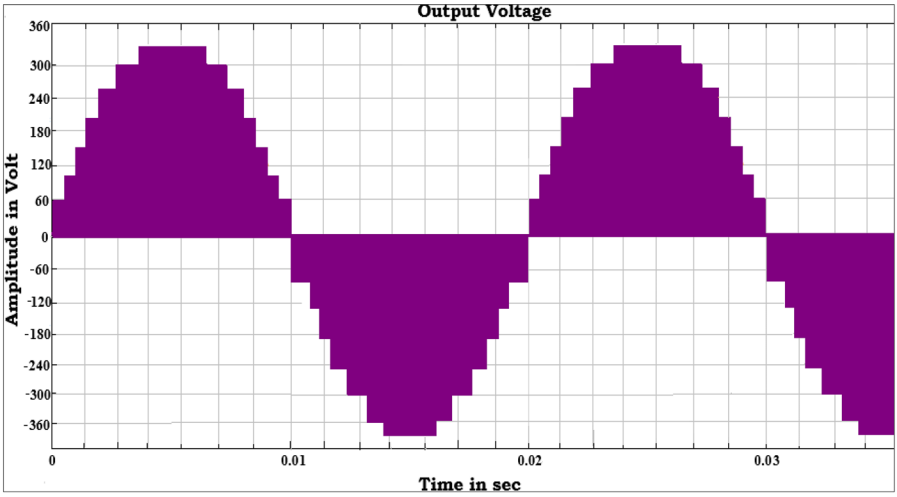
Fig. 18 CLD-PWM signal

signal, and the second counter is saw tooth waveform starts from 2.0 to 4.0 V of the carrier signal as shown in Fig. 17. In the same way, each saw tooth wave carrier signal amplitude is should be constant amplitude and frequency of 2000 Hz. In the range of 1000–2000 Hz can be used in a variable range of frequency to significantly reduce the level of THD. A CLD-PWM is approximate to generate by stepped digital square wave by using 8 bit up-down counter. This is implemented by a digital counter based comparator with flip flop S-R logic combinational circuits. The phase value is zero but, the magnitude of voltage is varied as per the digital pulse also varied in Fig. 18. The state variables are increased by load voltage, but it can be controlled by the digital modulator.

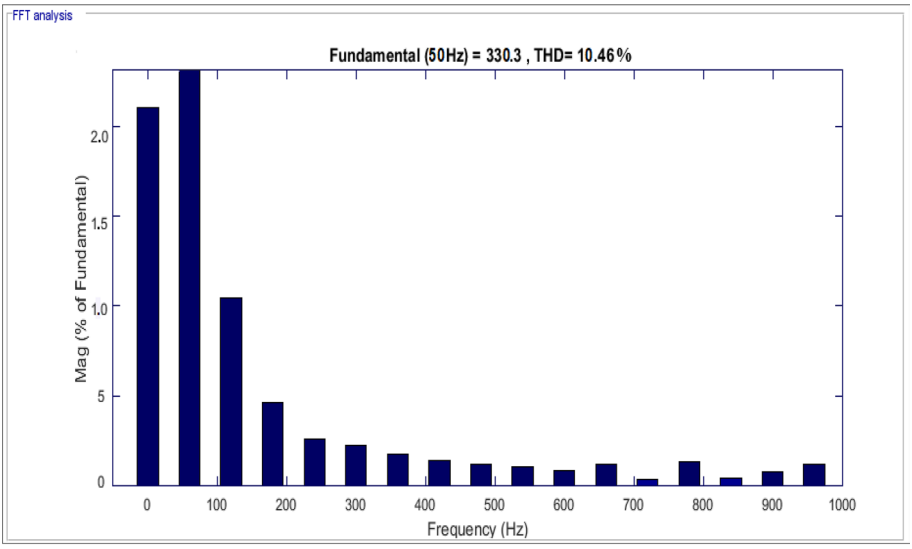
The Up/Down counter or dual-edge triggering CLD-PWM strategy is continuously compared to a counter and duty cycle arrangements both of the half-cycle (positive and negative-cycle). If the duty cycle is lesser than the counter value, the D-PWM is set to high. The first half switching cycle is appeared in leading triggering and another half switching cycle serves as the trailing edge triggering with the help of S-R flip flop. Figure 19a–h display the variation of voltage levels are presented with minimum harmonics distortion in fifteen level SFI.

6 Hardware Results

The Solar-PV rating should be taken as 305-watts for both simulation and hardware test, hence the solar module is tested at STC. The input solar power is developed by four PV array, it's consists of a single module series-connected DLC and SFI. The design of the circuit is fifteen level, and the solar fed SFI is used to apply in R-load application. Figure 20 displays the experimental view for the overall system unit, and its 15 level MLI uses only a single switch (MOSFET), where the FPGA clock pulses are up to 50 MHz. The voltage



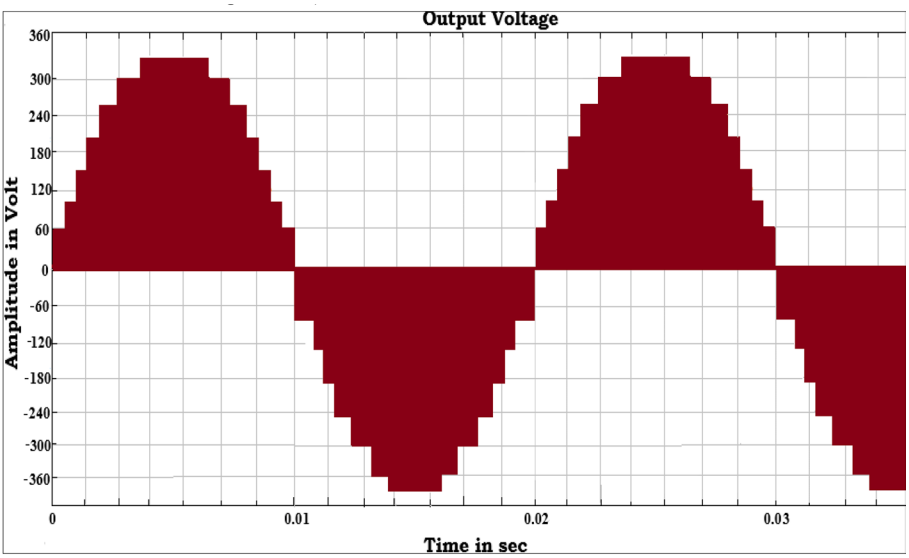
a) OL-PWM using for SFI output voltage



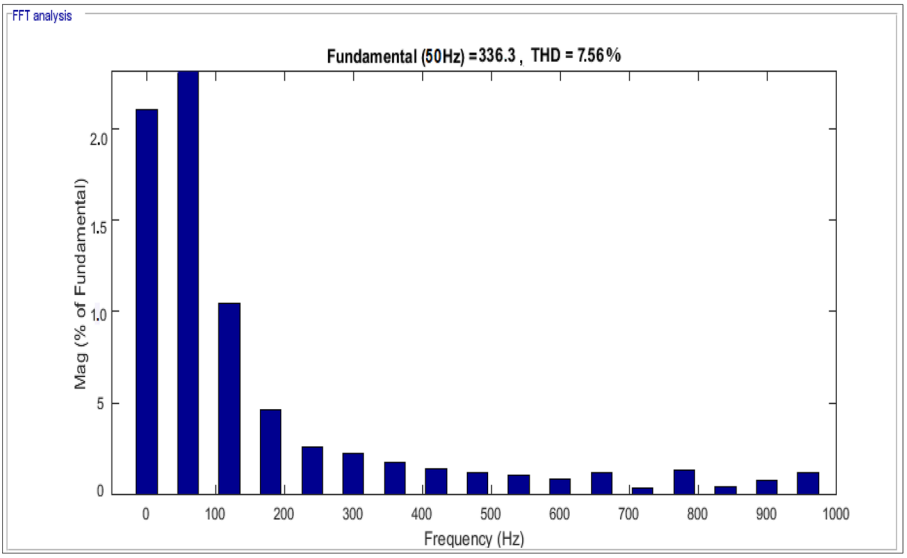
b) Minimum harmonics level of OL-PWM

Fig. 19 **a** OL-PWM using for SFI output voltage. **b** Minimum harmonics level of OL-PWM. **c** OLS-PWM using for SFI output voltage. **d** Minimum harmonics level of OLS-PWM. **e** OLD-PWM using for SFI output voltage. **f** Minimum harmonics level of OLD-PWM. **g** CLD-PWM using for SFI output voltage. **h** Minimum harmonics level of CLD-PWM

drops through both DLB converter and SFI switching diode is 0.7 V. This SFI prototype model switches on MOSFET (IRFP460) by series voltage and along with the capacitor bank (1500 µF) or MLI capacitor bank C_6–C_{12}. The positive half cycle (0–180°), and a negative half cycle (180°–360°) are composed of an electronic relay (KEMET-EE2) 2P2T switch unit. The relay unit pulses are functioning at 20 ms and the operating frequency from 1000 to 5000 Hz. These relays are used to positive half cycle (0–180°) is made by



c) OLS-PWM using for SFI output voltage

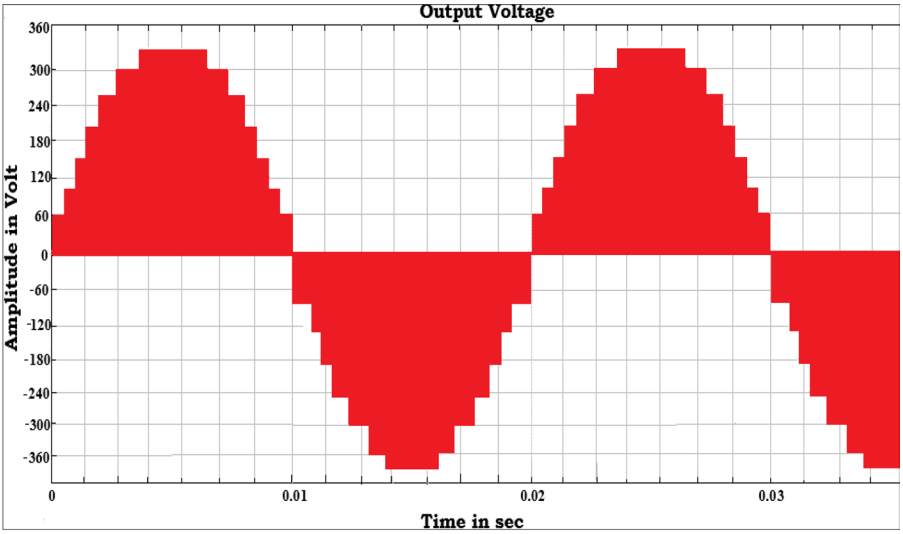


d) Minimum harmonics level of OLS-PWM

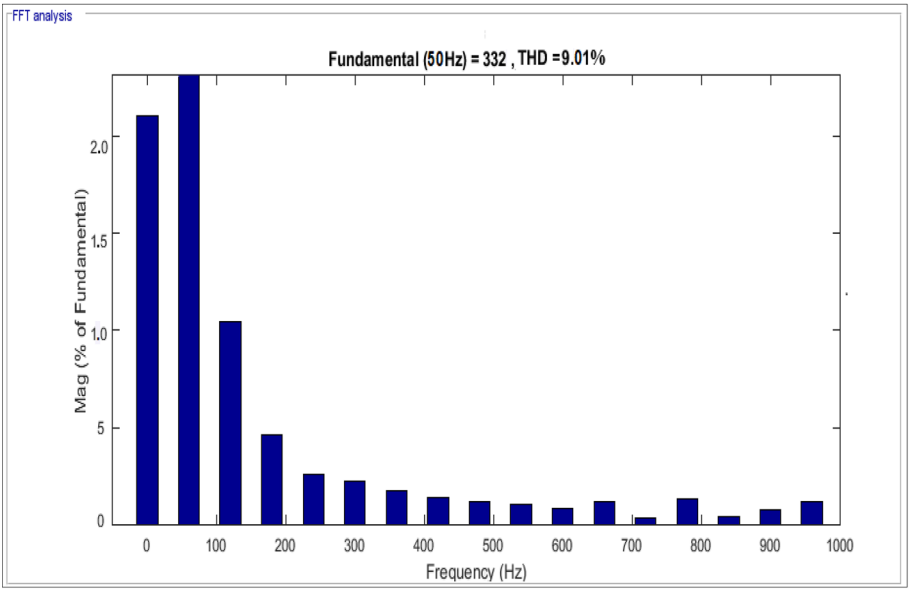
Fig. 19 (continued)

charging-discharging capability, the negative half cycle (270°–360°) is made by charging–discharging by the 2P2T-relay unit switch.

The system produced VHDL code into the test bench. The test bench is simulated for the verified D-PWM signals through the Spartan-Xilinx platform kit. The Verilog clock divider is simulated and tested in parallel programming of Hardware Description Language



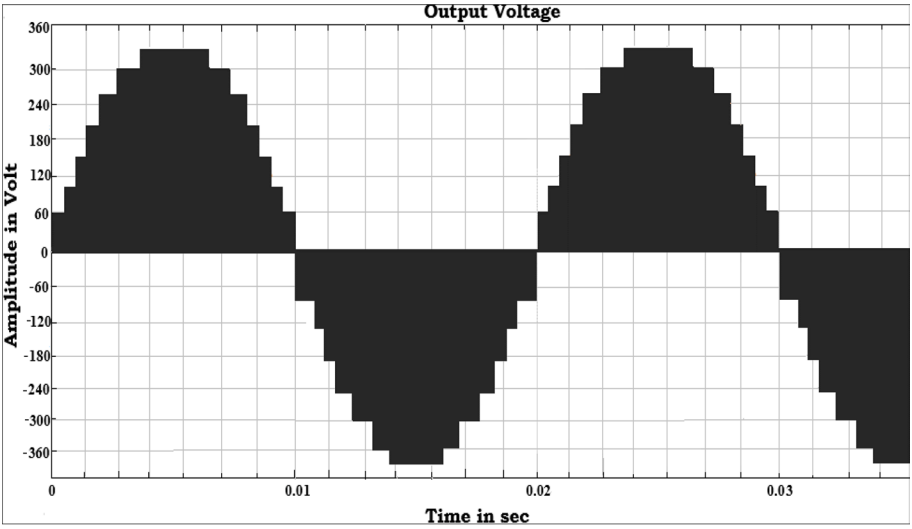
e) OLD-PWM using for SFI output voltage



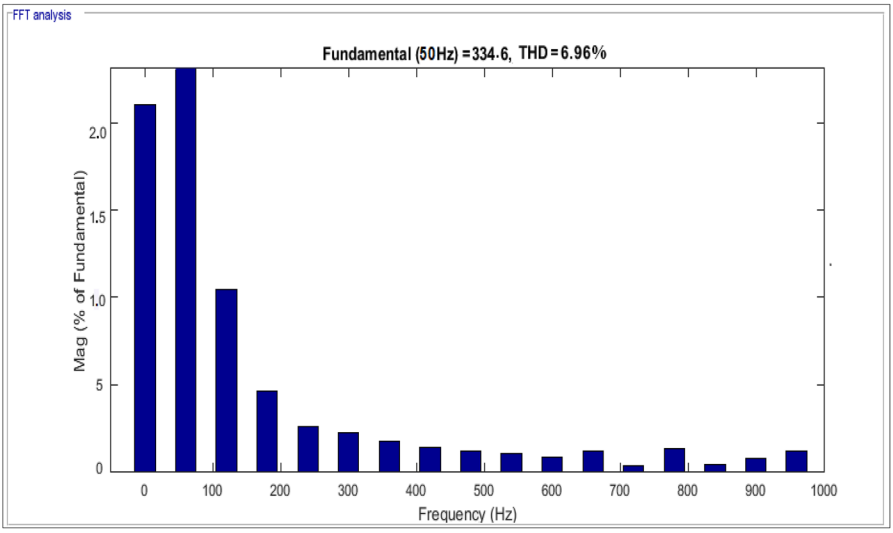
f) Minimum harmonics level of OLD-PWM

Fig. 19 (continued)

(HDL) code verified with the Xilinx 3AN kit. The development of SFI is used to FPGA controller to generate the D-PWM, S-PWM pulses in an open-loop manner as shown in Fig. 21a, b. Figure 22a, b shows that the experimental output results are verified at 230 Vrms, 250 Vrms with frequency (50 Hz) at variable resistive load conditions using D-PWM and S-PWM modulation scheme. The proposed multilevel inverter can work at a



g) CLD-PWM using for SFI output voltage



h) Minimum harmonics level of CLD-PWM

Fig. 19 (continued)

varying frequency and amplitude from 1000 to 3000 Hz with a different carrier and reference signals. This strategy is more appropriate for reducing the THD level compared to other carrier arrangements techniques. Based on the simulation comparative analysis of D-PWM, and S-PWM methods, it is found that a lower THD value of 6.06% (S-PWM), 6.90% (D-PWM) is achieved by R load.

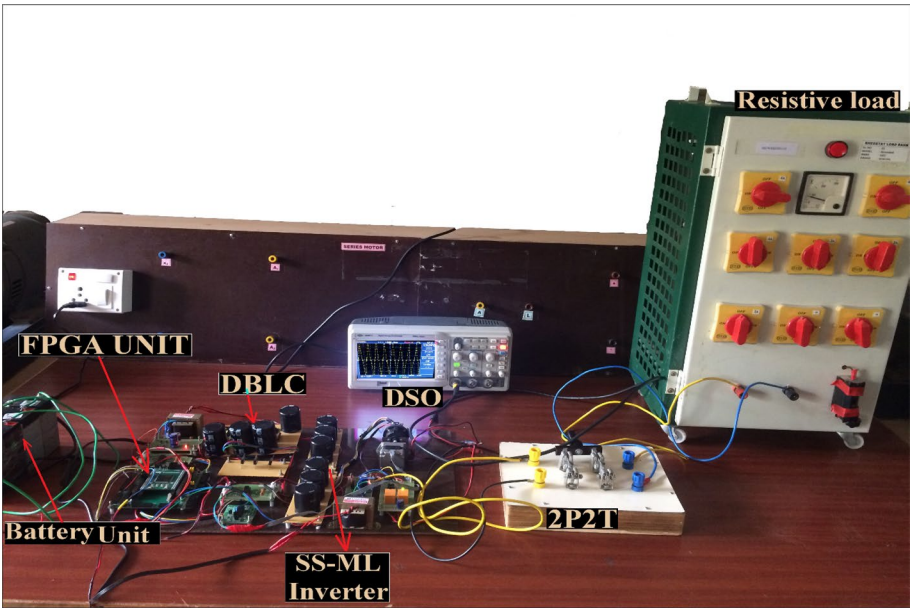
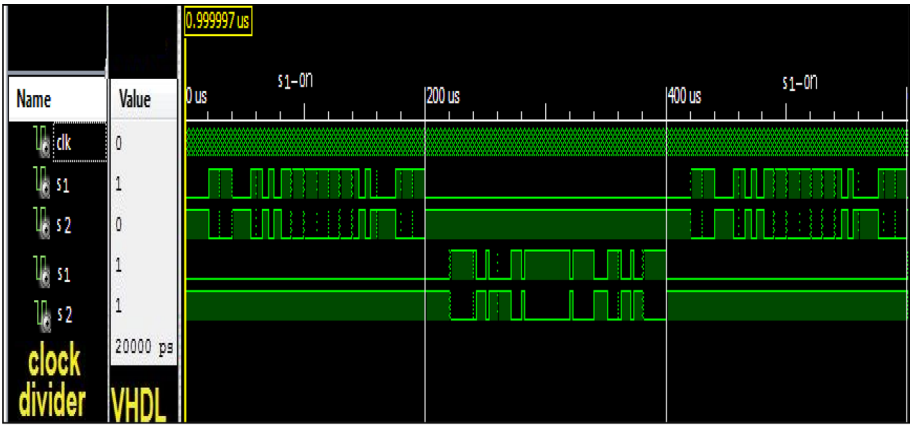


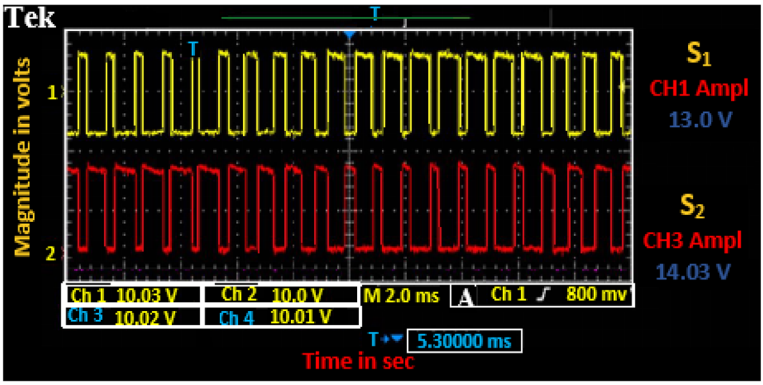
Fig. 20 Experimental Setup

The maximum reactive power is developed in a series capacitor bank using a SFI and fifteen voltage level of the minimum harmonics are presented in Fig. 23a, b. The simulation and hardware results are verified in Table 3, it shows the details of the comparison in OL-PWM, OLS-PWM, OLD-PWM, and CLD-PWM technique for presents in the simulation of SFI. The hardware results are shown in Table 4, the S-PWM and D-PWM technique to achieve the minimum THD levels are presented compared to other modulation technique. Proposed inverters drawbacks are predominantly for large ones dissipate a power from the input source, then the resulting inefficiency of the waste power for inverter power conversion. Which is dissipated around 10 W of power at no load conditions. Because, the proposed inverter consume 110 W means the battery will deplete in just two hours. If the proposed inverter are connected to monitor, then it will result in a total power consumption around 120 W, due to changing load impedance values and the heat dissipation from each semiconductors. These types of problem keep arising with all newly developed inverters.

The maximum function of a relay pulse is 20 ms, and the working frequency ranges from 300 to 3 kHz. In a series capacitor device, the electronic relay has been operated for both positive and negative cycles. The capacitor switching terminal output voltage is $V_0 - V_7$ (or) $V_7 - V_0$, and it may interface with the voltage of the resistance or inductive load. It has the fewest low harmonic levels in the FFT spectrum up to the 17th order. When the PV module is combined with an off-grid (R and RL) load that suggested inverter supports reactive power in an electric load linked system without the need of any extra filter equipment. The simulation and hardware results are almost the same, especially for D-PWM method. The minimum THD levels are present in



a) Switching arrangement of DPWM



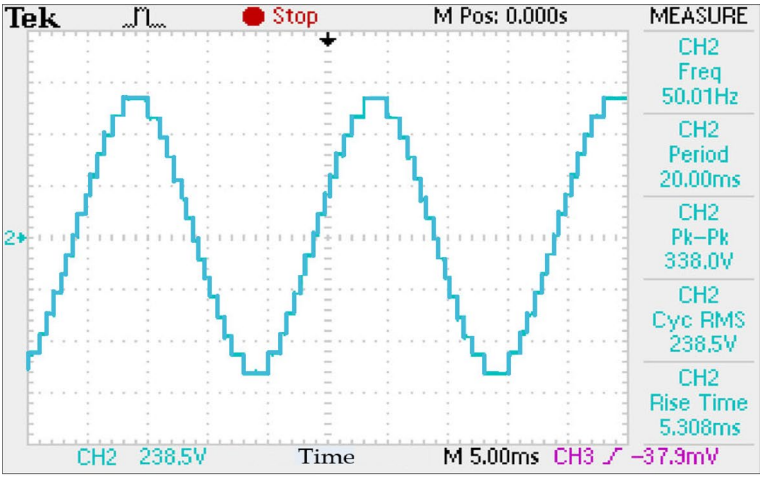
b) SPWM Switching pattern

Fig. 21 **a** Switching arrangement of DPWM. **b** SPWM switching pattern

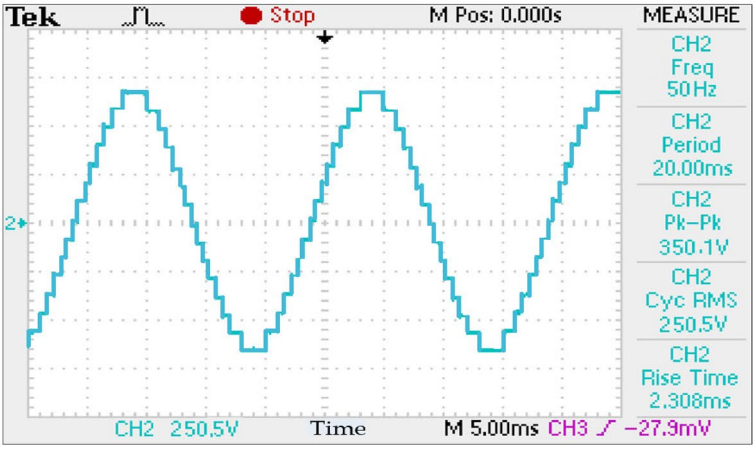
D-PWM, and S-PWM (6.90% and 6.06%) compare with other modulation methods. The reduced output harmonics levels are presented in a power quality analyzer, and most probably the maximum electrical domestic loads are operated at the same voltage level.

7 Conclusion and Future Scope

This section is illustrated in several carrier PWM techniques for fifteen level SFI solar fed module prescribed. For the proposed modulation inverter topologies have been examined with a bipolar different type of carrier, reference signals, and their outputs are estimated.



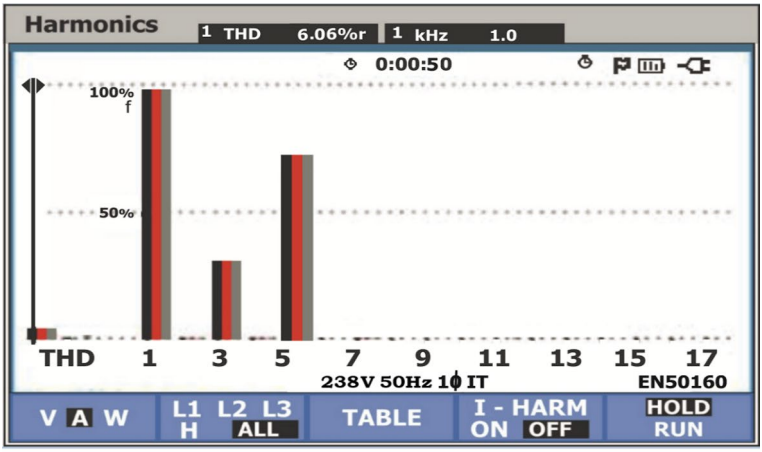
a) Output voltage of the SFI using SPWM



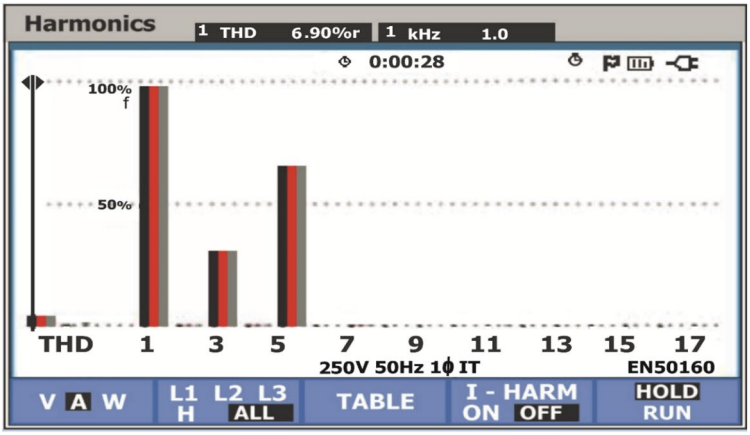
b) Output voltage of the SFI using DPWM

Fig. 22 **a** Output voltage of the SFI using SPWM. **b** Output voltage of the SFI using DPWM

The configuration of the solar panels and different PWM techniques such as digital and analog methods has been evaluated and verify with SFI. The findings of the simulation and experimental were compared with a minimum THD in bipolar S-PWM and D-PWM almost the same results obtained, which is better achievement of the proposed objective work. To generate the PWM pulses for each converter switches, and it can measure the output voltage in DSO and power quality instruments. The 305 W solar system is investigated with the FPGA controller. The variable frequency of OLS-PWM in experimental results and the simulation of CLD-PWM results are verified under the lowest THD. The harmonics level has been compared into the other modulation-carrier arrangements like as OLD-PWM, and CLS-PWM. On the basis of future work can be carried out under the following possibilities for extending the research work present in this proposed work:



a) THD analysis of dynamic change of R load using S-PWM



b) THD analysis of dynamic change of R load using D-PWM

Fig. 23 **a** THD analysis of dynamic change of R load using S-PWM. **b** THD analysis of dynamic change of R load using D-PWM

(1) The recommend proposed inverter can be applied to the three-phase systems and also it may be applied to wind-based conversation for power quality development by using Internet of Things (IOT). The application of IOT in renewable energy (i.e., solar, wind) production involve sensors that are implemented in Distribution, transmission, and generation.
(2) Other intelligent and optimization approach such as Artificial Neural Network (ANN)-Fuzzy tuned approach, Meta-heuristics and differential evolutionary algorithm have to applied in a proposed MLI.
(3) This proposed MLI may apply in a grid interface approach.

Table 3 Comparison of simulation results with the existing topologies and proposed topology

Reference paper	Techniques	Level	THD (%)
Modulation techniques			
[40]	S-PWM	13	9.46
[41]	S-PWM	17	9.2
[42]	S-PWM	11	10.11
[43]	S-PWM	15	9.32
[44]	S-PWM	15	10.26
[45]	S-PWM	15	10.77
[39]	D-PWM	15	13.27
Proposed SFI	OL-PWM	15	10.46
	OLS-PWM	**15**	**7.56**
	OLD-PWM	15	9.01
	CLD-PWM	**15**	**6.96**

Table 4 Comparison of hardware results with the existing topologies and proposed topology

Reference paper	Techniques	Level	THD (%)
Modulation techniques			
[42]	S-PWM	13	10.5
[43]	S-PWM	9	13.8
[44]	S-PWM	15	38.7
[45]	S-PWM	9	13.46
[40]	S-PWM	11	13.8
[41]	S-PWM	15	12
[39]	D-PWM	7	8.5
[38]	D-PWM	5	14.9
Proposed SFI	**OLS-PWM**	**15**	**6.06**
	OLD-PWM	**15**	**6.90**

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Data Availability Enquiries about data availability should be directed to the authors.

Declarations

Conflict of interest Author declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper. There is no conflict of interest.

Ethical Approval This article does not contain any studies with human participants or animals performed by any of the authors.

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