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A Low-Noise Dynamic Comparator with Offset Calibration for CMOS Image Sensor Architecture*

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A low-noise, high-speed, low-input-capacitance switched dynamic comparator (SDC) CMOS image sensor architecture is presented in this paper. The comparator design occupying less area and consuming lesser power is suitable for bank of comparators in CMOS image readouts. The proposed dynamic comparator eliminates the stacking issue related to the conventional comparator and reduces the offset noise further. The need for low-noise, low-power, area-efficient and high-speed flash analog-to-digital converters (ADCs) in many applications today motivated us to design a comparator for ADC. The rail-to-rail output swing is also improved. The input capacitance is reduced by using shared first-stage technique. The comparator is designed with constant I_d/g_m biasing to suppress the environmental drift. The simulation results from 45-nm and 65-nm CMOS technologies confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced. The maximum clock frequency of the proposed comparator can be increased to 3.5 GHz and 2.2 GHz at supply voltages of 1 V and 0.6 V, respectively. Simulations are carried out using predictive technology models for 45 nm and 65 nm in HSPICE.

Keywords: Double-tail comparator; switched dynamic clocked comparator; flash ADC.

1. Introduction

In the image sensor architecture the photodiode is sampled multiple times during an exposure. When the photodiode voltage drops below the comparator's threshold

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voltage, charge feedback is applied to cancel the photogenerated charge. This prevents charge saturation of the photodiode under high illumination which greatly extends the image sensor's dynamic range. In flash analog-to-digital comparators (ADCs) comparators are the basic building blocks which transfer the difference of the input voltage and reference voltage to the next stage. The design of the comparators should meet the requirements based on the applications.[1] In bio-medical applications, where data acquisition units are present, the comparators should be fast and less noisy. They should provide sufficient gain to the difference of inputs. Nowadays latched comparators play vital roles in all ADCs due to the controllability through a clock signal. The dynamic latched comparator circuit is being widely used as a sense amplifier in dynamic RAMs and ADCs. But the mismatches between the transistors and circuit parameter deviations lead to large input offset current. The offset voltage can be overcome by preceding the dynamic latch using linear amplifier. The offset can be reduced by designing the comparator with differential input stage. In recent times the clocked regenerative comparators were used in many applications due to their behavior to take fast decisions. The circuits have high input impedance, sufficient rail-to-rail output swing and no static power consumption. But the features like high speed, low offset voltage and huge output swing made dynamic comparators to be dominant in the field. This work focuses on designing a dynamic comparator with less noise for the flash ADC used in System-on-Chip application. A vast survey is made on different comparators. He *et al.*[2] analyzed the random offset voltage and reported offset sources of noise are the internal positive feedback and transient response. The operating point using balanced method was analyzed using explicit expressions for offset voltage, threshold voltage and parasitic capacitances mismatch. Jeon and Kim[3] presented a novel dynamic latched comparator and reported that the design provides higher driving capacity when compared to the conventional dynamic comparators (CDCs). Their work was focused on the improvement in the regenerative latch stage with two additional inverters inserted between the input and output stages of the conventional double-tail dynamic comparator (DTDC). The work was done on 90-nm CMOS technology and a 19% less offset voltage was reported maintaining the same area and power consumption.

Nikoozadeh and Murmann[4] presented the offset due to load capacitor mismatch. Offset noises are an important issue in comparators. When the offset noises are not eliminated it will lead to saturation of output. Figueiredo and Vital[5] presented existing solutions to minimize the noises present in the latched comparator. The demonstration was done using 180-nm CMOS technology. Two methodologies were proposed for the removal of noise based on sampling switches and asynchronous reset. Understanding of amplification and noise removal in the comparator was one of the problems. Lu and Holleman[6] reported a high-precision comparator with tuned offset cancellation. The reported time domain-based bulk tuned offset cancellation technique reduces the input-referred noise. For the noise removal additional power

was consumed. A similar analysis of comparator with respect to noise was presented by Chan *et al.*[7]

The comparators can compromise on the number of transistors to improve noise immunity and amplification. A less number of transistors helps the design to work fast but the offset cancellation[8] will not be taken care in the design. Goll and Zimmermann[9] designed a comparator working with a supply voltage below 0.7 V with minimum delay in 65-nm CMOS. But the comparator suffers in current driving capability. Huang and Wang[10] proposed a priority encoder-based high-performance, power-efficient CMOS comparator featuring multiple output domino logic. The paper presents a post-format recreation result demonstrating a 64-bit comparator. The proposed work was implemented in a 3-V, 0.6 nm CMOS technology and was 16% quicker, half smaller and 79% more power-efficient. In most of the ADCs the offset values are so troublesome which need a comparator of less offset. For a 7-bit, 1.4-GS/s ADC, Nakajima *et al.*[11] proposed an offset drift suppression technique. The ratio between the transconductance and drain current was kept constant to suppress the offset drift. Zhu *et al.*[12] proposed a dynamic comparator which reduces the threshold voltage. The comparator was designed using a preamplifier and latch. The comparator suffers from offset errors due to transistor size mismatch. Babayan-Mashhadi and Lotfi[13] proposed a low-voltage, low-power double-tail comparator utilizing the regenerative principle and current boosting. The authors investigated the comparator delay and the tradeoffs in element comparator outline. In addition, the paper proposes a traditional double-tail comparator for low power and quick operation even with little supply voltages. The reported post-format reproduction results in a 0.18-μm CMOS innovation affirming the examination results. Some designs use BICMOS technology.[14]

A switched dynamic comparator (SDC) was proposed by Xu *et al.*[15] which eliminates the limitation on the maximum operating speed due to regeneration time. The design consists of a dynamic amplification stage with a NAND gate for switching operation. Only one extra transistor was used in this proposed design. Amico *et al.*[16] address the corruption of input signal by large kickback noise. The increase in the size of transistors reduces the kickback noise but increases the large parasitic capacitances. Zeller *et al.*[17] proposed a dynamic latched comparator with complementary input stage for large input common-mode range and short decision time at small differential input voltages. The work reported presents that there are no static currents and all internal nodes are discharged during the low clock phase to avoid offset that depends on previous decisions. Xu *et al.*[18] proposed an element comparator which works in lower voltage and rapidly low power. Sigma–delta ($\Sigma\Delta$) modulation[19] is always used in image sensors where pixels are more.

The offset of the $\Sigma\Delta$ modulator is zero because of the offset errors in the loop and the first-order difference of all the noises.[20] The low response is due to the quantization interval associated with the lowest input signal range which has the lowest resolution. Due to the nonlinear charge of the junction photodiode, the $\Sigma\Delta$

modulator has a nonlinear response. This effect can be reduced by reducing the voltage swing across the photodiode or increasing the reverse bias voltage. A five-transistor pixel implementation of the pixel-level modulator was designed in Ref. 21. The 128-channel ADC-based image sensor was constructed and a decimation filter was implemented. This work is based on the image sensor design.

2. Clocked Regenerative Comparators

Clocked regenerative comparators are used in high-speed ADCs due to their advantages of high input impedance, rail-to-rail output swing, no static power consumption and good robustness against noise and mismatch. Due to the strong positive feedback the decision making is done so fast. The comparator is normally implemented using CMOS technology. The comparator offset from fabrication mismatch degrades the ADC's resolution in architectures. Interpolation-based methods were followed for sampling and reduction of blocks.[22] The interpolation technique has reduced the number of comparators by half. It utilizes only dynamic comparators and SR latches. Trimming circuits will be effective but vary due to mechanical stress and are converted into offset voltage due to the piezoelectric prosperities of silicon. But the input offset cancellation trimming technique[23] provides an injected current to the analog input. This technique avoids the stability issue, consumes low silicon area and results in low power consumption. Architecture based on on-chip compensation technique can remove the offset voltage by compensating the process variations in parameters such as W/L, μC_{OX} and threshold voltage independently. In normal compensation technique the I_{DS} of the transistor pair at one input voltage point is compensated.

Circuits for offset calibration when involved with clocks create addition errors in skew or jitter. Unbalanced clocks are also used for calibration but the phase is difficult to attain. This increases the complexity and area. Digitally-assisted offset cancellation technique for ADC can reduce errors. Residual amplification, digital counters and complementary clock signals are used to design the compensation circuit. But the design will be bulky having more number of blocks. This circuit was suitable only for system where more digital assistant units are available. So all the above factors are to be considered while designing a comparator for the ADC. The comparator is used in circuits where speed requirement is higher. But the mismatches between the transistors and circuit parameter deviations lead to large input offset current. The large input offset current limits the resolution to about 5 bits. The offset voltage can be overcome by preceding the dynamic latch using linear amplifier. This can increase the feasibility of medium-resolution comparators (8 bits). The offset can be reduced by designing the comparator with differential input stage. This paper discusses the detailed analysis of four existing comparators. The dynamic behavior of the CMOS latch is presented and a technique to reduce the input-referred offset is proposed. In recent years, several dynamic comparators have been widely

employed in ADCs offer high operating speed while consuming no static power. The CDC has drawbacks which can be rectified by the DTDC. The DTDC topology reduces the transistor stacking and operates at lower supply voltages compared to the CDC. The double tail enables both a large current in the latching stage and wider tail transistor, for fast latching independent of the input common-mode voltage, and a small current in the input stage for low offset.

3. Proposed Methodology

The proposed high-speed switched dynamic comparator (HSDC) with constant I_d/g_m biasing is shown in Fig. 1. The double-tail structure reduces the number of stacked transistors. For the analysis, we consider from left end in Fig. 1 consisting of the constant I_d/g_m biasing connected to the tail transistors M9 and M10. This circuit reduces the environmental drift. The input-referred offset voltage V_{OS} is given by the threshold mismatch $\Delta V_{T1a,1b}$ and the current factor mismatch $\Delta\beta_{1a,1b}$ of the

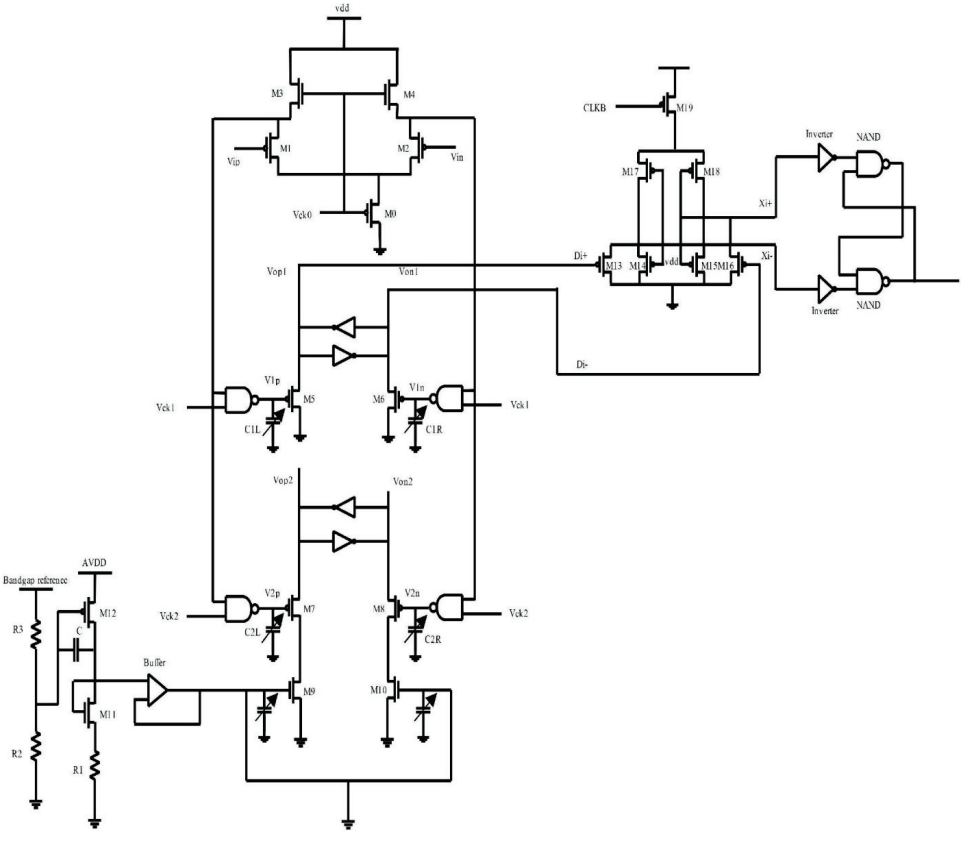

Fig. 1. Proposed high-speed, low-power SDC.

differential pair M_{1a} and M_{1b}, as given below:

$$V_{OS} = \Delta V_{T_{1a,1b}} - \frac{I_{d1}}{g_{m1}} \frac{\Delta\beta_{1a,1b}}{\beta_1}. \quad (1)$$

The counter offset (amount of threshold shift) by the programmable capacitors is given by $V_{COS} = (I_{d1}/g_{m1})(\Delta C/C)$,[18] where ΔC is the difference in capacitances. The residual input-referred offset after calibration is therefore given by

$$V_{ROS} = V_{OS} - V_{COS} = \Delta V_{T_{1a,ab}} - \frac{I_{d1}}{g_{m1}} \left(\frac{\Delta\beta_{1a,1b}}{\beta_1} + \frac{\Delta C}{C} \right). \quad (2)$$

In general, the temperature dependences of ΔV_T and $\Delta\beta/\beta$ are negligible for 7-bit ADCs. The constant I_d/g_m biasing circuit can drive other circuits in the ADC. For this purpose a differential unity gain buffer is included in the circuit which maintains the voltage level. The switched dynamic comparator is designed to drive two latches L_1 and L_2. The digital switching operation is carried out using NAND gate. The first stage is shared between the driving circuits which reduces the input capacitance. The input capacitance lowering reduces the power consumption. Three clock signals are used to operate the SDC. The dynamic amplifier block operates with full rate through CLK_0. The latches L_1 and L_2 are controlled by CLK_1 and CLK_2. The offset calibration is taken care by the two capacitances C_{1L} and C_{1R}.

During the reset phase LAT_1 is made to rest by making $V_{ck0} = 0$ and $V_{ck1} = V_{DD}$, the source nodes V_{sp} and V_{sn} are charged to V_{DD} while the nodes at gate terminal, i.e., V_{1p} and V_{1n}, are discharged to ground, causing the outputs V_{op1} and V_{on1} to be charged to V_{DD}. During the sampling phase, $V_{ck0} = V_{DD}$ causing V_{sp} and V_{sn} to change their states depending on the inputs V_{1p} and V_{1n}. A differential signal $\Delta V_{spn} = V_{sn} - V_{sp}$ is applied between V_{sp} and V_{sn}. Now LAT_1 regenerates the final output when $V_{ck1} = V_{DD}$ at which point V_{sp} and V_{sn} are in discharge state to pass the differential signal $\Delta V_{spn} = V_{sn} - V_{sp}$ to LAT_1. This is achieved by adding a delay t_{dl} to V_{ck1} such that $t_{dl} > t_s + t_1$, where t_s and t_1 are charging and discharging of source and node 1 to V_{DD} and ground, respectively. Worst-case approximation is made so that the clocks V_{ck1} and V_{ck2} toggle only after the delay when V_{sp} and V_{sn} reach ground potential and V_{1p} and V_{1n} reach V_{DD}. This will eliminate the jitter and skew spurs in the system. In the regenerative phase $V_{ck1} = 0$ as well as $V_{1p} = V_{DD}$ and $V_{1n} = V_{DD}$, signal regeneration happens in the cross-coupled inverters. The outputs of the latches are given to a second stage where the transistors M_{13} and M_{16} accelerate the values. The M_{19} transistor provides fast latching independent of the output voltages from latches LAT_1 and LAT_2. The transistors M_{13} and M_{16} pass ΔV_{op2} to cross-coupled inverters formed by the transistors M_{14}, M_{15}, M_{17} and M_{18} and provide a shielding between the latches and next stage.

The obtained output voltages are shown in Table 1. The output voltage swing is about 97% of V_{DD} which is a 6% improvement in voltage swing when compared to

Table 1. Output voltages for different inputs.

		CDC		DTDC		MDCS		HSLP	
Input 1 (V)	Input 2 (V)	OUT+ (V)	OUT− (V)	OUT+ (V)	OUT− (V)	OUT+ (V)	OUT− (V)	OUT+ (V)	OUT− (V)
0	0	0.044	0.044	0.050	0.050	0.050	0.050	0.051	0.050
1	1	0.490	0.490	0.999	0.999	1.000	0.997	0.998	0.996
0.5	0	1.000	0.055	1.000	0.034	0.999	0.043	0.998	0.042
0.25	0	0.812	0.036	0.817	0.050	0.878	0.050	0.877	0.050
0.26	0	0.917	0.032	0.960	0.050	0.963	0.050	0.967	0.050

Table 2. Performance comparison between the proposed comparators for different inputs.

Input 1 (V)	Input 2 (V)	Avg. power (mW)		Avg. current (mA)		Peak power (mW)	
		45 nm	65 nm	45 nm	65 nm	45 nm	65 nm
0	0	3.905800	4.235900	0.479390	0.740130	13.887000	9.061700
0.5	0	3.918500	4.237100	0.445650	0.576420	14.125000	7.970700
0	0.5	3.919000	4.237200	0.550230	0.572170	13.951000	8.034900
0.1	0	3.905800	4.235900	0.501280	0.738380	14.323000	9.017300
0	0.1	3.906600	4.236900	0.466660	0.751310	14.063000	8.944100
1	0	3.924400	4.246400	0.475700	0.610000	13.898000	7.520000
0	1	3.924300	4.244700	0.429680	0.619180	14.002000	7.497600

the conventional method. Additional transistors are consumed for the I_d/g_m biasing block and latching stages but providing better noise immunity and driving capability. Table 2 shows the performance comparison between the proposed circuits in 45-nm and 65-nm CMOS technologies. Here the inputs are varied for different voltage combinations. The inputs are varied from 0 V to 1 V since V_{DD} is 1 V. For the comparison purpose for both 45 nm and 65 nm the V_{DD} is chosen as 1 V. The power consumed in 65 nm for the proposed method is 7.8% more when compared with that in 45 nm.

The proposed comparator will be used in the bank of comparators as shown in Fig. 2. The design employs five transistors per pixel to implement a charge-based ADC at each pixel. In the current design a dynamic regenerative latch comparator is divided into an input transistor, which is contained within each pixel, and the remaining comparator structure shared among the pixels of each column. A charge-feedback digital-to-analog converter (DAC) is implemented at each pixel with a three-transistor structure. As opposed to more traditional CMOS image sensors, this image sensor architecture is suitable for implementations in advanced low-supply-voltage CMOS technologies since its dynamic range is not affected by the reduction of the pixel reset voltage. In addition, similar to the readout methods in low-power random access memory designs, this pixel readout architecture does not employ any active amplifiers which allows for low static power operation.

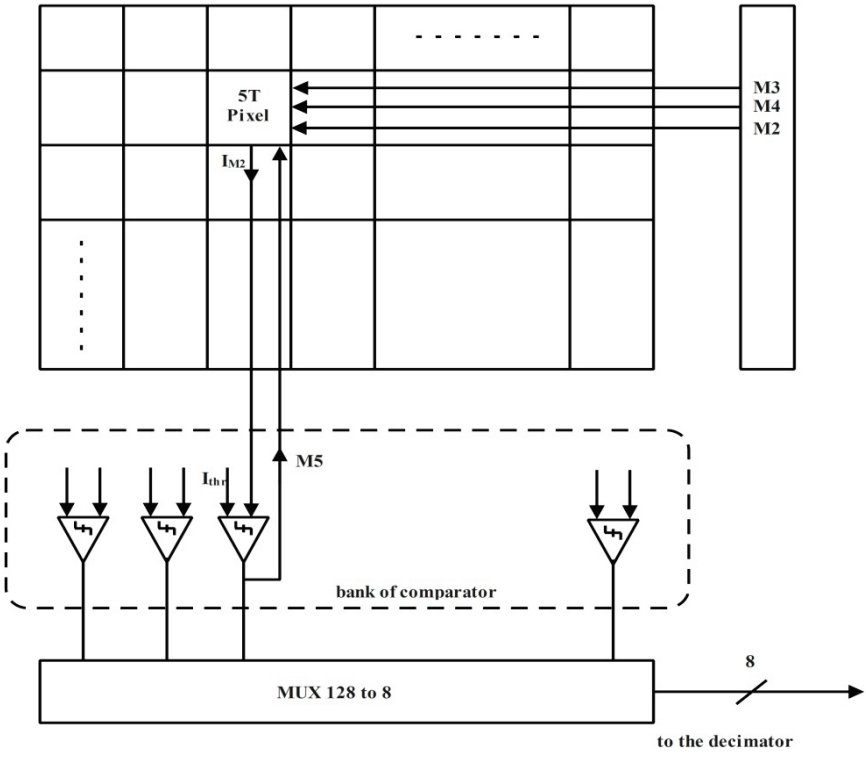

Fig. 2. Array-level diagram of the image sensor with readout.

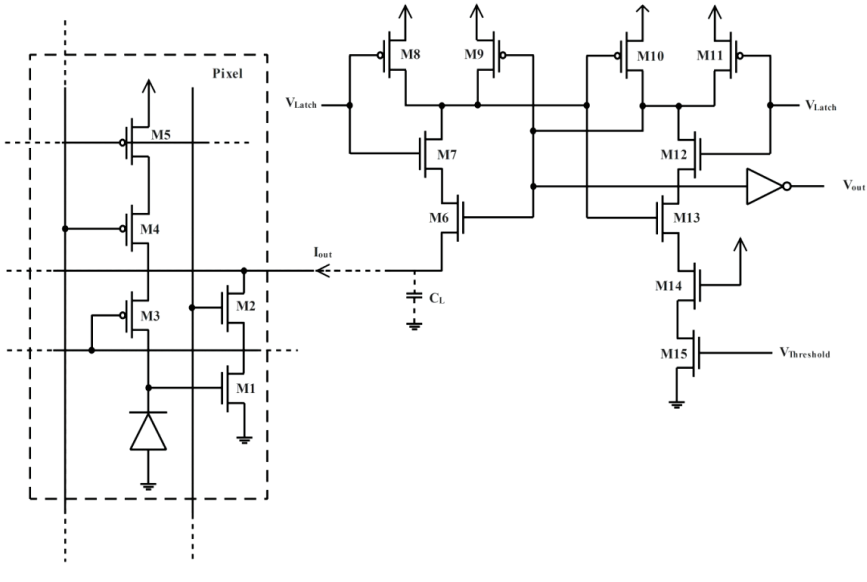

Fig. 3. Column-level comparator of the ΣΔ image sensor readout.

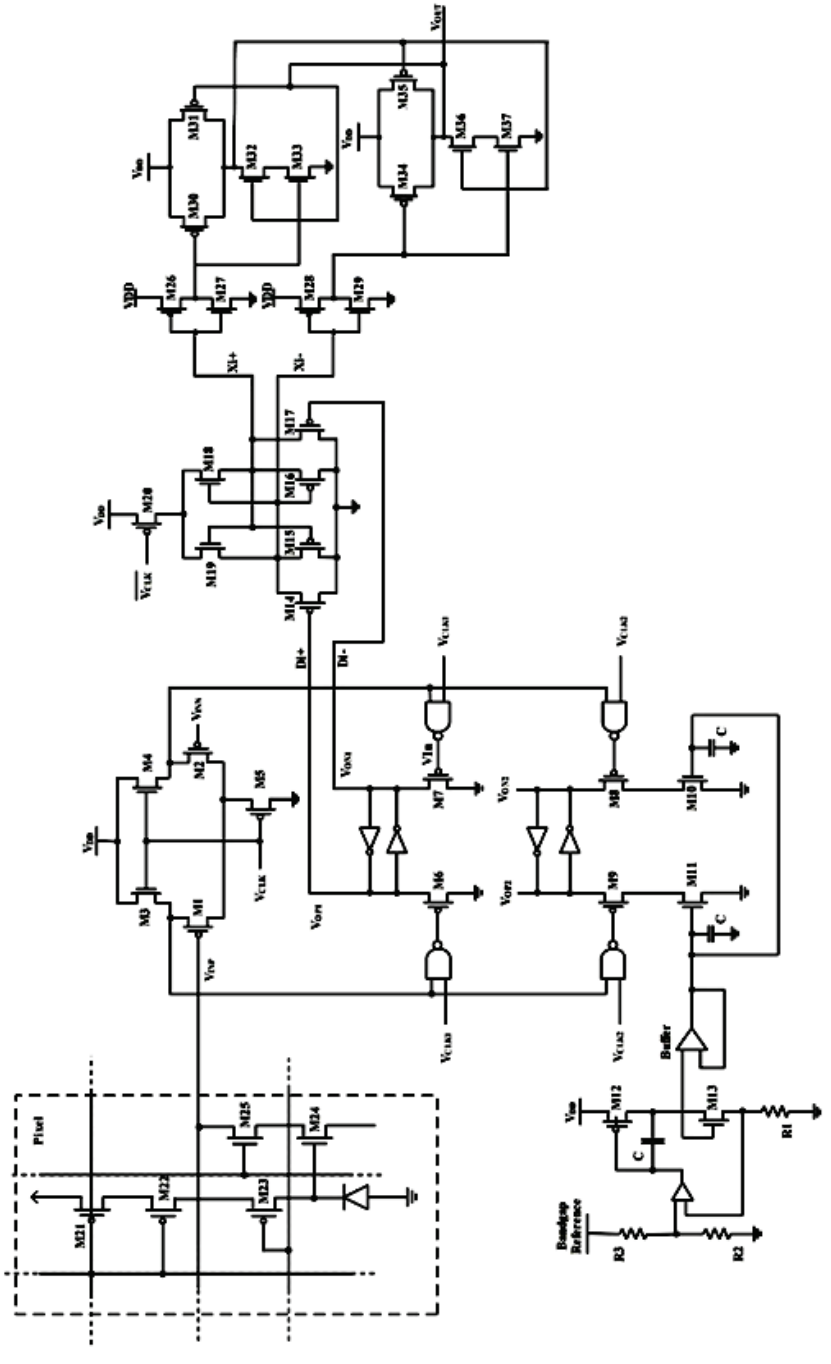

Fig. 4. Proposed column-level comparator of the ΣΔ image sensor readout.

Table 3. Performance analysis of the proposed column-level comparator.

Inputs (V)		Avg. power (mW)	Peak power (mW)	Max current (mA)	Min current (mA)
0	0	6.8005	7.4063	8.8759	4.1832
0	1	6.7902	7.3829	8.7384	4.1989
1	0	6.8005	7.4063	8.8759	4.1882
1	1	6.8005	7.4063	8.7696	4.1832

Table 4. The transistor sizes used in the existing and proposed circuits.

Primary parameters in PTM				
NMOS	$L_{\text{eff}} = 45\,\text{nm}$	$T_{\text{oxe}} = 1.75\,\text{nm}$	$V_{th0} = 0.466\,\text{V}$	$V_{DD} = 1\,\text{V}$
PMOS	$L_{\text{eff}} = 45\,\text{nm}$	$T_{\text{oxe}} = 1.85\,\text{nm}$	$V_{th0} = 0.4118\,\text{V}$	$V_{DD} = 1\,\text{V}$
NMOS	$L_{\text{eff}} = 65\,\text{nm}$	$T_{\text{oxe}} = 1.7\,\text{nm}$	$V_{th0} = 0.22\,\text{V}$	$V_{DD} = 1\,\text{V}$
PMOS	$L_{\text{eff}} = 65\,\text{nm}$	$T_{\text{oxe}} = 1.7\,\text{nm}$	$V_{th0} = 0.22\,\text{V}$	$V_{DD} = 1\,\text{V}$

Table 5. Performance analysis of the different types of comparators as column-level ones.

Method/Parameter	CDC	DTDC	MDCS	HSLP	HSDC
Average power (μW)	29.26	909	869	1,450	650
Peak power (μW)	191.82	181	1,942	3,105	2,748

Circuit implemented in an application is given in Fig. 3 with the existing method.

The proposed column-level comparator is given in Fig. 4. The proposed circuit provides higher voltage swing and noise immunity. The performance of the proposed column-level comparator circuit is given in Tables 3 and 4.

Table 5 provides the power analysis on average and peak powers observed during the comparator operation. The clock frequency is kept as 3 GHz and the supply voltage is 1 V. For the average power, the proposed HSDC consumes lesser power when compared to other circuits. It saves about 28% power compared to DTDC and 55% power when compared to HSLP comparator. The output voltage swing is about 97% of V_{DD} which is a 6% improvement in voltage swing when compared to the conventional method. Additional transistors are consumed for the I_d/g_m biasing block and latching stages but providing better noise immunity and driving capability.

4. Conclusion

The paper presents the design of low-noise, high-speed SDC for CMOS image readouts. The column-level dynamic comparator proposed in this work not only eliminates the offset voltage but also reduces the area occupied. The features are suitable for the image processing applications. The proposed methodology eliminates the staking issues and provides an improved maximum output voltage swing of 96%.

When compared with the conventional comparators the proposed method saves power. The delay issues are rectified by the regenerative feedback so the image capturing speed can be improved. The maximum clock frequency of the proposed comparator is increased to 3.5 GHz at supply voltage of 1 V. The circuits in 45 nm and 65 nm are tested with various supply voltages in the range of 0.6–1 V and frequencies of operation from 1 GHz to 4 GHz. The simulation is carried out using predictive technology models for 45 nm and 65 nm in HSPICE.

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