Low power very large scale integration (VLSI) design of finite impulse response (FIR) filter for biomedical imaging application

Diseño de integración a muy gran escala (VLSI) de baja potencia de filtro con respuesta de impulso finita (FIR) para aplicación de imágenes biomédicas

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RESUMEN

- Hoy en día, las técnicas de procesamiento de imágenes médicas utilizan diseños VLSI (Very Large Scale Integrated) para mejorar su disponibilidad y aplicabilidad. Los filtros digitales son un módulo importante de los sistemas basados en el procesamiento digital de señales (DSP). El enfoque de diseño de la Respuesta al Impulso Finito (FIR) existente se lleva a cabo con el Sumador Parcial Completo (PFA) basado en el Sumador de Carga (CLA) y la lógica del sumador de prefijo paralelo en el multiplicador védico. El objetivo de este enfoque es mejorar el rendimiento del circuito VLSI obteniendo el resultado de área, potencia y retardo, además, la incorporación efectiva entre el circuito VLSI y el enfoque de procesamiento de imágenes hace que se mejore la disponibilidad de la aplicación. El diseño del filtro digital FIR de alta velocidad se realiza con varios sumadores y multiplicadores. La incorporación del diseño VLSI y las técnicas de procesamiento de imágenes se utilizan en aplicaciones de imágenes biomédicas. El diseño del filtro FIR mejorado utiliza el sumador híbrido y el multiplicador védico adaptativo para aumentar el rendimiento de la parte VLSI y los resultados del procesamiento de imágenes se toman de la herramienta Matrix Laboratory. Este diseño de filtro FIR propuesto ayuda a realizar las técnicas de imagen biomédica. El resultado de la simulación obtiene el rendimiento del FIR mejorado con el área, el retardo y la potencia; para las imágenes biomédicas, se obtiene el error cuadrático medio (MSE) y la relación señal/ruido máxima (PSNR). En comparación con el método existente y el propuesto, el filtro FIR propuesto para la aplicación de imágenes biomédicas obtiene el mejor resultado. Por lo tanto, el modelo de diseño se establece con varios enfoques de disponibilidad de aplicación de procesamiento de imágenes VLSI y obtiene los mejores resultados de rendimiento de ambas aplicaciones VLSI y de procesamiento de imágenes. En general, el sistema propuesto está diseñado por Xilinx ISE 14.5 y el resultado sintetizado se realiza con ModelSim. El rendimiento de la imagen biomédica se realiza mediante MATLAB con la adaptación de 2018a.
- **Palabras clave:** Filtro FIR mejorado; multiplicador védico adaptativo; sumador híbrido; imagen biomédica; producto de retardo de potencia.

ABSTRACT

Nowadays, the medical image processing techniques are using Very Large Scale Integrated (VLSI) designs for improving the availability and applicability. The digital filters are important module of Digital Signal Processing (DSP) based systems. Existing Finite Impulse Response (FIR) design approach performed with Partial Full Adder (PFA) based Carry Lookahead Adder (CLA) and parallel prefix adder logic in Vedic multiplier. Objective of this approach is to improve the performance of VLSI circuit by obtaining the result of area, power and delay, also, effective incorporation between VLSI circuit and image processing approach makes improved application availability. The design of high speed digital FIR filter is designed with various adders and multipliers. The incorporation of VLSI design and image processing techniques are used on biomedical imaging applications. The Enhanced FIR filter design utilized the hybrid adder and adaptive Vedic multiplier approaches for increasing the performance of VLSI part and the image processing results are taken from Matrix Laboratory tool. This proposed FIR filter design helps to perform the biomedical imaging techniques. The simulation result obtains the performance of enhanced FIR with area, delay and power; for biomedical imaging, Mean Square Error (MSE) and Peak Signal to Noise Ratio (PSNR) is obtained. Comparing with existing and proposed method, the proposed FIR filter for biomedical imaging application obtains the better result. Thus the design model states with various application availability of VLSI image processing approaches and it obtains the better performance results of both VLSI and image processing applications. Overall, the proposed system is designed by Xilinx ISE 14.5 and the synthesized result is done with ModelSim. Here the biomedical image performance is done by using MATLAB with the adaptation of 2018a.

Keywords: Enhanced FIR filter; Adaptive vedic multiplier; Hybrid adder; Biomedical imaging; power delay product.

1. INTRODUCTION

Digital filters are plays a major role in DSP applications, which mainly depends on IIR and FIR filter. The biomedical image processing techniques are performed on various filtering approach by enhancing the improved adders and multiplier logics. The filter circuit adapts both medical images and signals for increasing the

performance of application. The ultrasound images are performed on the filter applications by incorporating the VLSI design. In VLSI filter structure, the adders are multiplier logics are the major blocks for effective performance. Here the multipliers are key parts of VLSI frameworks, which utilized the FIR and IIR filter, advanced signal processors, and so on. This presentation is commonly dictated by the exhibition of multiplier slowest lenient in the framework for reducing the adder logics. Enhancing the speed and territory of the vlsi multiplier have significant structure issue. Digital Signal Processing applications majorly focused FIR structure because of their dependability and direct stage opportunity. Recently, the low power utilization and less territory are the most significant boundary for the manufacture of DSP frameworks and superior frameworks.

The usage of a FIR filter has three fundamental structures that are Multiplication, Addition and Signal deferral delay unit. Multipliers are the most measured unit of area in a FIR filter. Here the pipeline structure for FIR filter executed with Distributed Arithmetic [1]. Design structures of filters comprise adders, multiplier and delay transformation unit. The filter configurations are utilized the power efficient design by clock gating technique, which utilized the carry Save Accumulation (CSA) [2]. The clock cycle utilized for the remaining tasks to decrease the power utilization on VLSI circuit. The digital filter activates the part to comprise the multiplier and adder for convolution activity. The design and implementation of VLSI structure - FIR filter utilized various adders and multiplier logics [3]. The performance of FIR filter also depends on delay unit, which activates the clock period. The pipeline registers activity utilized the clock gating strategy and it performed for low power procedure in the FIR and it also has the relationship of image information is high facts. The carry select adder and booth multiplier are utilized on the FIR direct form filter structure [4]. The images and signals of medical field applications are performed by utilizing various filters. The FIR filter structure plays an important role in medical image and signal processing. The ultrasound image enhancement techniques are utilizing structured based filtering approach, which is presented in [5].

Various digital filters are performed with the FPGA (Field Programmable Gate Array) based design, which utilized to perform the biomedical signals like Electroencephalogram and Electrocardiography signals [6]. The anisotropic diffusion filter is effectively performed on the medical MRI images with denoising approach. Here the presented existing approach utilized the learning based optimization approach [7].

FIR channel can be planned to utilizing windowing technique and sampling techniques. However, in windowing technique, the endless driving of filter utilizing a sampling frequency to get better results of digital filters in the way of area utilization, delay optimality and the power factors. The ultrasound image and video processing performed on the de-speckle approach for improving the quality of given data [8]. In the FIR based high pass performance filter selects the coefficient by varying the filtering approach, which is obtained based on the binary value of given biomedical image/signal [9]. Linearly separable filter data is processed with high pass filter and it provides the result of biomedical signals, which utilized the EEG (Electroencephalogram), ECG (Electrocardiography) and pulse reading data. The Window strategy is applied on the filter structure of direct form approach. FIR digital filters are utilizing with various multiplier and Carry Select Adder. Phonocardiography image is adopted on the FIR filter for medical diagnosis [10]. The wavelet based image analysis in medical field applications [11].

The area efficient parallel prefix adder adopts the ladner fischer adder logic, which is done with CBL Architecture with CSK adder [12]. Booth multiplier used widely in the FIR and Arithmetic Logic Unit (ALU) structures [13]; because it is an area efficient circuitry; to improve the design we also use the two or three combined adder logics in a single circuit. Unbiased frequency based image processing techniques are applied on the FIR filter [16]. Various adders and multipliers in VLSI circuits are applied to improve the performance and it also performed with parallel prefix adder logics [19] & [20]. The FIR architecture is contrasted and the ordinary FIR channel utilizing SQRT-CSA (Square Root Carry Select adder) based logics. FIR and Infinite Impulse Response (IIR) channels are the two normal types of channel structure in digital filter of VLSI domain [23]. The SPECT and ultrasound image processing techniques are processed with the VLSI filter circuit [24] & [25]. The main drawback of the IIR is shut structure and its configuration, which are started restrict with low pass and high pass channels. Therefore, proposed work utilized the FIR filter structure with direct form concern by improving the performance utilizing area, delay and power utility, which adopts with improved adders and multiplier blocks. The purpose of this study is to increase the availability of VLSI image processing in the field of medical, satellite image processing, etc., The VLSI circuit utilization determines the various combination of adders and multiplier logics, also the clock triggering state shows the better utility of results. So, the study determines the hybrid adder with adaptive vedic multiplier performed well with FIR Filter circuit for utilizing image processing applications. The aim of this proposed design is to improve the performance of VLSI circuit by enhancing the application of biomedical imaging.

1.1 RELATED WORK

Christeena M, and Dhanya P, (2016) has presented the VLSI design of CBL architecture using fastest adder, which comprises carry skip adder with ladner fischer adder. The hybrid structure of adder utilized the RCA based CSKA and parallel prefix adder. This approach aims to reduce the delay of VLSI circuit performance. Here the floating point adder unit helps to improve the circuitry of the adder, which optimizes CSKA. The area-delay product and structure performance is determined additionally to obtain better performance results.

Sampath Kumar D, and GRKS Subramanyam, (2016) has presented the VLSI design and implementation of parallel logic based FIR filtering algorithm, which uses the way of multiplication with symmetric co-productive characters and it performs the two parallel FIR filter constructions using FFA technique. Here this FFA system uses convey spare snake for tuning approach, which adopts the symmetric coefficients. The sub filter functions are performed with MATLAB tool to generate the canonical sign digits using remez exchanging approach.

L J Morales-Mendoza, et. al. (2016) has proposed the design of hybrid FIR filter for image processing applications, which utilized the ultrasound image filtration. Here the moving average filtering approach performed with median hybrid filtering technique. In this structure, the linear regression function is performed with continuous data utility, which is adopted mainly on the Lagrange multiplier. This approach designed to perform denoising of ultrasound images for medical field applications.

Swati B and Usharani S, (2017) have described the FIR filter design and applications in medical field. Here the reconfigurable FIR filter is designed to perform EEG signal analysis. The filtered EEG signal helps to the medical fields, which incorporate the VLSI

structure of FIR filter and signal analysis in EEG signal. This Reconfigurable FIR utilized the transpose form of pipelining model, which is done with multiple constant multiplication approach. Here the coefficient register unit takes much area on VLSI structure and it is also applicable for 2D design with block least mean square.

Jun M Jung, et. al. (2001) have presented the digital filter design for image filtering applications. This approach aims to design the low power VLSI structure using clock gating technique. The tap registers are fixed based on the size of FIR structure, which improves the switching activity of filter.

Ch Pratyusha C, and J B Seventline, (2019) has proposed the FIR filter structure utilized with the distributed arithmetic (DA) approach, which is applicable for DSP applications. This approach performs the denoising strategy of ECG signals, which adopts the 11 tap filter structure. In DA, the LUT is mapped with the lower accessibility of registers. This approach helps to utilize the medical healthcare applications for noise removal approach. Sumit K, et. al (2017) has designed the optimized denoising approach for ultrasound image noise removal, which utilized the anisotropic diffusion filter. Here the teaching learning approach performed with optimization algorithm for improving the applicability of the filter in various real-time applications. G Viranya and G Sridevi, (2017) has presented the FIR filter structure utilized with koggestone based CSLA logic. Here the regular CSA is performed with linear BK CSA logic. The impulse response of FIR filter is modified by changing the adder and multiplier blocks. Various comparisons were analyzed and obtains the better compared result of VLSI performances. The comparative analysis utilized the koggestone, Brent Kung and Carry select adders; this utilized the shift and adds method for improvement. The linear phase stability improvement analyzed the filtering properties.

Anqing Yang, (2010) have reviewed the study of medical image filtering techniques using morphology approach and self-adaption scheme. Adaptive filtering technique utilized the speckle noise reduction approach and the median filter utilized on the Rayleigh noise removal. The study also describes the adaptive median filtering with mathematical approach on morphology process. Comparative analysis of various image denoising technique of ultrasonic medical image are described. With this study, the adaptive morphological based median filter obtains the results on the ultrasound image.

Imteyaz A, et. al. (2006) has designed the FIR filter structure for image restoration approach. Here it aims to designed the biomedical imaging approach, which also adopts the learning procedure. This learning approach uses Hebbian learning procedure for enhancing the performance. Here the impulse noise, speckle noise, salt and pepper noise are analyzed to perform effective performance in FIR design.

Qasem Abu Al-Haija, et. al. (2019) has performed the FPGA synthesis model of parallel prefix-adder logic by validating the various VLSI parameters. Various parallel prefix adders like brent-kung, kogge stone, hans-carlo, sklansky and ladner-fischer adders are studied for improving the VLSI design. Here the PPA topology is implemented on FPGA device such as SPARTAN 3E and Cyclone4E. The synthesis of hardware utility analyzed the area, delay and power factors.

1.2. EXISTING APPROACHES

Various literature surveys are analyzed and compared to perform better logics in proposed system for utilizing the medical field application like image filtering. This mainly optimizes ultrasound images for removing unwanted noises presented in the image. This section describes the two previous work and its drawbacks. First work FIR filter designed with modified CSA with binary multiplier logics and the second work utilized the improved design of CLA along with vedic multiplier.

1.2.1. M-CSA and binary multiplier in FIR filter

A design of FIR filters utilizing the modified CSA logic with binary multiplier. This approach obtains the result of performance metrics like area, delay and power factors. Here the CSA is improved by adding RCA logics; this selects the carry bit at the end. Every time, the 2-bit carry value is rippled on the CSA for last bit addition. Here it studied the parallel prefix adder logic for increasing the performance of VLSI circuits. Depends in the input value of the filtering approach, the coefficient is selected and it obtains the result based on the RCA based CSA and binary multiplier logics. The analyzed result provides the area, delay and power for VLSI performance.

1.2.2. I-CLA and Vedic multiplier in FIR filter

Previous work designs the low power FIR structure utilizing the carry look-ahead adder and the vedic multiplier enhanced with

Author & Year	Title	Technique	Advantage	Disadvantage
L J Morales-Mendoza, et. al. (2016)	Moving average hybrid FIR filter in Ultrasound Image Processing	hybrid FIR filter for image processing applications	Improved overall performance of filtering	Couldn't identify the averaging and median filter results in it.
Swati B and Usharani S, (2017)	Reconfigurable FIR filter architecture for EEG application	Reconfigurable FIR filter is designed to perform EEG signal analysis.	Reduced delay and area	Increased power
G Viranya and G Sridevi, (2017)	Design of low power and high speed FIR filter using Koggestone CSLA	FIR filter structure utilized with koggestone based CSLA logic	Teaching learning approach performed with optimization algorithm for improving the applicability of the filter in various real-time applications	Optimization may increases power
Ch Pratyusha C, and J B Seventline, (2019)	An Efficient FIR filter Architecture Implementation using Distributed Arithmetic (DA) for DSP applications	FIR filter structure utilized with the distributed arithmetic (DA) approach, which is applicable for DSP applications.	With the help of DA the VLSI structure is improved	LUT is mapped with the lower accessibility of registers
Qasem Abu Al-Haija, et. al. (2019)	FPGA Synthesis and validation of parallel prefix adders	FPGA synthesis model of parallel prefix-adder logic by validating the various VLSI parameters.	Increased application	Design complexity

Table 1: Comparison of survey papers

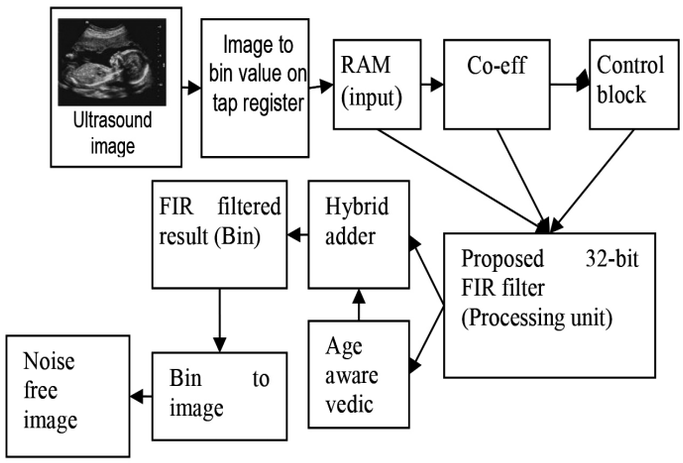

Fig. 1. Block diagram of proposed FIR filter design utilizing biomedical applications

adding Brent-kung adder logics. The power optimal technique in FIR circuit utilized the clock gating approach. This switching activity helps to improve the speed of filtering process by reducing the power consumptions. The carry look-ahead adder logic is enhanced with PFA and it also utilized the clock gating technique. Here the FIR filter structure adopts CLA and Vedic multiplier logics. Depends on the random selection of coefficients, the carry bit is modified and inverted with the selection unit. By varying the selection bit, the switching activity of gating logic obtains the result of reduced power consumptions. The clock gating technique utilized this approach for low power VLSI design. With the analysis of various adder and multipliers, the FIR filter is designed to adopt the hybrid adder and enhanced Vedic multiplier logics.

2. MATERIAL & METHODS

The design and utility of real medical imaging application is designed with 16x16 bit FIR filter structure. The direct form FIR filter structure is designed with 16bit data based on the input ultrasound image. Here the hybrid adder logic uses CLA and CIA for better performance results. The AHL based Vedic multiplier is designed to enhanced the performance by reducing the error on the VLSI structure (see figure1) by knowing the age factor and error

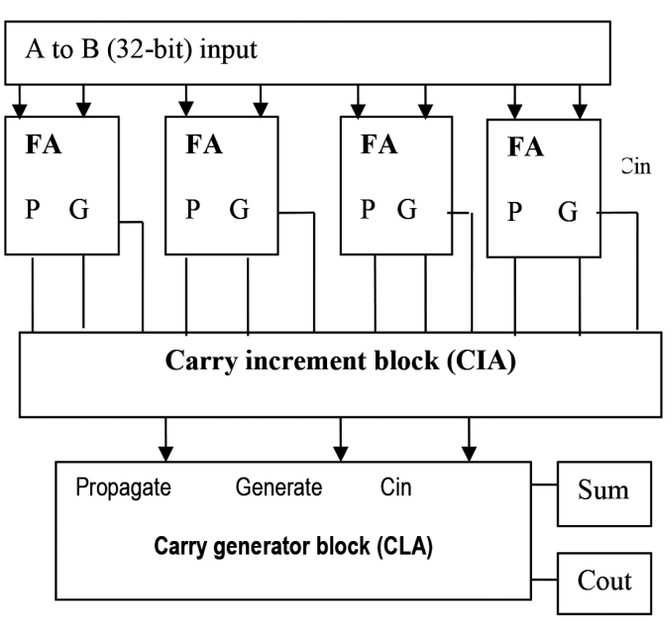

Fig. 2. Proposed Hybrid adder logic

circuitry detection approach. The objective of this approach is to improve the performance of VLSI structure and imaging analysis such as area, delay and power consumption rate for VLSI structure; the RMSE and PSNR for ultrasound imaging analysis.

The proposed design of FIR filter utilized to perform up to 32-bit of processing data. Here the input ultrasound image is applied on the MATLAB 'imread' function and it is providing the bin value, which is loaded on tap register of the VLSI circuitry. This bin value of respective image is loaded on the .mat function of image processing unit. The input block of FIR filter utilized the tap register, control unit and co-efficient loading block. The controlling strategy utilized the clock, reset, enable and scan_enable for performing the initial state of proposed FIR filter. The second step utilized the processing unit of FIR filter, which perform the delay function of transformation 'Z'. The vedic multiplier block is enhanced with the age aware multiplier unit, which is performed with AHL and razor flip flop block. The hybrid adder utilized the carry look-ahead and carry increment adder; this performance obtains the better result by reducing the area utility. The filtered value is converted into image without noise.

2.1. PROPOSED FIR FILTER STRUCTURE

The proposed FIR filter is constructed with 32-bit processing, which is enhanced with hybrid adder and age aware multiplier blocks. This approach aims to improve the performance on image processing techniques, which is applicable on the medical field. Here the ultrasound image is utilized to perform enhanced filtering technique. In FIR filter structure, the input assignments utilizing 32-bit design and it is expressed with impulse response, which is given as,

$$x_{32}(k) = [\mathrm{x_0(k)}, \mathrm{x_1(k)}, \ldots \ldots \mathrm{x_{31}(k)}] \quad (1)$$

$$\mathrm{h1(n)} = [\mathrm{h1(0)}, \mathrm{h1(1)}, \mathrm{h1(2)}, \ldots\ldots\mathrm{h1(31)}]^{Pn} \quad (2)$$

The coefficient selection in FIR with the discrete linear function is expressed as,

$$f(x) = a1(n) + b1(n)\,(t-c)_n \quad (3)$$

Where, the t and c represents the coefficient of FIR with discrete time factor. Each coefficient on tap register is expressed with average covariance points.

$$a(n) = \frac{1}{P_n}\sum_{j=0}^{P_n-1} y(n-j) \quad (4)$$

$$b(n) = \frac{conv\,(y,t)_n}{var(t)_n} \quad (5)$$

$$c(n) = \frac{1}{P_n}\sum_{j=0}^{P_n-1} t(n-j) \quad (6)$$

After performing the transformation, the desired function is given as,

$$f(x_n) = \sum_{j=0}^{Pn-1} \frac{2(2P_n-1)-w(j)}{P_n+1}\, y(n-j) \quad (7)$$

The delay response, clock switching activity and the transformation is performed on the initial state of filtering. Here the adder and multiplier logic plays a vital role, which uses hybrid adder logic and aging aware Vedic multiplier logic. Initially, the register unit takes the input from the matlab and it performs the FIR filter

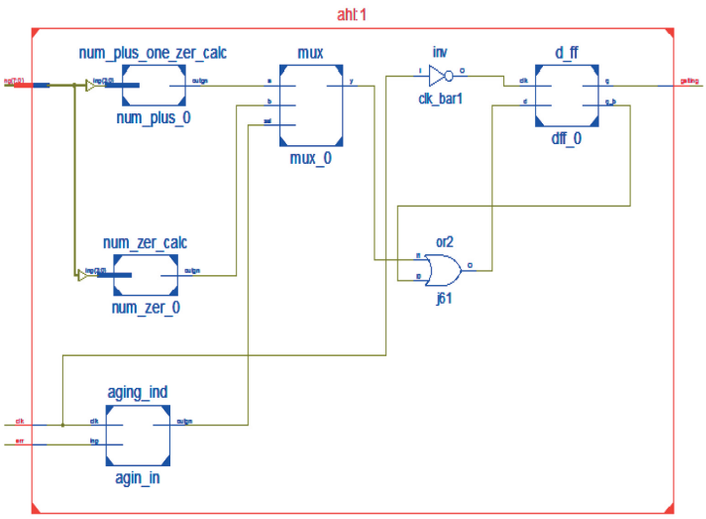

Fig. 3. Aging indication using Adaptive Hold Logic circuit

functioning then it obtains the result in binary form, which is given to the matlab for converting respective image of that binary value. Here the image is read from matlab based on the pixel value, the image is converter into the matrix form of bin value, which given to the registry of the FIR. At the initial state of FIR performance, the clock triggers the value and obtains the switching state. After getting results of FIR, the Matlab stores the matrix and convert the bin value into image that is noise free image.

2.1.1. Hybrid adder logic

The utility of hybrid adders are important block of VLSI circuits, which adopts CLA and CIA (Carry Increment Adder). By analyzing various adder logics, the carry look-ahead adder performs speed-up activation and performances. This CLA is adopted with carry incremental strategy on the hybrid block of adder circuit in FIR filter.

The proposed hybrid adder uses CLA and CIA logics; in this, the full adder circuit is used on the initial state of transformation block on FIR filter. The CLA is given as,

$$Pn = a_n \; xor \; b_n \tag{8}$$

$$Gn = a_n - b_n \tag{9}$$

The carry, propagate and generate are determined with carry lookahead adder logics. Every time it increases the carry bit and performs the CIA operation. This hybrid adder obtains the better result than other existing adders.

2.1.2. Aging aware vedic multiplier block

The AHL based Vedic multiplier is performed for increasing the performance of proposed VLSI design of FIR filter structure. The vedic multiplier performs the operation based on urdhvatriyagbyam algorithm. From this, the Vedic multiplication block utilized the Adaptive Hold Logic and razor flip flops for improving the applicability. The aim is to design the proposed Vedic multiplier is enhancing the performance by reducing the delay and power utility of VLSI circuit. Power reduction in proposed vedic multiplier is given by,

$$Pt = n(tap) * (P(latch) + P(xor) + P(and_g)) \tag{10}$$

$$Pc = 2 * (P(latch) + P(and\_g) + P(xor) + (Pn - 1) * (2P(Dy) + 2P(st)) \tag{11}$$

Every block utilized the 4-bit of data on the performance and it performs the effective analysis to obtain the better results. Here the D-FF is used for initial storing purpose of vedic data. The AHL (Adaptive Hold Logic) circuit helps to perform the aging detection technique and it re-execute the circuit for further result improvements. The RTL schematic diagram of AHL circuit design is given in the figure 3.

2.2 BIOMEDICAL IMAGING TECHNIQUE

The biomedical imaging application is utilized on the VLSI designs to improve the performance and applicability.

2.2.1. Availability of data

The ultrasound image database is collected from signal processing laboratory web page. http://splab.cz/en/download/databaze/ultrasound. With different volunteers database of common carotid artery; this utilized array of various transducers with different frequency range. Here the ultrasound image is used for filtering process, which obtains the better results as compared to the other existing approaches. Impulse response function of image pixel is determined as,

$$S_i = R1 * (1 - R2) \tag{12}$$

$$S_s = R1 * R2 \tag{13}$$

The pixel value determination on linearity approach is given as,

$$R1 > \beta, S_i > S_s, \rho \leq 0 \tag{14}$$

$$R1 > \beta, S_i > S_s, \rho > 0 \tag{15}$$

Based on the pixel value determination on MAT functions the binary value is loaded on the tap register of VLSI block and it selected the switching activity for power reduction on proposed FIR filter.

2.3. PERFORMANCE ANALYSIS

The VLSI performance metrics consists of delay, area and power consumption. In this, the area utility is depends on LUT, FF (Flip Flop), BOI (Bonded Input Output) and pin port utility. The delay analysis comprises path delay, gate delay and overall performance of VLSI circuitry by speed. The power factor depends on static and dynamic power. Here the image processing performance is analyzed with MSE and PSNR. The quality of image is improved by reducing the error, which is obtained by MSE.

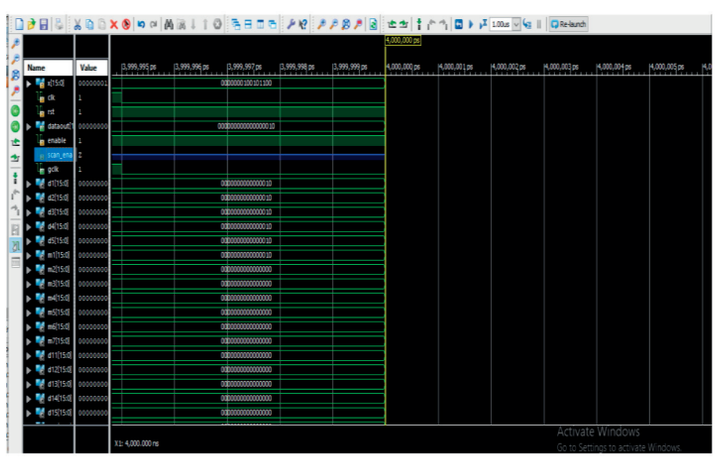

Fig. 4. Simulated result of FIR filter design

Fig. 5. Input ultrasound image

$$Mean\ square\ error = \frac{\sum\sum[In(a,b)-Io(a,b)]^2}{\sum\sum In(a,b)^2} \quad (16)$$

Fig. 6. Converted gray scale image

The signal to noise ratio evaluates the image processing performance. Based on original signal input and restored image signal output is compared and obtains the result.

$$SNR = 10\ log_{10}\left(\frac{\sum\sum[In(a,b)]^2}{MSE}\right) \quad (17)$$

Therefore, the performance of proposed FIR filter for ultrasound image processing is designed and obtains the better results than previous works. Based on the performance metric results, the overall design of 32-bit proposed FIR filter on image filtration technique obtains the best result. The performance of overall design is done by utilizing the hybrid combination of adder logic and adaptive vedic multiplier. Here the hybrid logic uses the CSLA and CIA. By comparing with the carry save adder, the proposed hybrid adder reduces the power consumption, because it has high clocking frequency and cascaded logic in sum and carry alignments.

Parameters	Existing E-CSA based FIR filter	Existing I-CLA based FIR filter	Proposed hybrid FIR filter
Area (slices)	30	14	11
Clock Delay (ns)	9.843	8.436	3.916
Path Delay (ns)	9.703	9.313	4.132
Power(mW)	14	13.69	13.49

Table 2: VLSI performance comparisons

Fig. 7. Noisy ultrasound image

Fig. 8. Noise free image

3. RESULTS

Thus the designs of FIR filter with image processing techniques are performed well with novel approaches and techniques. The simulated result of VLSI design of FIR construction is shown in fig 4. This varies the bin value of FIR filter, which is based on clock activity.

Here the 32-bit adjustable design of FIR filter is designed and implemented for ultrasound image processing techniques. The applied ultrasound input image is given in the figure5. This input image is converted into grayscale for performing filtering operation, which is given in the figure 6.

The converted grayscale image is fitted with resized process of morphological approach. This approach helps to fit the model and it adopted with the filtering process. This resized image is applied with the salt and pepper noise for filtering process. This helps to enhance the white pixels value and extract the filtered results. The noisy image of ultrasound input image is given in the figure 7.

Here the ultrasound noisy image is extracted with the bin value on mat function file as text. Finally, the filtered ultrasound image is obtained with better resolutions, which is given by figure

Parameter	Existing method	Proposed method
MSE	34.78	17
PSNR	27.43	36.49

Table 3: Comparison result of image processing

8. This enhanced image processing model utilized with VLSI circuitry, which analyzed the results of MSE and PSNR. The table 2 shows the proposed FIR filter design performance, which utilized the area, delay and power consumptions. This comparison results obtains the better results for proposed method than other two previous works. In image processing method, the MSE and PSNR is determined to improve the results, which is given in the table 3. This obtains the better results of proposed filtering technique than other existing research works.

Therefore, the experimental design shows the better performance result with reduced area, delay and power. The MSE and PSNR improve the resolutions of imaging approach. The comparison results show the better performance results than existing approaches.

4. DISCUSSION

The technology improvement and applicability of biomedical imaging techniques are utilized on the VLSI designs, which utilized the FIR filter structure. Here the 32-bit FIR filter is constructed to perform effective filtering approach on ultrasound image. In this proposed design, the VLSI circuit utilized the enhanced direct form FIR Filter for biomedical imaging applications. Here the ultrasound image is applied for enhancing the visual and diagnosis process. The enhanced Vedic multiplier is designed to predict the error of VLSI circuit and the hybrid adder utilized the carry lookahead and carry increment adder logics. The Adaptive vedic multiplier, and hybrid adder logic improves the performance of FIR structure and it triggers the value from clocking state of initial value alignment process. With the combination of VLSI and image processing uses the Xilinx ISE and MATLAB tool. The FIR filter structure developed to increase the application availability of medical image processing application in VLSI structures. The proposed design of FIR filter design is designed for adopting the performance of filtering in ultrasound image analysis. Thus it achieves the better result on VLSI circuit and ultrasound images.

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