IETE Journal of Research

ISSN: (Print) (Online) Journal homepage: www.tandfonline.com/journals/tijr20

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To cite this article: V. Thamizharasan & N. Kasthuri (2023) Design of Proficient Two Operand Adder Using Hybrid Carry Select Adder with FPGA Implementation, IETE Journal of Research, 69:12, 9152-9165, DOI: 10.1080/03772063.2022.2071771

To link to this article: https://doi.org/10.1080/03772063.2022.2071771

Published online: 15 May 2022.

IETE JOURNAL OF RESEARCH
2023, VOL. 69, NO. 12, 9152–9165
https://doi.org/10.1080/03772063.2022.2071771

Design of Proficient Two Operand Adder Using Hybrid Carry Select Adder with FPGA Implementation

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ABSTRACT

In every modern ICs the adders are essential components. Adder's performance has a substantial impact on the architecture of signal processing, controller, the module of filter, the module of data storage, *etc*., high-speed and area-efficient circuits are the most substantial parameters in every modern integrated circuit. Carry select adder operates at high speed, but it consumes more power due to the large area. The present approach discloses different VLSI hybrid carry select adder architectures. The hybrid technology-based Carry Select adder (CSELA) consists of two stages, namely the Hancarlson adder stage and Hybrid Stage is proposed. In this technique, all the stages (4 bits in each stage) are performed simultaneously to improve the speed and area further. The propagation delays of the proposed adder are the summation of two full adders, seven Multiplexers (4:1) and BEC(3 bit) for producing Cout. The proposed work indicates that the hybrid carry select adder operates at high a speed with a lesser area than the conventional adder. The proposed design is simulated and synthesized in Xilinx ISE 12.1 using Verilog HDL with a family of Vertex6 FPGA devices (Device No. XC6VLX75T, Package FF484, Speed -3). The synthesized report shows that the speed of the proposed adder is improved by 49.06%, 52.61%, 47.58%, 19.08%, 39.9%, 1.25%, 44.43%,19.08%, 44.07% and 71.59% compared to RCA, CBL-based CSELA, CLA, Weinberger BEC-based CSELA,D latched CSELA, Brent Kung CSELA, Brent Kung RCA-based CSELA, CSA Weinberger, Conventional CSELA and Ling CSELA, respectively.

KEYWORDS

Multiplexers; Carry select adder; Hybrid adder; Xilinx ISE 12.1; Verilog HDL

1. INTRODUCTION

Adders play a significant role in image, signal and video processing in digital systems [1]. They influence the system performance and support other arithmetic operations (multiplication and division). The operation speed in terms of delay is the most significant constraint. Also a high-speed adder is a major prerequisite of the fast arithmetic operation [2].

The adders are used for various applications depending on the restraints each application holds with it. For example, multiplier is one type of component in microprocessors and controllers. Generally, the multiplications are carried out by repeated addition; hence, adders are crucial in multipliers. The multipliers' performance depends on the adders, which makes the whole system performance depend on the adder performance [3].

In Signal processing System Modules, the high-speed adder with low power and the minimum area plays a crucial role. Hence, it is necessary to investigate the area, power and delay parameter of the adder used in signal processing operations [4]. Several types of adders were considered for the addition of two binary numbers. They are Carry Save adder, Ripple Carry Adder [1], Carry Look Ahead Adder [1], Carry Increment Adder, Carry Select Adder [1–3,5], Han Carlson adder [6] and Brent Kung Adder [7].

The proposed adder designs are more suitable for digital signal/ biomedical signal processing applications such as OFDM, MIMO, multi-point transceivers, image blending [2], FIR filters[3], MAC, multimedia applications, matched filtering, video convolution functions [8], channel equalization, and various communication applications [9], hardware security in the field of IoT applications, *etc*.

The dddition is a significant arithmetic operation in many signal processing applications [1]. Hence, high-speed adder architecture is required to design such a signal processing module.

The objective of this work is to improve the speed and area of CSELA using a hybrid technique.

The contributions of this work can be summarized as follows:

(1) The proposed work is still scoped to reduce delay/area in CSA by introducing hybrid technology.
(2) The utilization of delay, area and power consumption are compared and analyzed in Vertex6 FPGA Board.
(3) In terms of delay and Area delay product (ADP) , the proposed CSELA is the best among all the adders.

This paper is systematized as follows. Section 2 surveys various 2 operand adders and their architecture. Section 3 describes the hybrid adder architecture. Section 4 proposed carry select adder architecture. Section 5 deals with performance analysis adders. Section 6 concludes the article.

2. ADDERS

2.1 Ripple Carry Adder (RCA)

RCA is a basic adder containing full adder cells connected in a cascade.Every full adder has to generate a sum and carry for respective binary bits. For each block, full adder carry is passed to the next full adder block as input carry. At every stage, the sum is not evaluated until receiving the previous stage output carry. The output carry and sum can be calculated as follows [1,8]. Thus, the total delay is all the stage delay plus the final carry output generation delay. RCA occupies the minimum hardware components among other adders [10]. But they are low speed due to the propagation of carry. This delay is the major disadvantage of RCA [1].

Pros: Requires minimum hardware components.

Cons: Exhibits low speed due to the propagation of carry.

2.2 Carry Look Ahead Adder

The No. of stages is increased, and hence more delay is introduced in RCA. To overcome this drawback, another technique, Carry Look-Ahead Adder (CLA), was used [1,2].

This CLA reduces the delay for generating the carry bits, as it introduces generate and propagate terms to calculate carry bits separately.

The propagate and generate signals are calculated using Equations (1) and (2) [1,4].

$$\text{Propagation}(P_i) = A_i \oplus B_i \tag{1}$$

$$\text{Generate}(G_i) = A_i \,\&\, B_i \tag{2}$$

Each Stage carry is generated separately using Equation (3) [1].

$$C_i = G_i + P_i \,\&\, C_{i-1} \tag{3}$$

Depending upon the no. of bits size, the no.of carry bits is determined [1].

Pros: Exhibits increased speed because the final output carry depends only on input carry.

Cons: Increases in the area due to the need for a separate circuit for generating the sum and carry.

2.3 Carry Save Adder (CSA)

Carry Save Adder is another version of parallel RCA ,but there is a small change in the architecture. It does not evaluate the carry through the stages. The carry is saved in the present stage, and renewed as an addend value in the next stage [4].

The benefit of a CSA is high-order bits have no dependency on any low-order bits, as all bit positions are calculated independently. The latency associated with carry bits is reduced in CSA.

Pros: All bit positions are calculated independently

Cons: The latency associated with carry bits.

2.4 Carry Skip Adder (CSKA)

In some applications (Design), there is no need to calculate intermediate carry for some combinations of inputs [2,6]. Hence, the carry skip logic was introduced. Even adding the more no. of bits, the CSKA is a fast as to RCA [6].

Pros: Increases the speed of operation because intermediate carry calculation for some designs is ignored.

Cons: Suitable for limited application.

2.5 Carry Select Adder (CSELA)

In CSELA [11], possible values of the input signal Cin (*i.e.* carry input "0" and "1") for each stage are recognized in advance, and the sum is calculated well in advance. The design unit of CSELA is displayed in Figure 1.

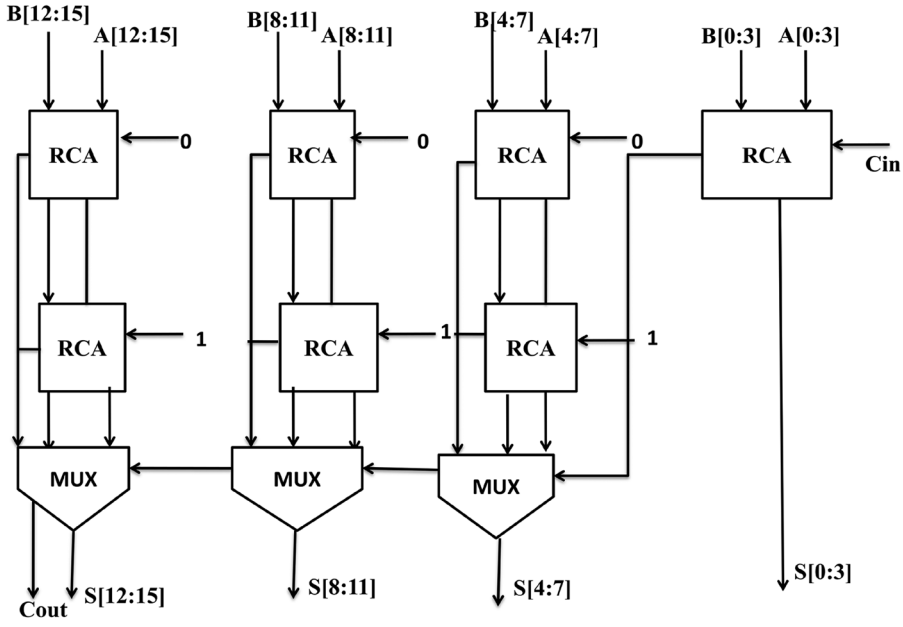

Figure 1: Architecture CSELA (16-bit)

Commonly, the CSELA [1,11] is designed using double RCAs and a multiplexer (it is used to select the final output carry and sum). The benefit of CSELA [1,11] is to decrease the carry propagation time. Consequently, the speed of operation is enhanced. But no. of full adders is higher than RCA [2,5].

Pros: The speed of operation is improved further with the help of dual RCA.

Cons: Occupies more area.

2.6 Carry Increment Adder (CIA)

Another method to improve the speed of operation is carry increment logic circuit. This logic has two RCAs and carry increment circuits. In this adder, two RCAs are simultaneously produced: sum and output Carry bits. The first stage output carry bit and the second RCA sum bits are passed to carry increment logic. The carry increment logic consists of a series of Half adders to form the final sum output bits [12].

Pros: Enhancement of power utilization.

Cons: The speed of operation is moderate.

2.7 Brent-Kung Adder

The BK adder is used to improve the speed of adder further. This uses parallel prefix calculation logic [5,7,8]. It consists of three phases, namely

(1) Pre-computation Phase: The propagate and generate signals of every pair of inputs A and B are computed. The computing expressions are mentioned in Equations (1) and (2). [8,11,12]
(2) Carry estimation phase: Every bit carry is computed simultaneously. The carry generate, carry propagate and intermediate signals are computed using Equations (4) and (5) [4,5,8].

Carry Generate

$$CG_{i:j} = G_{i:k+1} + (P_{i:k+1} \,\&\, G_{k:j}) \tag{4}$$

Carry Propagate

$$CP_{i:j} = P_{i:k+1} \,\&\, P_{K:j} \tag{5}$$

(3) Post-computation phase:

The final stage summations are calculated using Equation (6) [4,8]

$$Sum = P_i \oplus CG_i \tag{6}$$

The architecture of BK Adder is displayed in Figure 2.

Pros: Improves the speed of operation due to less wiring congestion [11].

Cons: Fan-out.

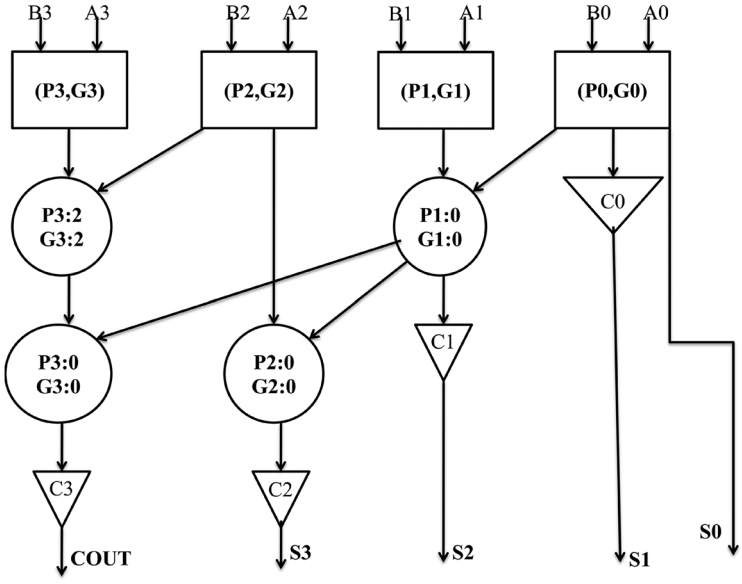

Figure 2: Brent-Kung Adder (4-bit)

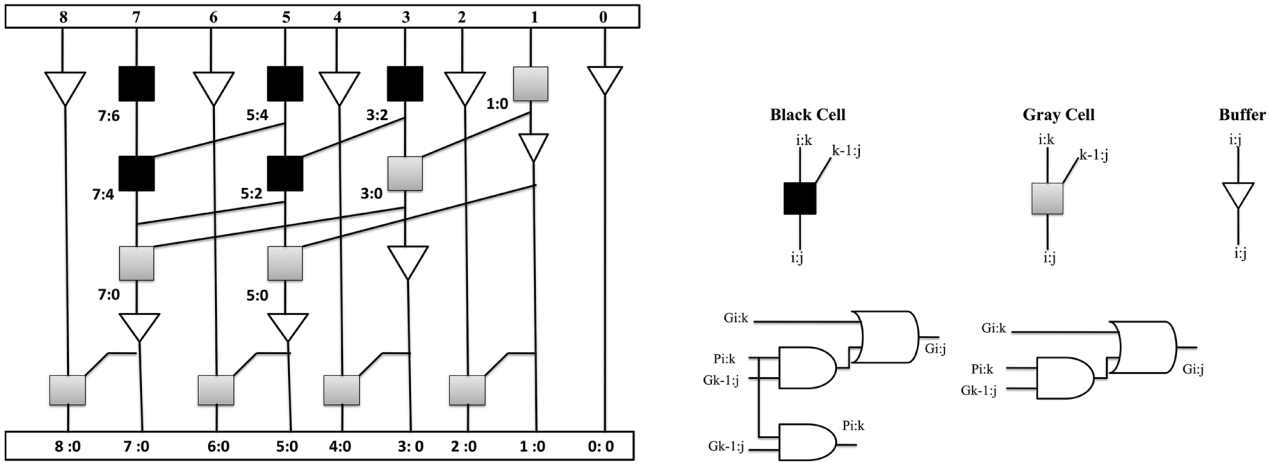

Figure 3: Han-Carlson adder

2.8 Hancarlson Adder

HanCarlson adder is designed using the principle of parallel prefix addition.

HanCarlson adder [11] is the mixture of KoggeStone [5] and BrentKung adder [11]. KoggeStone adder offers less delay, and BrentKung adder has less area [6]. The design of the HanCarlson adder is displayed in Figure 3.

Pros: Good trade-off between fan-out and the number of logic cells.

Cons: Longer path to the output.

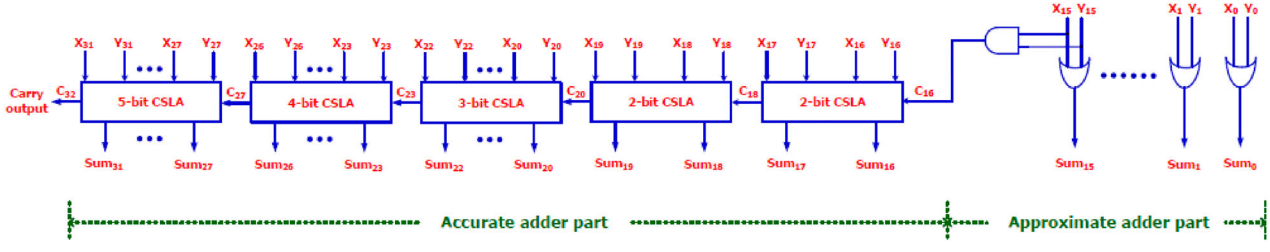

Figure 4: 32-bit modified adder with approximate part and accurate part

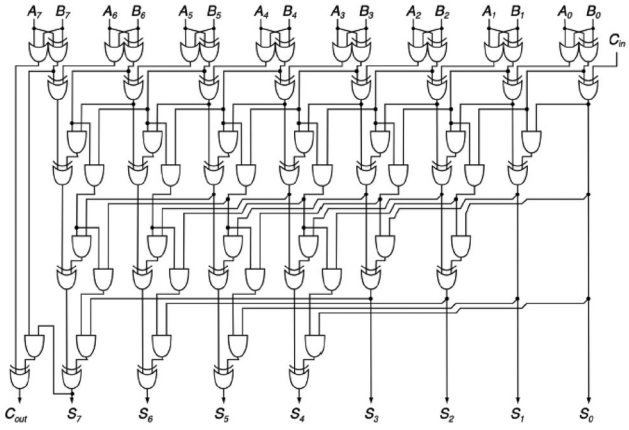

Figure 5: 8-bit Kogge-Stone sum-propagate adder

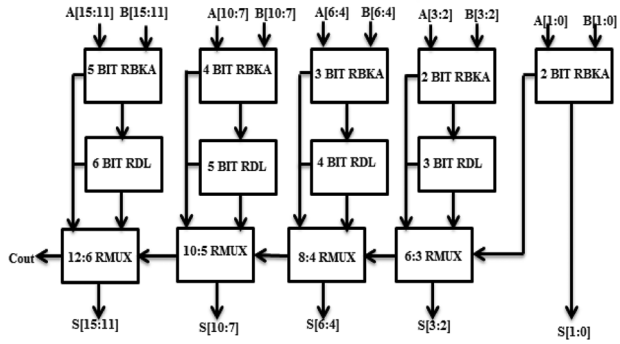

Figure 6: Reversible BK CSLA using D-latch

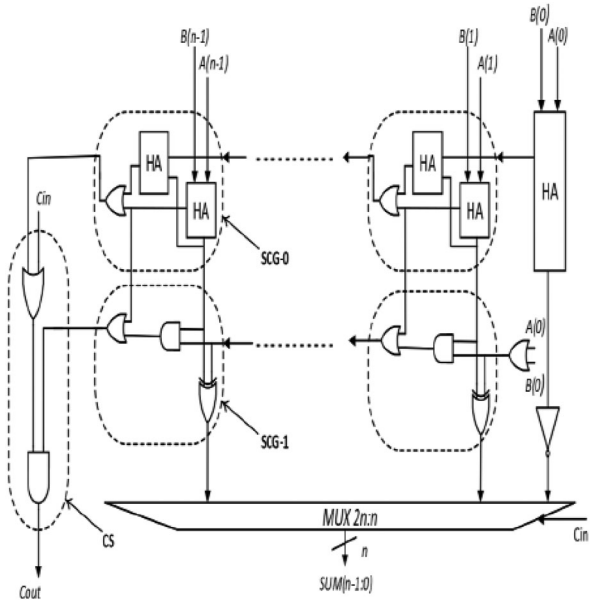

Figure 7: Single-stage CSLA

2.9 Modified High-speed Architectures

Padmanabhan.B *et.al* [1] proposed 32-bit approximate and accurate Carry select adder shown in Figure 4 for homogeneous and hybrid CLAs, and CSLAs with and without the BEC converters. The hybrid CLA/RCA architecture was preferred among CLA and CSLA designs in terms of speed and power to carry out the accurate and approximate additions.

G. Dimitrakopoulos *et al.* [4] proposed a Sum Propagate Adders, as shown in Figure 5, to perform addition by propagating directly the sum bits of previous bit positions instead of carries. New parallel-prefix structures that follow the sum-propagation architecture are presented using a new associative prefix operator. At present, and using current state-of-the-art implementation technologies, sum-propagate adders are executed slower operation than carry propagation adders.

Athira V. S [7] *et al.* designed a carry select adder with reversible logic to abridge power loss, as shown in Figure 6. To replace the BEC and BK adder, D-Latch and multiplexer combination, it helps reduce the power utilization and delay. The modified SQRT BK CSLA using D-latch has a slightly larger area, but power utilization and delay were reduced by 7.8% and 15%, respectively compared to the modified SQRT BK CSLA.

G. Kishore Kumar *et al.* [9] proposed a Reconfigurable Delay Optimized Carry Select Adder, as shown in Figure 7, to calculate the final sum before calculating the final carry. The delay of the proposed CSLA was improved by 31.6%, 23.3%, 27.1% and 36.9% compared to HSCG, CONV, BEC and CBL-based SQRT CSLAs, respectively.

Omid Akbari *et al.* [13] designed a fast reconfigurable approximate carry look-ahead adder with energy-efficient, as shown in Figure 8. It is suited for applying error-resilient and exact methods as it can switch between the approximate and exact operating operation. This design was more efficient in the area and power utilization than the conventional carry-look-ahead adder (CLA). In this, the delay is reduced by 55% and power reduction by 28% compared to exact CLA.

3. HYBRID-ADDER

The system designed using multiple logic structure styles in a combined manner is called a hybrid adder. The configuration of the hybrid adder is shown in Figure 9. In this configuration, A and B are the input signals in Module-1. Module-2 and Module-3 are in-between blocks of the adder. Different adder techniques are used in intermediate components to generate sum and carry outputs.

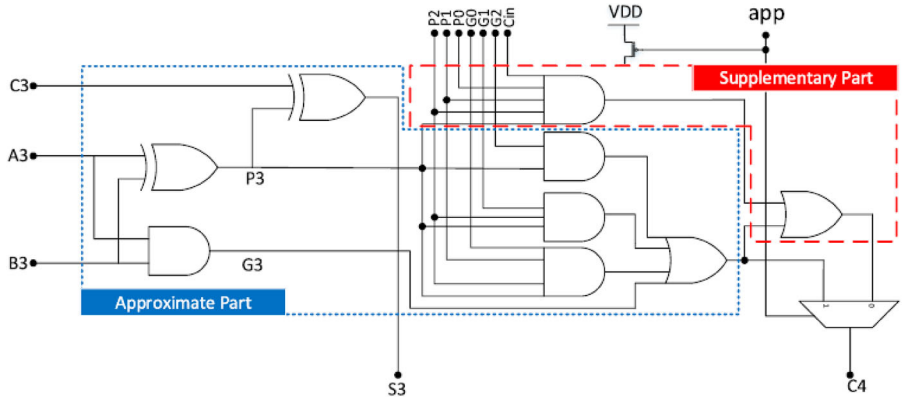

Figure 8: RAP-CLA structure

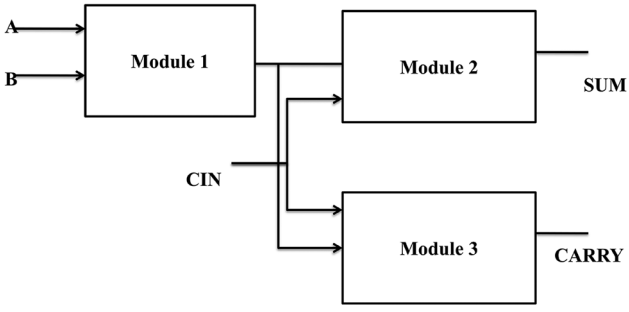

Figure 9: Structure of the hybrid adder

The following two design configurations are followed in the hybrid adder design.

(1) Homogeneous: a combination of a similar type of more than one adder structure is called homogeneous design [14,15].
(2) Heterogeneous: Combining the different types of more than one adder is called a heterogeneous design [14,15].

The proposed idea forms a hybrid configuration using structure (Figure 9) techniques to bring the high-performance and low-cost (chip size) products.

3.1 Linear Brentkung CSELA

The basic CSELA includes two RCAs and a single multiplexer. To reduce the area and delay of CSELA, the RCA (Cin = 0) is replaced by the BK Adder Structure. This type of design is known as LBKCSELA [9].

3.2 Square Root BKCSELA

The speed of operation is boosted using the Square root [9] concept in LBKCSELA. The 20-bit CSELA consists of five stages with equal bit sizes (each stage with 4 bits).

But the same 20-bit Square root BKCSELA consists of five stages with different input sizes (First^{t} stage 2 bits, Second stage 3 bits, Third stage 4 bits, and so on). Each group consists of two blocks, one for BKA (cin = 0), and another one for RCA(cin = 1). Also a different bit-sized multiplexer is used to select the sum output. This structure is called SQRTBKCSELA [10,11].

3.3 Modified Square Root BKCSELA

The delay of SQRTBKCSELA is reduced compared to Linear BKCSELA, but the size of the chip is increased. To reduce the chip area of SQRTBKSELA, the RCA (cin = 1) is replaced by the BEC Module [11]. Hence the no.of circuit elements is lower than that of N-bit RCA. This structure is called MSQRTBKCSELA [12,13,15]. The structure for Modified Square Root BKCSELA is displayed in Figure 10.

3.4 D LATCH-Based CSA

The power consumption is increased in BKCSELA. To reduce the power consumption, the D-Latch-based adder was used in CSELA. This D-Latch is used instead of BEC (Cin = 1) in BKCSELA [7,10].

3.5 Common Boolean Logic (CBL)-Based CSA

The carry select adder discussed in previous sections provides high speed but increases the chip area. To optimize the chip area, common Boolean logic is used in CSELA. In this way, a duplicated adder module is created to share the existing full adder and half adder outputs of RCA(cin = 0) in the conventional carry select adder. Hence, the no. of transistors and consumption of power is reduced. In CBL implementation [11], only a single OR gate and NOT gate is required to produce the sum and Cout output signal pair [10].

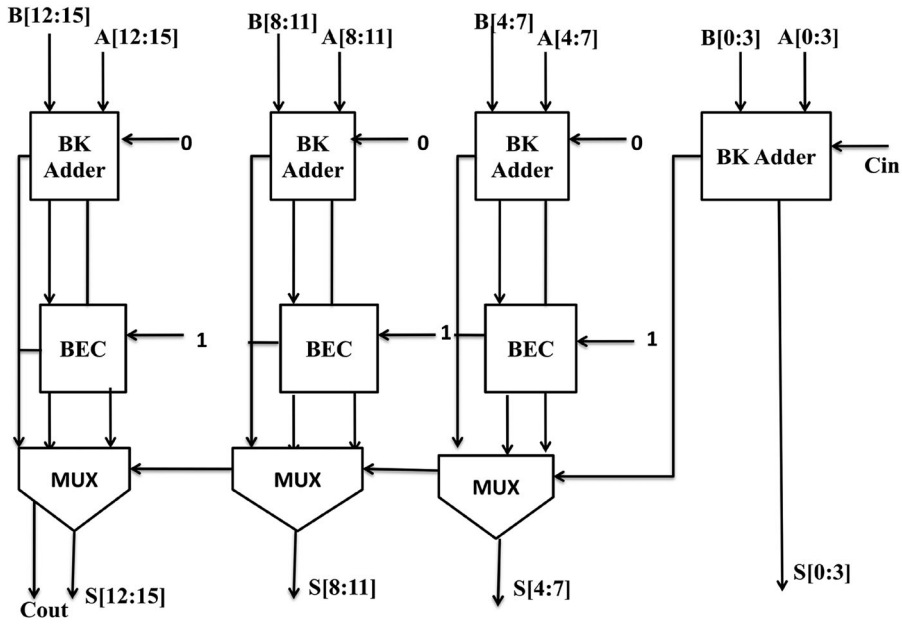

Figure 10: Modified Square Root BKCSELA

The CBL-Based adder consumes lesser area and lesser power consumption than the Modified CSELA [10,11]. The time delay of this adder is proportional to the no.of bits "N". Also, the time delay of the data selector (MUX) is lower than that of the full adder. Hence the speed of operation is more than the Regular CSELA.

3.6 Modified Linear Ling CSELA(LLCSELA)

In LBKCSELA, the Brent Kung stage is changed to Ling adder [12], as Ling adder provides lesser delay and minimum chip size compared to CLA [1,16].

It is called a Modified Linear Ling CSELA. The following expressions are used to calculate the Generate and propagate Bitwise signals Equations (1) and (2). [1,8,16]

Pros: Requires less Computation time to compute final carry.

Cons: Does not use regular layout Structure. For longer frequency delay, a problem is encountered.

3.7 Modified Linear Han Carlson CSELA

The speed of operation is improved in LBKCSELA as the BK stage is replaced by HanCarlson Adder [11,17]. The speed of the adder is further improved compared to the conventional Carry select adder. The architecture of Modified Linear HanCarlson CSELA is displayed in Figure 11. This technique obtains a better trade-off between the fan-out, no. of black cells and no. of logic levels [18].

3.8 Modified Linear CSELA Using Weinberger Adder (WCSELA)

The concept of the Weinberger recurrence algorithm[12] is used to calculate the carry for improving the delay of adder [19,20]. The BK adder is replaced by the Weinberger adder to create WCSELA [11].

The architecture of WCSELA is displayed in Figure 12. This adder utilizes a lower area (only minimum number of Gates required in BEC) compared to RCA. Also, the consumption of power and delay is low compared to Modified Linear Hancarlson CSELA, Common Boolean Logic (CBL)Based CSA [11] and D LATCH-Based CSA

Pros: Have the least area and overall delay.

Cons: Complexity will be increased for carry generation.

4. PROPOSED CARRY SELECT ADDER

The various adders are discussed in Sections 3 and 2. The major constraints of adders (Section 2 and 3) are the speed of operation; hence, it is necessary to concentrate on the delay (critical path of output) of an adder [19,20]. To improve the speed and area further, the proposed design adopts a new version of CSELA that is proposed using hybrid technology. The architecture of

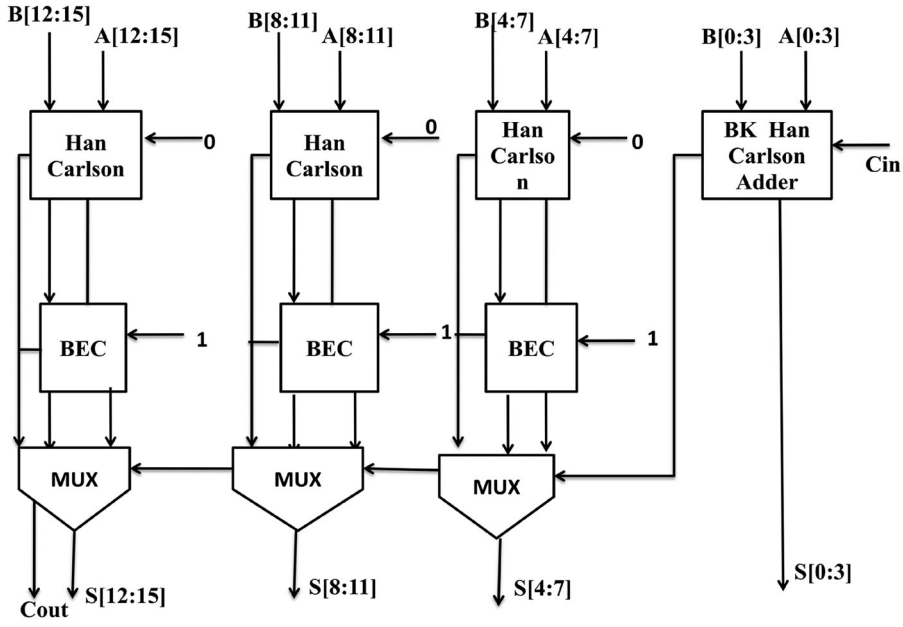

Figure 11: Structure for Modified Linear HanCarlson CSELA

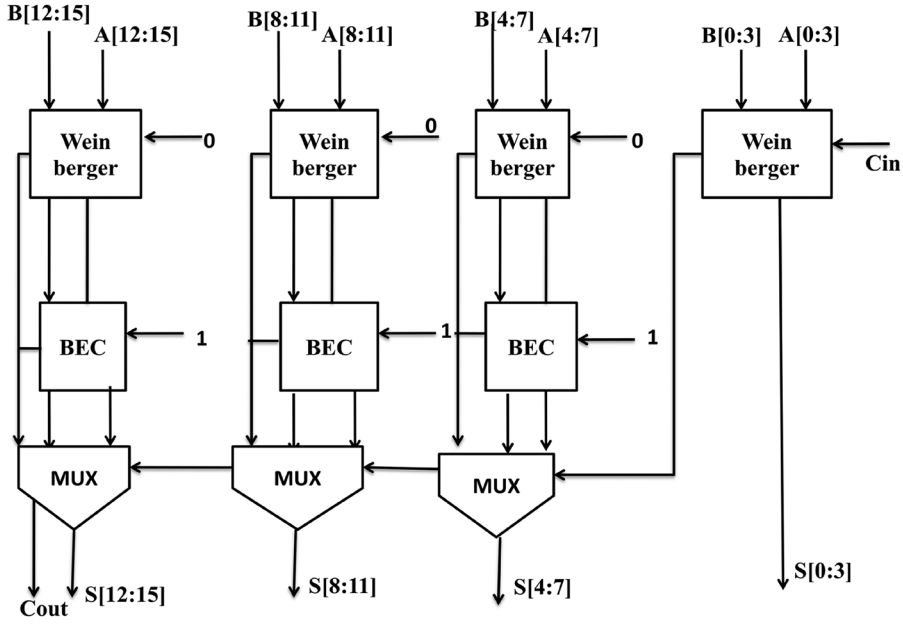

Figure 12: Architecture of (WCSELA)

the proposed CSELA is displayed in Figure 13. This proposed hybrid adder Figure 13 combines BEC, Hancarlson adder and multiplexer. The proposed 32-bit adder consists of two stages. Stages are Hancarlson adder stages (Stage 1-LSB), and hybrid Stages (Stages 2-MSB).

In the first stage, the bitwise addition of two 4-bit binary numbers is performed with the help of the Hancarlson adder. The details of the Hancarlson adder is discussed in Section 2.8. The Second Stage consists of seven modules, each with 4 bit. The bitwise addition of two 4-bit binary numbers is performed using carry select adder (2-bit adder, Binary to Excess one converter and 4:1 multiplexer),the 2-bit adder is produced the sum (2-bit) and carry (1-bit).

Here the 4-bit adder is divided into two 2-bit adders. This 2-bit adder performs the addition operation based on without input carry(assumed as zero input carry) and produces the sum(2-bit) and Carry (1bit). The sum is passed to the input of the BEC circuit This BEC circuit is added to the sum (sum+1). The multiplexer selects the sum based on the input carry (cin), and the first 2-bit adder output carry.

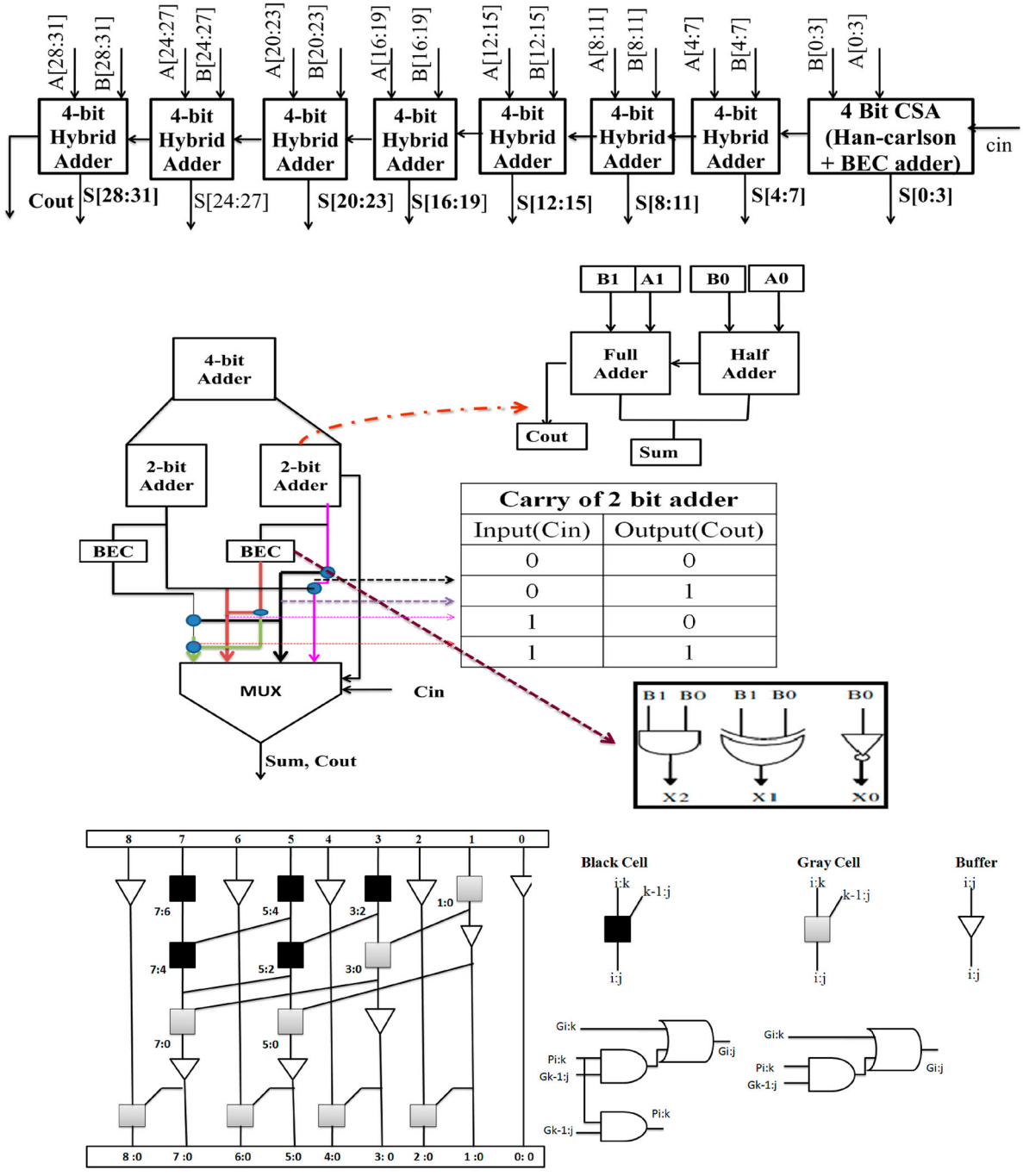

Figure 13: Proposed CSELA, (a) 32-bit adder, (b) 4-bit Hybrid Adder and (c) 4-bit CSA (Hancarlson)

The sum of 2-bit adder is passed to multiplexer(4-bit). The input of the 4:1 multiplexer is 2-bit adder sum based on the input and output carry of 2-bit adder(first). If the input and output carry 2-bit adder (1^{st}) is "00", then multiplexer output will be sums of 2-bit adders. If the input and output carry of 2-bit adder (1^{st}) is "01", then multiplexer output will be the first 2-bit adder sum and output of the second BEC. If the input and output carry of 2-bit adder (1^{st}) is "10", then multiplexer output will be the output of the first^{t} BEC and the output of the second 2-bit adder sum. If the input and output carry of 2-bit adder (1^{st}) is "11", then multiplexer output will be the output of the first and second BEC. Normally ripple carry adder is used for carry select adder with cin = 0 and 1.

The critical path delay of various adder architectures is observed as follows (i) RCA is the propagation delay of a 32-bit full adder, (ii) CLA is the summation of delay of four Full adders, 32-bit AND gate and 32-bit OR gate,(iii) Conventional CSA is the summation of delay of four Full adders plus seven Multiplexer (4:1), (iv) CSA-BK-BEC is the summation of delay of four Full adders, BEC (4 bit)

Table 1: Delay and area Evaluations of various CSELA in Vertex6 FPGA

S.No	Adders Techniques	16-bit		32-bit		64-bit	
		No. of Slice	Delay (ns)	No. of Slice	Delay (ns)	No. of Slice	Delay (ns)
1.	RCA	26	5.09	49	9.07	97	17.06
2.	CBL-Based CSELA	25	4.91	50	9.39	133	18.34
3.	CLA	24	4.60	48	8.59	96	16.58
4.	Weinberger BEC-based CSELA	30	3.32	62	5.71	124	10.74
5.	D Latched CSELA	42	4.21	84	7.62	168	14.46
6.	Brent Kung CSELA	36	3.44	72	5.20	144	8.80
7.	CSA-BK-RCA1	24	4.94	48	9.28	96	15.61
8.	Han Carlson BEC CSELA	36	3.44	72	5.20	144	8.80
9.	CSA Weinberger	30	3.32	62	5.70	124	10.74
10.	Conventional CSELA	24	4.94	48	9.28	96	15.54
11.	Ling CSELA	27	7.19	57	15.69	114	30.59
12.	Proposed CSELA	24	2.96	48	4.68	96	8.69
13.	WCSLA in [11]	25	12.28	–	–	–	–
14.	CIA Hancarlson [21]	24	10.09	–	–	–	–
15.	CBYA in [22]	–	–	57	24.63	–	–
16.	CSELA KSA in [15]	–	–	85	9.34	–	–
17.	BK Adder [18]	–	–	64	6.05	–	–
18.	EAll-CSLA in [17]	–	–	39	16.33	–	–

and seven Multiplexer (4:1) delays, (v) CSA-Hancarlson with BEC is the addition of delay of Four 2- Input AND gate, Four 2- input OR gate, one Buffer, BEC(4-bit) and seven Multiplexer (4:1).

In the proposed full adder, all the stages are performed simultaneously. Figure 13 shows that the maximum path delay (also called critical path delay) of the proposed adder is encountered as two full adder delay, one BEC (Binary to Excess one converter -3 bit) and seven multiplexers (4:1) delay for producing Cout. Compared to other adder delay, hown in Table 1, the delay of the proposed adder is decreased.

5. PERFORMANCE ANALYSIS

All the existing adders are discussed in Sections 2, 3 and proposed designs are discussed in Section 4. These adders are implemented in XILINX ISE 12.1 with a family of Vertex 6 devices (Device No. XC6VLX75T, Package FF484, Speed -3). and speed grade of -5 using Verilog HDL. Each adder is simulated and verified separately. The comparison chart for delay and area utilization of various CSELA is shown in Figures 14 and 15, respectively. Table 1 shows the delay and area (in terms of no. of the slice, LUTs) utilization of Various CSELAs.

Table 1 shows that the delay of the proposed 64-bit CSELA is improved 49.06%, 52.61%, 47.58%, 19.08%, 39.9%, 1.25%, 44.43%,19.08%, 44.07% and 71.59% compared to RCA,CBL-based CSELA,CLA, Weinberger BEC-based CSELA, D latched CSELA, Brent Kung RCA based CSELA, CSA Weinberger, Conventional CSELA and Ling CSELA respectively. Similarly Table 1 shows

Table 2: Comparison of synthesis of 32-bit adder results in Vertex6 FPGA

32 BIT Addition	No. of Slice	Delay(ns)	% of Improvements in delay
Proposed design	48	4.684	–
Brent kung adder in[18]	64	6.058	22.68
Modified adder-2 CSelA_KSA in [15]	85	9.344	49.87
CIA_HAN-CARLSON in [21]	34	10.091	53.58

that the Area Delay Product (ADP) of the proposed 64-bit CSELA is improved 49.58%, 65.79%, 47.58%, 37.35%, 65.65%, 34.16%, 44.37%, 34.16%, 37.35%, 44% and 76% compared to RCA, CBL-based CSELA, CLA, Weinberger BEC-based CSELA, D latched CSELA, Brent Kung CSELA, Brent Kung RCA-based CSELA, Han Carlson BEC CSELA, CSA Weinberger, Conventional CSELA and Ling CSELA, respectively.

In terms of delay and ADP the proposed CSELA is the best among the other adders in Table 2, because delay is improved by 22.68%.

Furthermore, the FIR filter (4-tap) is designed using the proposed hybrid adder and compared with the conventional FIR filter. This FIR system has utilized a delay of 30.06 ns. This FIR filter improved the delay by 30.02% compared to the conventional FIR Filter.

6. CONCLUSION

In this paper, a hybrid technology-based carry select adder (CSELA) is proposed, designed using the Hancarlson adder, Brent Kung adder and BEC circuit. To reduce the delay and area of the adder, these hybrid

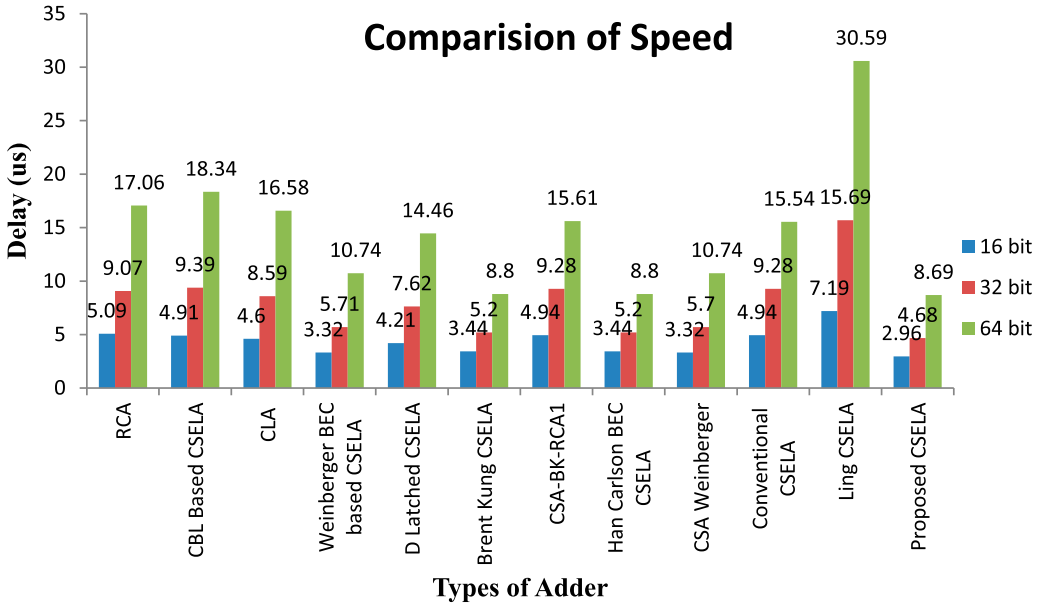

Figure 14: Delay Comparisons of Various Adders

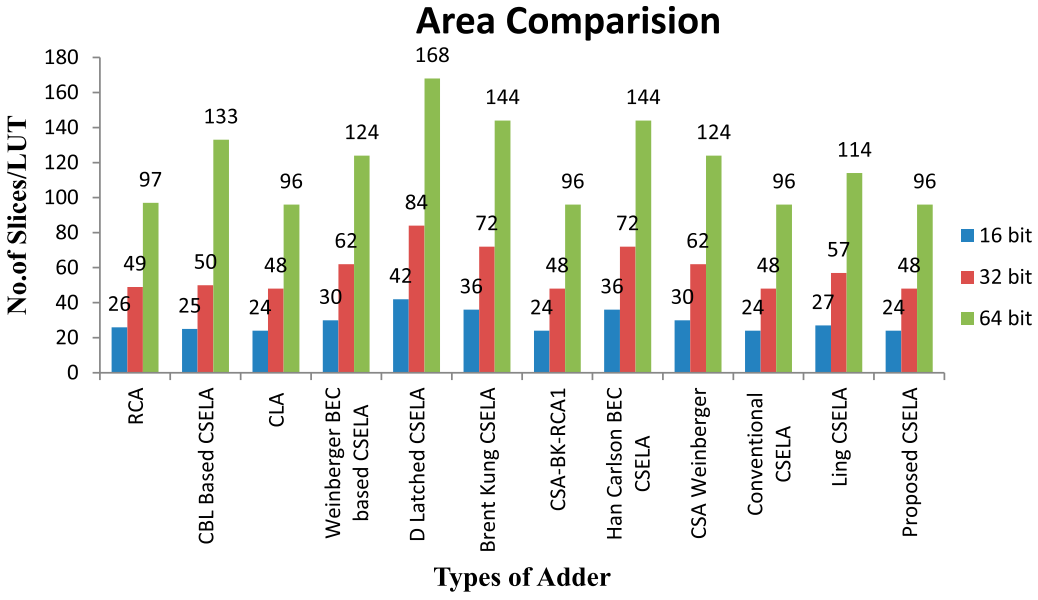

Figure 15: Area Comparisons of Various Adders

adders are used instead of a single RCA or BrentKung adder in CSELA. The simulation is carried out in Xilinx ISE 12.1 using Verilog HDL with the family of Vertex6 FPGA device (Device No. XC6VLX75T, Package FF484, Speed -3). The simulation report shows that the proposed hybrid 64-bit CSELA improves the Area delay product by 49.58%, 65.79%, 47.58%, 37.35%, 65.65%, 34.16%, 44.37%, 34.16%, 37.35%, 44% and 76% compared to RCA, CBL-based CSELA, CLA, Weinberger BEC-based CSELA, D latched CSELA, Brent Kung CSELA, Brent Kung RCA-based CSELA, Han Carlson BEC CSELA, CSA Weinberger, Conventional CSELA and Ling CSELA, respectively.

The delay of the proposed hybrid CSLA is optimized, as shown in Table 1. This may be increased by the power utilization, as shown in Table 3. The VLSI Design trade-off between speed, power and area will be there. Hence depending upon the applications, choose the suitable design.

Furthermore, this design can be extended to test the different input-sized (input bits) adders, multipliers, and filters and signal processing modules [23,24]. Also, it is possible to optimize the performance of ALU [21], DSP processors and data path modules using the proposed design. FIR filter [25,26] is the most important

Table 3: Delay and Power Evaluations of various CSELA in Vertex6 FPGA

		16-bit			32-bit			64-bit		
S.No	Adders Techniques	Power(uW)	Delay (ns)	PDP	Power(uW)	Delay (ns)	PDP	Power(uW)	Delay (ns)	PDP
1.	RCA	45.3	5.09	230.57	84.6	9.07	767.32	162.7	17.06	2775.66
2.	CBL-Based CSELA	44.5	4.91	218.49	82.3	9.39	772.80	158.4	18.34	2905.06
3.	CLA	46.2	4.60	212.52	88.4	8.59	759.36	159.5	16.58	2644.51
4.	Weinberger BEC-based CSELA	58.45	3.32	207.33	107.4	5.71	613.25	215.4	10.74	2313.40
5.	D Latched CSELA	69.45	4.21	292.38	126.4	7.62	963.17	230.45	14.46	3332.31
6.	Brent Kung CSELA	67.1	3.44	230.82	120.1	5.20	624.52	236.9	8.80	2084.72
7.	CSA-BK-RCA1	67.6	4.94	333.94	122.2	9.28	1134.02	238.5	15.61	3722.99
8.	Han Carlson BEC CSELA	67.1	3.44	230.82	120.1	5.20	624.52	236.9	8.80	2084.72
9.	CSA Weinberger	54.4	3.32	203.35	103.2	5.70	588.24	203.1	10.74	2181.29
10.	Conventional CSELA	66.4	4.94	328.01	112.4	9.28	1043.07	220.6	15.54	3428.12
11.	Ling CSELA	49.45	7.19	355.54	90.2	15.69	1415.71	160.4	30.59	4906.64
12.	Proposed CSELA	67.3	2.96	199.20	120.3	4.684	563.49	237.4	8.69	2063.01

module of many recent communication/ signal processing applications such as OFDM, MIMO [27], multipoint transceivers , *etc*. This hybrid CSELA can provide an optimal solution for designing the FIR filter [28,29].

DISCLOSURE STATEMENT

No potential conflict of interest was reported by the author(s).

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