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Certain Investigation on Multilevel Inverters for Photovoltaic Grid Connected System*

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This paper presents a photovoltaic (PV) system to convert the solar energy into electrical energy. DC power from PV system is converted into AC power using multilevel inverters. Cascaded H-bridge (CHB) inverter and diode clamped inverter (DCI) are used to convert variable DC power into sinusoidal AC power. Harmonic content is the important part to improve the efficiency of the inverter. Harmonics of CHB inverter and DCI are simulated and analyzed with different pulse width modulation (PWM) techniques.

Keywords: MPPT; PSPWM; LSPWM; IPDPWM; PODPWM; APODPWM; SVPWM.

1. Introduction

The developments of renewable energy resources are focused recently to reduce the pollution in the world. In the solar system, inverter is the important part to convert variable DC power into sinusoidal AC power and is connected to the electrical grid or to a local, off-grid electrical network.[1] Function of the inverter is fully controlled by a microcontroller. The microcontroller executes the algorithms to generate the

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triggering pulses to control the inverter. The controller is also used to obtain maximum power from the photovoltaic (PV) panel through algorithms called maximum power point tracking (MPPT).[2]

The purpose of using multilevel inverters in the grid connected system is having more benefits than the other inverters. Some of the advantages are less *dv/dt* rating, low switching stress, less harmonic content and low electromagnetic interference. There are three types of multilevel inverters used to convert DC to AC, namely diode clamped inverter (DCI), flying capacitor inverter and cascaded H-bridge (CHB) inverter.[3] Harmonic spectrums are simulated and analyzed for DCI and CHB inverter with phase shifted pulse width modulation (PSPWM), level shifted pulse width modulation (LSPWM) and space vector pulse width modulation (SVPWM) for various modulation indices.[4,5]

1.1. *The DCI*

There are totally $3(m-1)(m-2)$ clamping diodes, $6(m-1)$ active switches and $(m-1)$ DC link capacitors (where m is number of levels). Main problem in DCI is the deviation of neutral point due to unbalanced voltage and also the sharing of capacitor voltage is not equal. Single DC source is needed in DCIs. Nine-level DCI is simulated using different pulse width modulation (PWM) techniques and harmonics content of the DCI is compared with CHB inverter.[6]

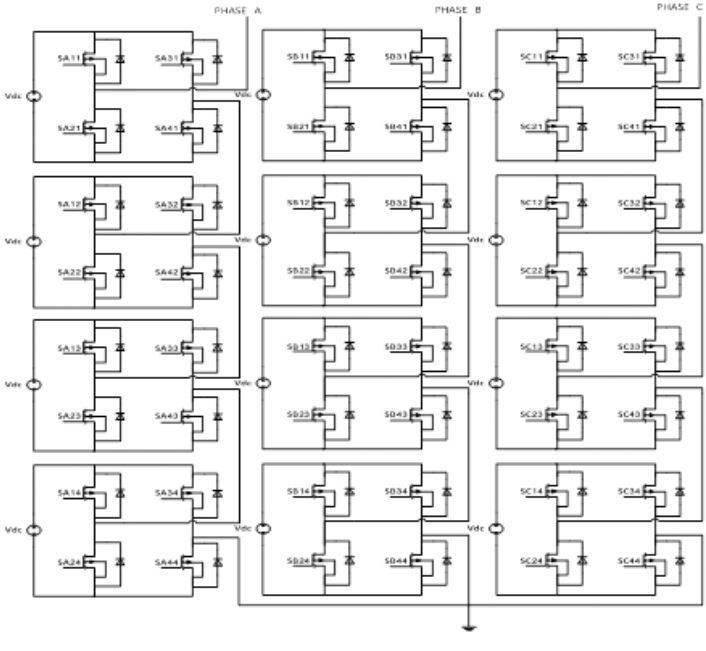

Fig. 1. Circuit diagram of nine-level CHB inverter.

1.2. *The CHB inverter*

This inverter consists of number of H-bridges connected in series. To form a $(2H + 1)$-level inverter, H numbers of H-bridges are cascaded.

Separate DC bus is required for each H-bridge and for m-level inverter, $2(m - 1)$ numbers of switches per phase and $2(m - 1)$ numbers of antiparallel diodes are needed.[7] Power circuit of the nine-level CHB inverter with RLC load is shown in Fig. 1. V_{dc} denotes the input DC bus voltage from PV array.

Table 1 shows the switching states of nine-level CHB inverter. An advantage of multilevel inverter is redundancy of switching state (to get the same level of voltage) and different switchings are possible, and it allows a flexibility in switching.[8] The above-mentioned switching states and corresponding voltage levels are obtained by different types of carrier-based PWM techniques.

Table 1. Switching states of CHB inverter.

	Switching states							
Phase voltage V_{AN}	S11	S31	S12	S32	S13	S33	S14	S34
0	1	1	1	1	1	1	1	1
$4V_{dc}$	1	0	1	0	1	0	1	0
$-4V_{dc}$	0	1	0	1	0	1	0	1
$3V_{dc}$	1	1	1	0	1	0	1	0
	1	0	1	1	1	0	1	0
	1	0	1	0	1	1	1	0
	1	0	1	0	1	0	1	1
$-3V_{dc}$	1	1	0	1	0	1	0	1
	0	1	1	1	0	1	0	1
	0	1	0	1	1	1	0	1
	0	1	0	1	0	1	1	1
$2V_{dc}$	1	1	1	1	1	0	1	0
	1	1	1	0	1	1	1	0
	1	1	1	0	1	0	1	1
	1	0	1	1	1	1	1	0
	1	0	1	1	1	0	1	1
	1	0	1	0	1	1	1	1
$-2V_{dc}$	1	1	1	1	0	1	0	1
	1	1	0	1	1	1	0	1
	1	1	0	1	0	1	1	1
	0	1	1	1	1	0	1	1
	0	1	1	1	1	1	1	0
	0	1	0	1	1	1	1	1
V_{dc}	1	0	1	1	1	1	1	1
	1	1	1	0	1	1	1	1
	1	1	1	1	1	0	1	1
	1	1	1	1	1	1	1	0
$-V_{dc}$	0	1	1	1	1	1	1	1
	1	1	0	1	1	1	1	1
	1	1	1	1	0	1	1	1
	1	1	1	1	1	1	0	1

2. Proposed Switching Methods for Multilevel Inverters

To generate a pulse for switch, two types of multiple carrier PWM techniques which have multiple carriers are compared with the reference signal.[9]

2.1. *PSPWM technique*

Total number of carrier signals needed for m-level CHB inverter with PSPWM is given by $(m-1)$. These signals are all equal in magnitude and having the same frequency; the signals are in a phase shift of φ which is given as

$$\varphi = 360^{\circ}/(m-1). \tag{1}$$

Pulse is generated for S11 during $V_{\text{ref}} > V_{\text{cr1}}$ (by comparing the reference signal V_{ref} with V_{cr1}), similarly pulses are generated for S12, S31 and S41 by using V_{cr2}, V_{cr3} and V_{cr4} respectively.

Likewise, pulses are generated for S31, S32, S33 and S34 by using V'_{cr1},V'_{cr2}, V'_{cr3} and V'_{cr4} which are in 180° phase shift with V_{cr1}, V_{cr2}, V_{cr3} and V_{cr4}, respectively when $V_{\text{ref}} < V'_{\text{cr}}$. Amplitude modulation index and frequency modulation index are given by $m_f = f_{\text{ref}}/f_{\text{cr}}$ and $m_a = v'_{\text{ref}}/v'_{\text{cr}}$, respectively.

Device switching frequency is given by

$$f_{\text{sw,dev}} = m_f \times f_{\text{cr}}. \tag{2}$$

Inverter switching frequency is given by

$$f_{\text{sw,inv}} = (m-1) \times f_{\text{sw,dev}}. \tag{3}$$

Total DC voltage is given by

$$E = ((m-1)/2)V_{\text{dc}}. \tag{4}$$

Utilization of maximum DC voltage is given by

$$V_{\text{AB1,max}} = \sqrt{3} \times (V_{\text{pk}}/\sqrt{2}) \times E = 0.612(m-1)V_{\text{dc}} \quad \text{for} \quad m_a = 1. \tag{5}$$

For nine-level inverter, carrier signals are in phase shift of 45° and the number of carriers signals are eight. Phase voltage (V_{AN}) of the inverter is given by

$$V_{AN} = V_{H1} + V_{H2} + V_{H3} + V_{H4}. \tag{6}$$

Voltages across H-bridges 1, 2, 3 and 4 are V_{H1}, V_{H2}, V_{H3} and V_{H4}, respectively. Phase voltage of the inverter is obtained by nine steps namely 0, V_{dc}, $2V_{\text{dc}}$, $3V_{\text{dc}}$, $4V_{\text{dc}}$, $-V_{\text{dc}}$, $-2V_{\text{dc}}$, $-3V_{\text{dc}}$ and $-4V_{\text{dc}}$. Figure 2 shows the comparision of carriers and references for PSPWM technique.

2.2. *LSPWM technique*

Total number of carrier signals needed for m-level CHB inverter with LSPWM is given by $(m-1)$. These signals are all equal in magnitude and having the same

frequency, and the signals are vertically disposed.[10] Pulse is generated for S11 during $V_{\text{ref}} > V_{\text{cr1}}$ (by comparing the reference signal V_{ref} with V_{cr1}), similarly pulses are generated for S12, S31 and S41 by using $V_{\text{cr2}}, V_{\text{cr3}}$ and V_{cr4}, respectively.

Likewise, pulses are generated for S31, S32, S33 and S34 by using $V'_{\text{cr1}}, V'_{\text{cr2}}, V'_{\text{cr3}}$ and V'_{cr4} which are in 180° phase shift with $V_{\text{cr1}}, V_{\text{cr2}}, V_{\text{cr3}}$ and V_{cr4}, respectively, when $V_{\text{ref}} < V'_{\text{cr}}$.

Frequency modulation index is given by

$$m_a = v'_{\text{ref}}/v'_{\text{cr}}(m-1) \quad \text{for} \quad 0 < m_a \leq 1. \tag{7}$$

Amplitude modulation index is given by

$$m_f = f_{\text{ref}}/f_{\text{cr}}. \tag{8}$$

Device switching frequency is given by

$$f_{\text{sw. dev}} = f_{\text{cr}}/(m-1). \tag{9}$$

Inverter switching frequency is given by

$$f_{\text{sw. inv}} = f_{\text{cr}}. \tag{10}$$

Total DC voltage is given by

$$E = ((m-1)/2)V_{\text{dc}}. \tag{11}$$

Utilization of maximum DC voltage is given by

$$V_{\text{AB1,max}} = \sqrt{3} \times (V_{\text{pk}}/\sqrt{2}) \times E = 0.612(m-1)V_{\text{dc}} \quad \text{for} \quad m_a = 1. \tag{12}$$

The types of LSPWM are as follows:

(a) In-phase disposition (IPD) PWM: All the carriers are in-phase with each other.
(b) Phase opposite disposition (POD) PWM: All the alternative carriers are oppositely disposed.
(c) Adjacent phase opposite disposition (APOD) PWM.

All the carriers below zero reference line are opposite to carriers above the zero reference line; and the carriers above zero reference line are in-phase with each other. By comparing the carriers and references, IPDPWM, PODPWM and APODPWM techniques are simulated.

2.3. *SVPWM technique*

In LSPWM and PSPWM techniques, all the references signals are compared with carriers individually. But in SVPWM technique, all the reference signals are

combined into a single vector. The vector is used to calculate ON time of each switch. If there is any change in the reference signal, it affects the ON times of all the switches which are used to maintain generated output voltage of inverter.[11]

To generate the SVPWM signal the following steps need to be carried out:

- From abc to α–β transformation (3φ–2φ transformation).
- Reference signal magnitude and angle calculation.
- Identification of sector.
- The dwell times T_0, T_1 and T_2 calculation.
- T_a, T_b and T_c calculation.
- To generate pulse for switches needed to compare T_a, T_b and T_c with V_{cr}.

DC utilization is higher than SPWM, which is an important advantage of SVPWM. Due to this same rating of load, it requires smaller voltage than SPWM. Utilization of maximum DC voltage is given by

$$V_{\text{AB1,max}} = (\sqrt{3}/\sqrt{2}) \times (2/3)V_{\text{dc}} \cos 30^\circ (m-1) = 0.707(m-1)V_{\text{dc}} \quad \text{for } m_a = 1. \tag{13}$$

Amplitude modulation index is given by

$$m_a = \sqrt{3} \times (\text{S}_{\text{ref}}/V_{\text{dc}}) \quad \text{for } 0 < m_{\text{a}} \leq 1. \tag{14}$$

Comparison of carrier signal and reference SVPWM pulse is then generated.

3. Analysis of Harmonics for CHB Inverter and DCI using Various PWM Techniques

Nine-level multilevel DCI and CHB inverter are simulated by using different PWM switching techniques. Harmonic content of line voltage is captured for both the inverters. Based on the value of harmonics for different pulses, graphs are obtained.

The line voltage THD variations of CHB inverter using different modulation techniques for modulation indices (m_a) 1, 0.8 and 0.6 are represented as 1, 2 and 3, respectively, with $f_s = 10,050$ Hz, as shown in Fig. 2. Harmonic content increases in the output parameters when m_a decreases. In Fig. 2, harmonic content of the inverter is low when SVPWM technique is used. The harmonic frequency of order $pm_f \pm qf_{\text{ref}}$ with p and q as even(odd) and odd(even) integers in SVPWM technique.

Figure 3 shows the harmonic spectrum of CHB inverter line voltage using SVPWM technique. Due to the movement of harmonic contents into high frequency, filter requirement, size and losses are reduced. Harmonic content is very low and maximum cut-off frequency of output filter of inverter is increased as 7,500 Hz up to 150th order. The 74 V DC bus for each H-bridge and 586.8 V (415 V rms) peak line voltage of inverter are supplied by PV array.

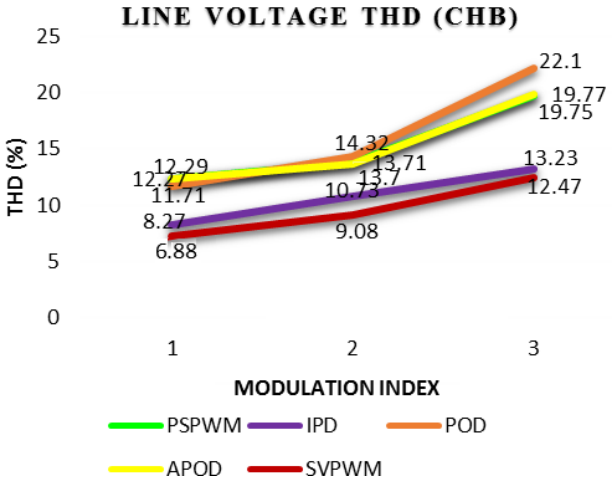

Fig. 2. Comparison of line voltage THD variations for CHB inverter with $f_{cr} = 10,050\,\text{Hz}$ for $m_a = 1$, 0.8 and 0.6.

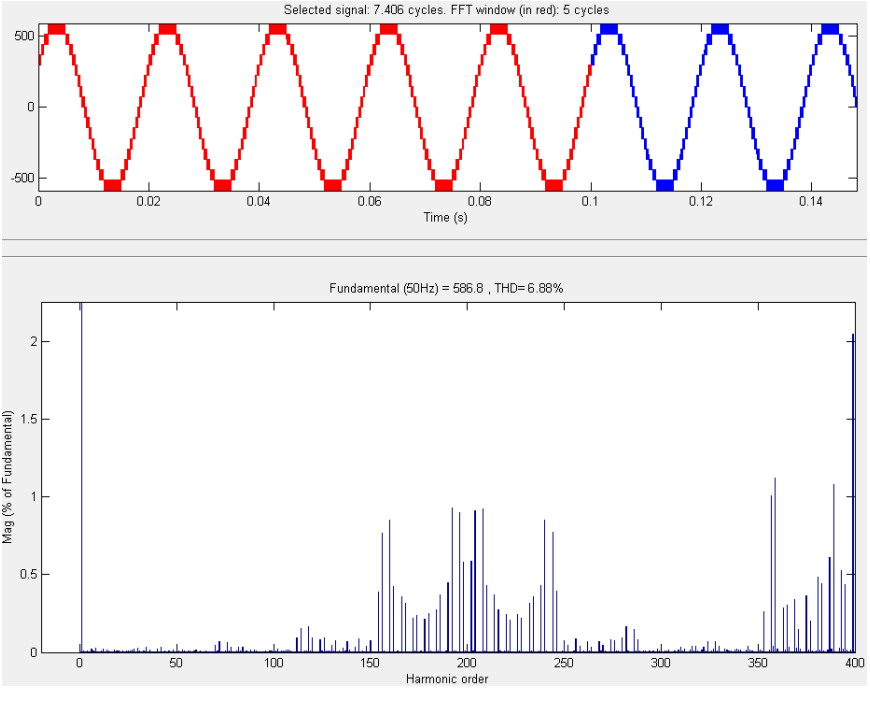

Fig. 3. Harmonic spectrum of CHB line voltage using SVPWM technique.

The line voltage THD variations of DCI using different modulation techniques for modulation indices (m_a) 1, 0.8 and 0.6 are represented as 1, 2 and 3, respectively, with f_s =10,050 Hz, as shown in Fig. 4. The harmonic spectrum of DCI using SVPWM is shown in Fig. 5. The harmonic specturm of line voltage in CHB inverter

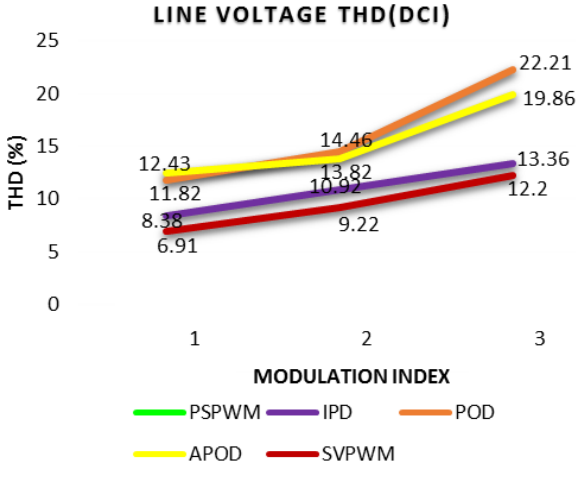

Fig. 4. Comparison of line voltage THD variations for DCI inverter with $f_{cr} = 10,050$ Hz for $m_a = 1$, 0.8 and 0.6.

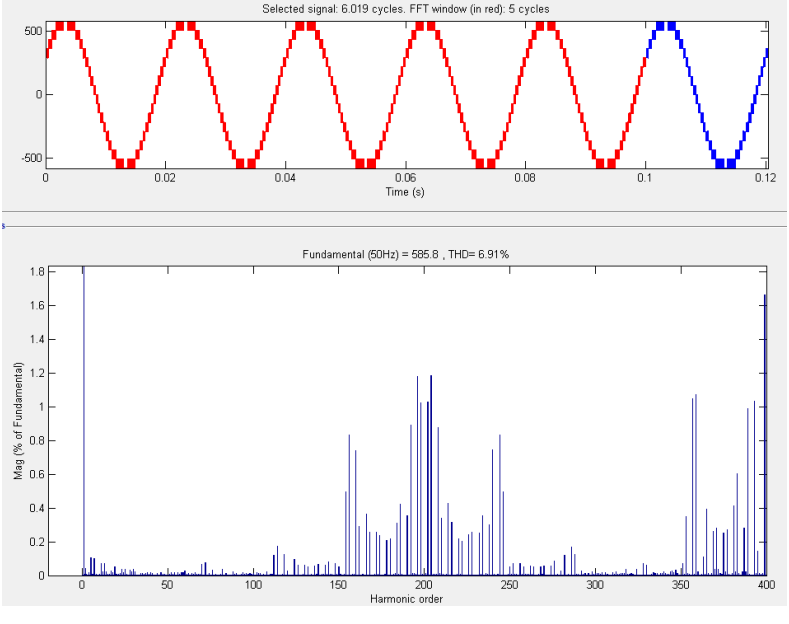

Fig. 5. Harmonic spectrum of CHB line voltage using SVPWM technique.

using SVPWM is 6.88% and the harmonic specturm of line voltage in DCI using SVPWM is 6.91%.

4. Comparison of CHB Inverter with DCI

CHB inverter and nine-level multilevel DCI line voltages are simulated using different types of PWM techniques. MATLAB simulation diagram of nine-level CHB inverter using SVPWM technique is shown in Fig. 6.

CHB inverter and DCI are compared based on line voltage harmonic contents for different PWM techniques. Figure 7 shows the comparison of the harmonic values of both inverters using POD switching technique. The harmonic spectrum of line

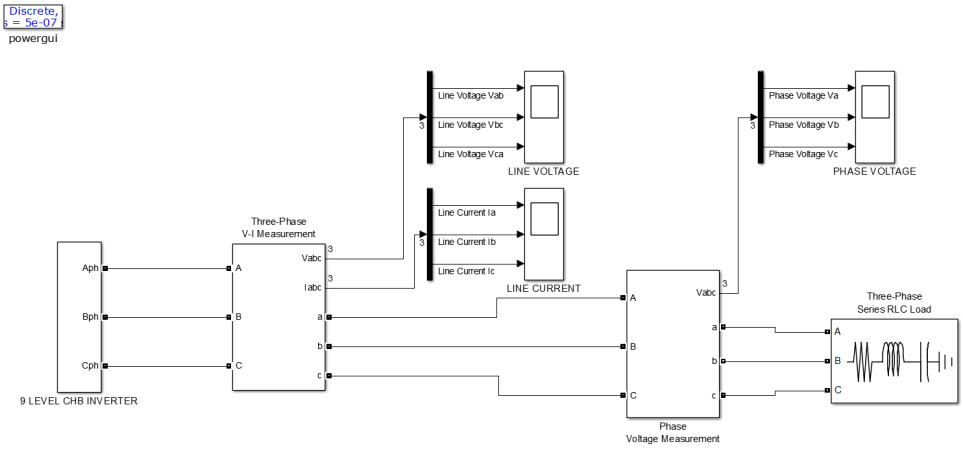

Fig. 6. Simulation diagram of nine-level CHB inverter.

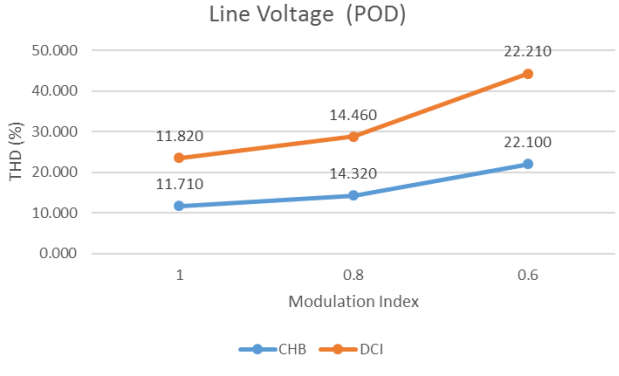

Fig. 7. Comparison of line voltage harmonic contents using POD switching technique with $f_{cr} = 10,050\,\text{Hz}$ for $m_a = 1$, 0.8 and 0.6.

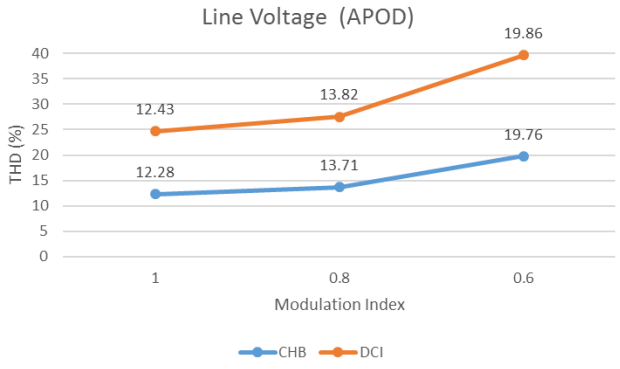

Fig. 8. Comparison of line voltage harmonic contents using APOD switching technique with $f_{cr} = 10,050\,\text{Hz}$ for $m_a = 1$, 0.8 and 0.6.

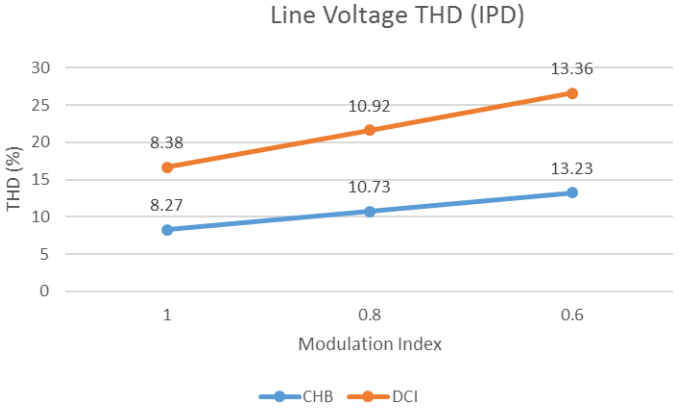

Fig. 9. Comparison of line voltage harmonic contents using IPD switching technique with $f_{cr} = 10,050\,\text{Hz}$ for $m_a = 1$, 0.8 and 0.6.

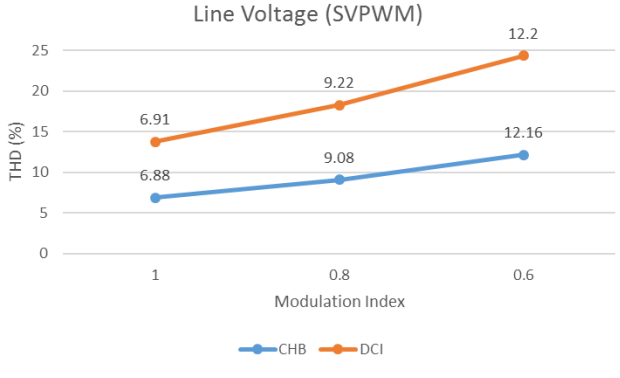

Fig. 10. Comparison of line voltage harmonic contents using SVPWM switching technique with $f_{cr} = 10,050\,\text{Hz}$ for $m_a = 1$, 0.8 and 0.6.

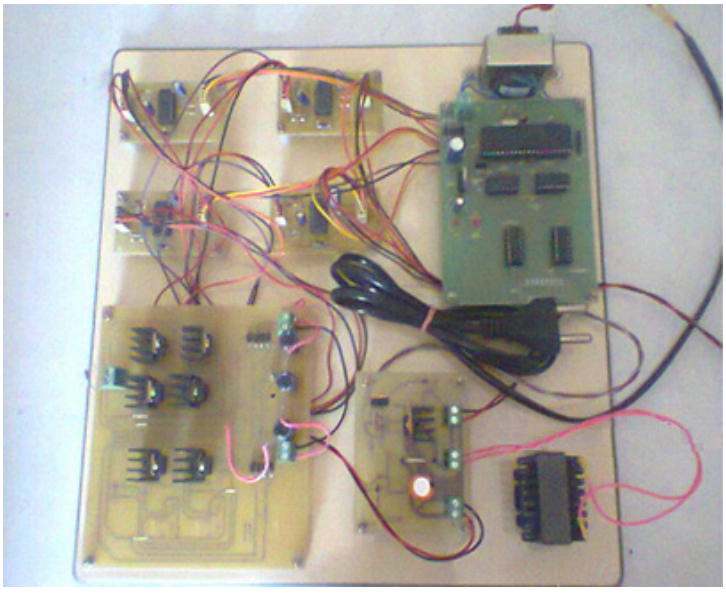

Fig. 11. Hardware implementation of CHB multilevel inverter.

Fig. 12. Experimental result of five-level CHB multilevel inverter.

Fig. 13. Harmonic spectrum of CHB multilevel inverter line voltage.

voltage in CHB inverter using PODPWM is 11.71% and the harmonic spectrum of line voltage in DCI using PODPWM is 11.82%.

Figure 8 shows the comparison of the harmonic values of both inverters using APOD switching technique. The harmonic spectrum of line voltage in CHB inverter using APODPWM is 12.28% and the harmonic spectrum of line voltage in DCI using APODPWM is 12.43%.

Figure 9 shows the comparison of the harmonic values of both inverters using IPD switching technique. The harmonic spectrum of line voltage in CHB inverter using IPDPWM is 8.27% and the harmonic spectrum of line voltage in DCI using IPDPWM is 8.38%.

Figure 10 shows the comparison of the harmonic values of both inverters using SVPWM switching technique. The harmonic spectrum of line voltage in CHB inverter using SVPWM technique is 6.88% and the harmonic spectrum of line voltage in DCI using SVPWM technique is 6.91%.

Hardware implementation of five-level CHB inverter is shown in Fig. 11. Line voltage and line current of CHB inverter is shown Fig. 12. Harmonic spectrum of five-level CHB inverter is shown in Fig. 13. The line voltage THD of the five-level CHB inverter is 7.2%.

5. Conclusion

Nine-level CHB inverter and DCI are simulated using different PWM techniques such as PSPWM, LSPWM, IPDPWM, PODPWM, APODPWM and SVPWM at different modulation indices ($m_a = 1$, 0.8 and 0.6) with f_{cr} as 10,050 Hz and with a power rating of 5 kVA. Line voltage THD of CHB inverter is 6.88% and line voltage THD of DCI is 6.91%. Based on the results of this paper, among different modulation techniques, the CHB inverter topology works better to reduce the THD, compared to multilevel DCI.[1] SVPWM technique is having a lower harmonic content compared to all other PWM techniques.

References

1. J. Selvaraj and N. A. Rahim, Multilevel inverter for grid-connected PV system employing digital PI controller, *IEEE Trans. Ind. Electron.* **56** (2009) 149–158.
2. J. Rodriguez, J.-S. Lai and F. Z. Peng, Multilevel inverters: A survey of topologies, controls, and applications, *IEEE Trans. Ind. Electron.* **49** (2002) 724–738.
3. V. Nagabhaskar Reddy, Ch. Sai Babu and K. Suresh, Advanced modulating technique for diode clamped multilevel inverter fed induction motor, *ARPN J. Eng. Appl. Sci.* **6** (2011) 90–99.
4. A. Nabae and H. Akagi, A new neutral-point clamped PWM inverter, *IEEE Trans. Ind. Appl.* **IA-17** (1981) 518–523.
5. J. Pou, R. Pindado and D. Boroyevich, Voltage-balance limits in four level diode-clamped converters with passive front ends, *IEEE Trans. Ind. Electron.* **52** (2005) 190–196.
6. T. Meynard and H. Foch, Multi-level choppers for high voltage applications, *Eur. Power Electron. J.* **2** (1992) 45–50.
7. D.-W. Kang, B.-K. Lee, J.-H. Jeon, T.-J. Kim and D.-S. Hyun, A symmetric carrier technique of CRPWM for voltage balance method of flying capacitor multilevel inverter, *IEEE Trans. Ind. Electron.* **52** (2005) 879–888.
8. B.-R. Lin and C.-H. Huang, Implementation of a three-phase capacitor clamped active power filter under unbalanced condition, *IEEE Trans. Ind. Electron.* **53** (2006) 1621–1630.
9. X. Kou, K. Corzine and M. Wielebski, Overdistention operation of cascaded multilevel inverters, *IEEE Trans. Ind. Appl.* **42** (2006) 817–824.
10. R. S. Kanchan, M. R. Baiju, K. K. Mohapatra, P. P. Ouseph and K. Gopakumar, Space vector PWM signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages, *IEE Proc., Electr. Power Appl.* **152** (2008) 297–309.
11. N. Celanovic and D. Boroyevich, A fast space-vector modulation algorithm for multilevel three-phase converters, *IEEE Trans. Ind. Appl.* **37** (2008) 637–641.