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Performance Analysis of Digital Circuits Device under Test at Different FPGA Families

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ABSTRACT: Despite their tremendous success over the years, the Digital circuits are still confronted with some of the critical challenges such as, manufacture, maintenance, and repair. To fulfill this, digital integrated circuits industry defined an Integrated Automatic test generation (ATG) / Automatic Test Equipment System for complex boards / circuits, which comprises Low Cost, Reconfigurable and easy to use digital circuits. It allows circuit parameters to be extracted from HDL Simulation then functionality is verified by using Xilinx Environment. The aim is to develop an ATG technique called Behavior - Based Automatic Test Generation technique (BBATG), where the system uses the structural model to describe circuit board as an interconnection of devices. Thus application of a deterministic algorithm to deduce the tests for complex circuit boards. Unlike most other deterministic ATG using the stuck-atfault model, BBATG use the device behavior fault model which can completely describe functions and pin timing relations for a combination or sequence device, and then needn't decompose devices to gate-level descriptions. The objective of the functional testing is to validate the correct operation of the system with respect to its functional specifications. Functional Testing is carried out for a small number of vector combinations. The main focus is based on easy-to-use and reconfigurable automatic test machine referred as FATE (FPGA-based ATE). So the test generation for digital circuits with VLSI can be further simplified and optimized. The designed FATE is verified with and without fault using Xilinx software and result are included.

KEYWORDS: ATG, BBATG, Xilinx software, FATE.

I. INTRODUCTION

Testing in its broadest sense means to examine a product and to ensure that it functions and exhibits the properties and capabilities that it was designed to possess. Main purpose of testing is to detect malfunctions in the product hardware and to locate their causes so that they may be eliminated. Conventional Test Methods rely primarily on mechanical means and not on use of additional circuits in an OTBT for the purpose of facilitating its testing. Example: Including extra I/O for additional test points, improvement of test features.

The Basic characteristics of conventional methods are used for testing system parts only outside the system, Rely on feeding signals directly through the test interface during listing and Rely on the use of tester-driven timing. Some of the Difficulties in Testing's are Shortage of I/O points, Signal distortions in interface connection, Noise disturbances, Uncertainties in input feeding, Uncertainties in output sensing. (Rejection of good parts reduces apparent yield.), Difficulty in synchronizing test objects timing with tester timing, High costs for test equipment, test generation and execution, and Large volume of data to be processed.

FAULT DIAGNOSIS SYSTEM

The VLSI circuit manufacturer cannot guarantee the defect- free integrated circuits(IC's).This makes to evolve a fast accurate means of testing such circuits. In a small-scale environment, it may not be feasible to invest large sums of money into complex IC testers. In labs till now Digital testers which will test IC's based on some non-functional

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parameters like temperature, any short circuits in the IC etc. & are used for testing only Combinational circuits. The digital pattern generator and logic analyzer are used to test the combinational, sequential circuits.

Automatic Test Equipment is a test setup used to detect and diagnose the faults of any DUT (Device under Test).ATE technology has evolved considerably over the years, matching the diagnostic test requirements of advancing avionics. ASIC manufacturers generally resort to the companies when chip development phase has been resolved and an accurate digital test program is ready to be executed by the high-end commercial ATEs [3].

A versatile but inexpensive, testing system for standard digital IC's (7400-series transistor-transistor logic (TTL) based on the use of a FPGA is ATE (Automatic Test Equipment). This tester can be economically implemented for small or medium-scale users of such IC's & provides a quick but thorough checkout of most small & medium-scale functions with minimal operator action. Dedicated special-purpose hardware is minimal, allowing this tester to be implemented on virtually FPGA. Each IC is tested by applying test patterns to input pins of the chip & the resulting chip outputs are then examined for errors resulting from the stuck-at conditions or other functional errors. For Dedicated ATE, all input & output patterns are compacted and stored in a data base and are compared with the expected outputs. For Generalized ATE, the DUT output can be stored in the Logic analyzer& user need to check the functionality based on the input & output results. This ATE can be used to test the combinational and sequential circuits.

The test set for each IC is an exhaustive set of all possible input combinations; this ATE is used for SSI & MSI functions. Earlier the digital IC testers are implemented using Intel micro-processor family. Test patterns are applied to each IC to be tested from a lookup table stored in the memory. Along with appropriate clock signals if needed. Reconfigurable logic device has programmable interconnects so that user can realize desired function in it.

It is also called programmable logic device (PLD) or field programmable gate array (FPGA). Recently logic capacity of PLD becomes large enough to realize various data processing functions within it. Although PLD's performance is not as high as ASIC when it is designed for the same application, its re-programmability has advantages & many applications are proposed. PLD system can be over 100 times faster than processor based system for applications with high parallelism.

Two main categories of ATE machines are available nowadays on the market: high-end ATE and low-cost ATE. High-end ATEs are characterized by high grade of automation, digital and analogy test capability, high-current pin protections and high-speed test execution [2]. On the other hand they are very expensive and require an accurate setup and skilled people, so ASIC manufacturers also needs some other testing solution, which can be executed in house during preliminary chip evaluation phase, when the use of an aforementioned ATE should be unnecessary in terms of time and money. In last decade, beside this range of performing ATE machines low-cost ATEs took place in market.

The main focus is based on easy-to-use and reconfigurable automatic test machine referred as FATE (FPGA-based ATE) .The FPGA is very versatile thus allows us to realize a home-made low-cost ATE to check for the functional correctness of the circuit. Many VLSI designers propose into market various kinds of quick, flexible and feature-rich development boards featuring various sized FPGA.

II. PROBLEM DEFINITION

To develop an efficient test generation method for digital integrated circuits having reduced test generation complexity, high fault coverage and low test application time. Test generation technique is based on the Behavior-Based Automatic Test Generation technique (namely BBATG) should generates behavioral based faults. To perform device tests and yield analysis on their desktop and then transfer the test program directly to FPGA-based ATE (FATE) System.

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BLOCK DIAGRAM

The block diagram of the proposed system shown in Fig 1 consists of Test pattern generation, FSM Load/Write, Generation of Stimulus, Loading data in Flash Memory and Report generation.

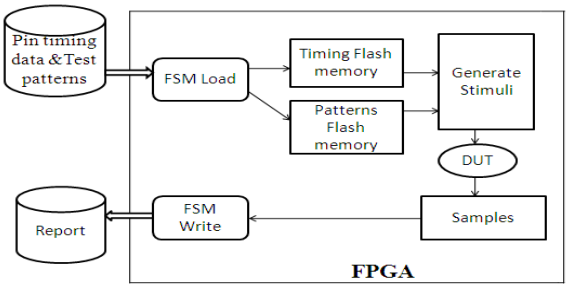

Fig 1: *Block Diagram of Proposed System*

BBATG TECHNIQUE

The three main components behind the BBATG technique are behavior-based device model, set of reusable device test libraries and automatic test deduction algorithm.

Circuit board model: A circuit board is defined as a system of an interconnection of components. In such a structural model, devices are at the lowest level and consequently are considered as primitive components.

Device model: A device is defined as a black box whose behaviours can be represented by the relationship between its inputs and outputs. Accordingly a device's behaviour model is described as its functional representation with the associated timing relations between the inputs and outputs.

Device Behaviour fault model: A device has a behaviour fault when its behaviour fails. In system test deductions, we only review device behaviour faults. Wire faults between individual devices in a system are attributed as faults at the connecting devices. In order to detect and diagnose fan-in/fan-out faults at system initial input/output pins, users can treat each system connector interface as one device so that wire faults are converted to device faults.

Test pattern generation technique makes use of Behaviour- Based Automatic Test Generation technique (BBATG).In BBATG, a behaviour error signal is presented as an "H" or "L". "H" represents "1" when the signal is normal and "0" when fault; "L" implies "0" when the signal is normal and "1" when fault.

III. RESULTS AND DISCUSSION

SIMULATION

It can perform the functional and timing simulation of your design with the ModelSim®-Altera Edition software, or any EDA simulators supported by Quartus II software. The Quartus II NativeLink feature allows you to run your third-party simulator and other EDA tools from within Quartus II software.

POITR PLAY ANALYZER FLOW

The Quartus II Poitr Play poitr analysis and optimization tools allow you to estimate poitr consumption throughout the design cycle. They use poitr optimization technology, which provides on average a 10-percent reduction in poitr consumption. The Altera Poitr Play Early Poitr Estimator estimate poitr consumption and produces a Microsoft Excel-based spreadsheet with estimate information. The Poitr Play poitr analyzer performs post-fitting poitr analysis and reports poitr characteristics by device resource and design entity.

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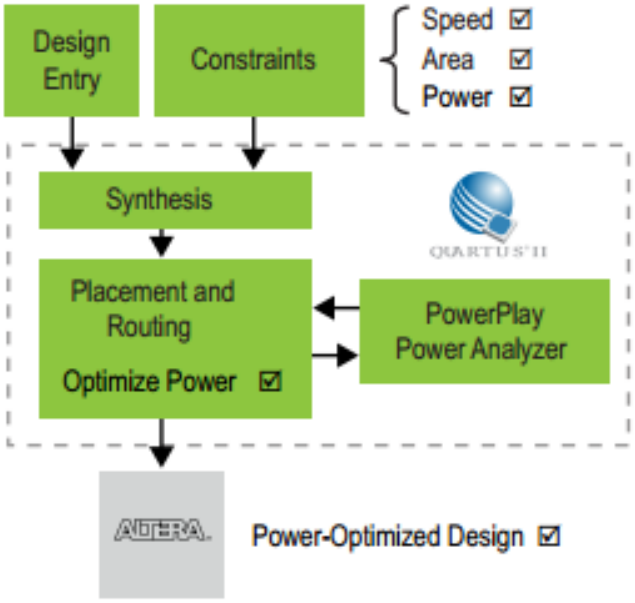

***Fig2**: Flow of Poitr Estimation.*

OUTPUT SCREENSHOTS

The Simulation Output without fault is observed as '0' for out sum and out_cout for the given inputs on the, b, c_{in}, sel, rst pin the output is processed from the flip flops, full adder and multiplexer.

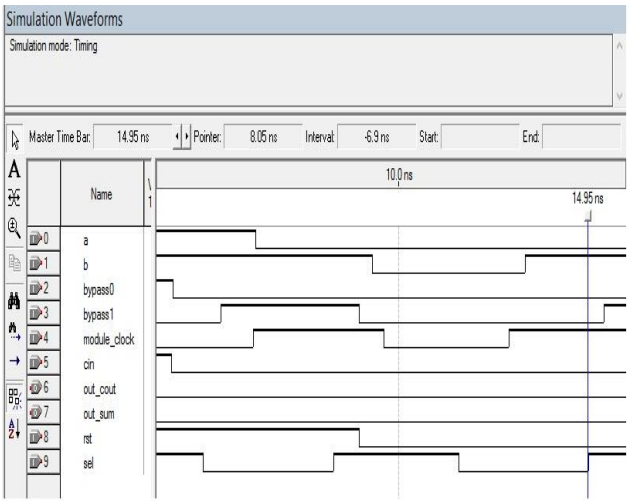

***Fig 3**: Simulation Waveforms*

The Fig 3 shown above is based on the parameter that is free from fault, in which the fault parameters are based timing delay and behavioural i.e., Boolean function of any digital circuits used.

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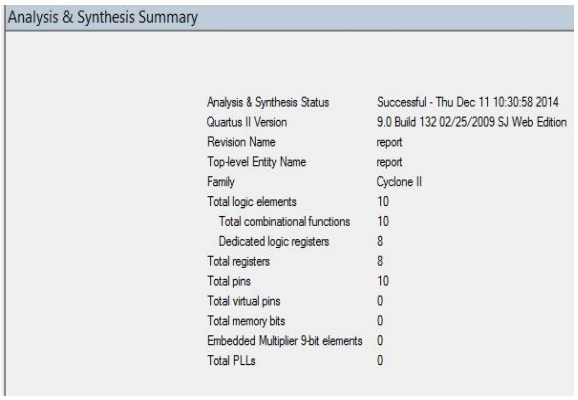
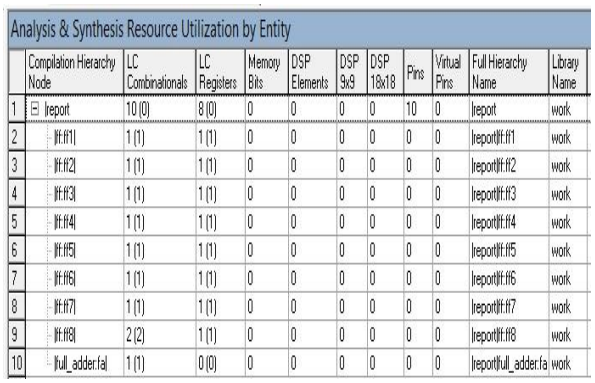


Analysis & Synthesis Summary

Analysis & Synthesis Status	Successful - Thu Dec 11 10:30:58 2014
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	report
Top-level Entity Name	report
Family	Cyclone II
Total logic elements	10
Total combinational functions	10
Dedicated logic registers	8
Total registers	8
Total pins	10
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0

***Fig4**: Analysis and Synthesis Summary.*

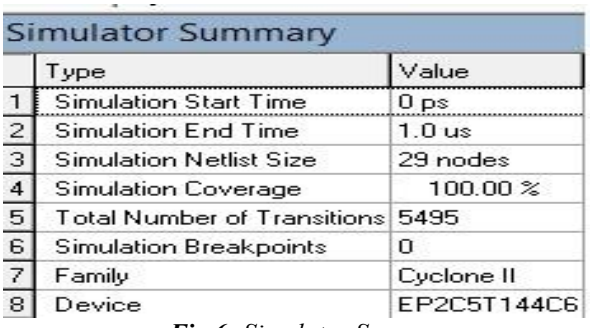


Analysis & Synthesis Resource Utilization by Entity

	Compilation Hierarchy Node	LC Combinationals	LC Registers	Memory Bits	DSP Elements	DSP 9x9	DSP 18x18	Pins	Virtual Pins	Full Hierarchy Name	Library Name
1	⊟ |report	10 (0)	8 (0)	0	0	0	0	10	0	|report	work
2	|ff:ff1|	1 (1)	1 (1)	0	0	0	0	0	0	|report|ff:ff1	work
3	|ff:ff2|	1 (1)	1 (1)	0	0	0	0	0	0	|report|ff:ff2	work
4	|ff:ff3|	1 (1)	1 (1)	0	0	0	0	0	0	|report|ff:ff3	work
5	|ff:ff4|	1 (1)	1 (1)	0	0	0	0	0	0	|report|ff:ff4	work
6	|ff:ff5|	1 (1)	1 (1)	0	0	0	0	0	0	|report|ff:ff5	work
7	|ff:ff6|	1 (1)	1 (1)	0	0	0	0	0	0	|report|ff:ff6	work
8	|ff:ff7|	1 (1)	1 (1)	0	0	0	0	0	0	|report|ff:ff7	work
9	|ff:ff8|	2 (2)	1 (1)	0	0	0	0	0	0	|report|ff:ff8	work
10	|full_adder:fa|	1 (1)	0 (0)	0	0	0	0	0	0	|report|full_adder:fa	work

***Fig 5:** Analysis and Synthesis Resource Utilization by Entity*

The Figure 4, 5 shows the Internal Analysis and Synthesis for the DUT. It may obtain this state by applying the Analysis and Synthesis View Section once again and it may verify the Device Components which are taken as DUT.



Simulator Summary

	Type	Value
1	Simulation Start Time	0 ps
2	Simulation End Time	1.0 us
3	Simulation Netlist Size	29 nodes
4	Simulation Coverage	100.00 %
5	Total Number of Transitions	5495
6	Simulation Breakpoints	0
7	Family	Cyclone II
8	Device	EP2C5T144C6

***Fig 6:** Simulator Summary*

The Figure 6 shows the Simulator Summary for the DUT. It may obtain this state by applying the Simulator Summary View Section once again and It may verify the Device Components which are included as DUT where each element consumption of simulation start time, end time, net list size, coverage, total number of transitions and device.

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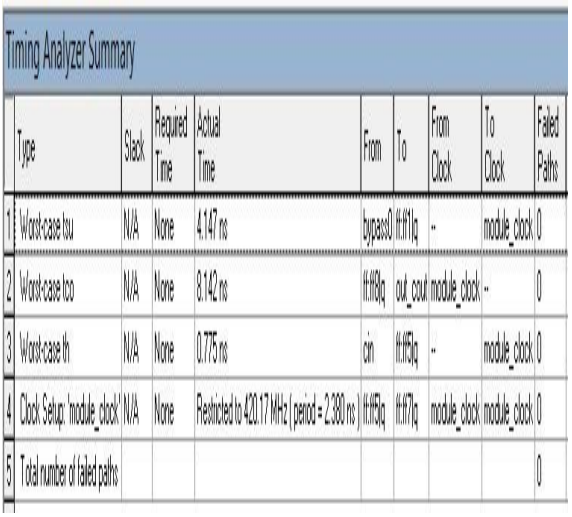

Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths
1	Worst-case tsu	N/A	None	4.147 ns	bypass0[1]	ff1[1]q	--	module_clock	0
2	Worst-case tco	N/A	None	8.142 ns	ff1[8]q	out_cout	module_clock	--	0
3	Worst-case th	N/A	None	0.775 ns	cin	ff1[0]q	--	module_clock	0
4	Clock Setup: 'module_clock'	N/A	None	Restricted to 420.17 MHz (period = 2.380 ns)	ff1[8]q	ff1[7]q	module_clock	module_clock	0
5	Total number of failed paths								0

***Fig7**: Timing Analyzer Summary*

The Figure 7 shows the Timing Analysis summary for the DUT. It may obtain this state by applying the Timing Analyzer Summary View Section once again and It may verify the Device Components which are taken as DUT where each element is listed as required time, Actual time.

IV. CONCLUSION

The test patterns generation based on the behavioural functionalities of any DUT is processed. BBATG uses the device behaviour fault model and represents a circuit board as interconnection of devices. A behaviour of a device is a set of functions with timing relations on its in/out pins.

When used for a digital circuit board test generation, BBATG utilizes device behaviour libraries to drive behaviour error signals and sensitize paths. Thus the test vectors for effective fault coverage are generated. Data can be processed by a versatile UART interface implemented on FPGA and able to support any baud-rate in order to interface a USB converter.

After the implementation, simple test patterns are loaded to the memory by FSM using FPGA-equipped board. Based on that DUT stimulus is generated, tested and samples should be collected. The low-cost, easy-to-use and reconfigurable automatic test machine referred as FATE (FPGA-based ATE) is yet to be implemented.

The communication between the Laptop and FPGA can be done by the UART. If target FPGA board doesn't support an USB to UART converter, a serial cable communication is also available.

In this case, baud rate is selectable in a predefined range of discrete values. The systemic failures, with the consequent reduction of time-to-market, time-to-yield and time-to volume. Experimental results can be obtained using this test machine for the screening of digital part of complex SoCs confirmed its validity, at least for the addressed applications.

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