



ERODE SENGUNTHAR ENGINEERING COLLEGE

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

COURSE TITLE

**END-TO-END PRODUCT DEVELOPMENT USING
PRINTED CIRCUIT BOARD DESIGN**

PREPARED BY :

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1. INTRODUCTION TO PCB DESIGNING

1.a. CAD System

CAD or computer-aided design and drafting (CADD), is technology for design and technical documentation, which replaces manual drafting with an automated process. If you are a designer, drafter, architect or engineer, you have probably used 2D or 3D CAD programs such as Auto Cad or Auto Cad LT software. These widely used software programs can help you draft construction documentation, explore design ideas, visualize concepts through photo realistic renderings and simulate how a design performs in the real world.

Circuit CAD tools are the cornerstone of PCB design. These tools give you the capability to create schematics and a circuit board layout of your new product, but not all CAD features are created equal. Today's designers need to take a comprehensive approach to PCB design that includes mechanical design, simulation, and preparation for manufacturing. Your productivity stays high when your CAD tools are integrated with more advanced design features and your other design tools, and you can quickly design PCBs for advanced applications.

To handle the complex challenges of a complete design project, you need a complete circuit CAD system for PCB design. Altium Designer offers all these advantages and many more in a single program. You'll have everything you need to design your next PCB in a single program, including tools for MCAD collaboration in popular mechanical design applications.

The Role of Circuit CAD Tools in PCB Design

CAD circuit design tools in your PCB design software do more than just allow you to place components on a board outline. Simpler circuit CAD software will give you these capabilities, but not much else. PCB CAD tools should not be limited to component layout in 2D board designs. Working with more advanced board configurations like rigid-flex design takes CAD tools that link multiple boards into a single device. The best CAD tools create a link between multiple layers on your board, allowing routing through vias and within the inner layers. Modern CAD circuit design tools give you a full view of your device and allow you to approach your design holistically.

The best CAD software for PCB design will interface with a comprehensive set of design rules. These design rules govern the function of your routing features, simulation tools, and features for generating manufacturer deliverables. A rules-driven design engine in your circuit CAD software will automatically show you when you've created a rules violation, allowing you to fix any problems before you send your board off for manufacturing. A great CAD module forms the foundation for designing your next PCB, regardless of the application.

1.b. CNC drilling/milling machine

CNC drilling is a machining process that utilizes a rotating cutting tool to produce round holes in a stationary work piece. The holes are typically made to accommodate machine screws or bolts for assembly purposes. However, they can be used for aesthetic purposes depending on the design of the component.



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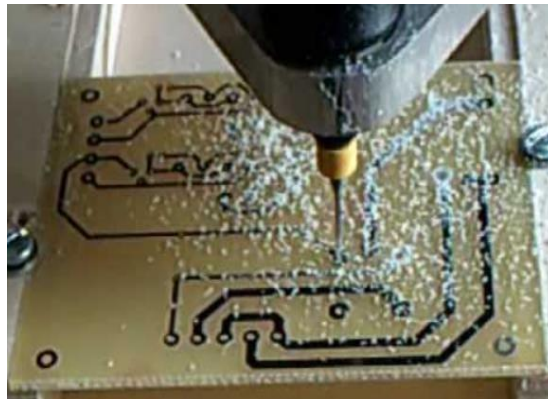
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- i. Creating the component design in CAD software
- ii. Converting the design into machine instructions
- iii. Loading the instructions to the CNC machine
- iv. Setting up the CNC machine
- v. Evaluating the component



1.c. Photo-plotter

A photo plotter is a specialized elector-opt-mechanical machine that exposes a latent image on a medium, usually high-contrast monochromatic (black-and-white) photographic film, using a light source under computer control. Once the film has been exposed, it must be processed before it is ready for use.

Photo plotters are used primarily for industrial production of printed circuit boards (PCB) and integrated circuit (IC) packaging. In the PCB industry, photo plotting is the first step of making photolithography masks for printed circuit boards. These masks are called photo plots and are limited in resolution by the technology in use; in 1998 photo-plots with resolvable details of 2.5 μm or more were possible. Integrated circuits are made in a similar fashion utilizing photomasks with sub-micrometer feature sizes; photo masks are traditionally made by photo reducing photo plotter output.

1.d. Film Developer

Operates machine to develop still or motion-picture film: Pulls reel of motion-picture film or rack of film strips through trapdoor into darkroom. Examines film to determine type processing required, utilizing knowledge of film developing techniques.

In the processing of photographic films, plates or papers, the film developer (or just developer) is one or more chemicals that convert the latent image to a visible image. Developing agents achieve this conversion by reducing the silver halides, which are pale-colored, into silver metal, which is black when in the form of fine particles.

1.e. Brushing Machine

Brushing machines create a uniform work piece surface finish after undergoing turning, punching, milling, or machining processes. Work-pieces include wires, metal discs, pipes, tubes, and sheet metal blanks. Removal of dust or impurities is a secondary application of brushing machines. Brushing machines are employed in polishing, edge radiating, debarring, and honing



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applications. They are also used for processing agricultural products. They are effective in cleaning and polishing seeds or grains and removing skins from nuts.



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Uniform copper abrasion due to automatic adjustment of brushes Virtually constant cutting Speed Evenly brushed surface due to bi-directional operation of oscillating brushes Brushing module, cleaning module and ultrasonic device can be combined. The standard brushing machine is primarily used for the deburring and cleaning of drilled PCBs. Thin inner layers are brushed bi-directionally at a high oscillating frequency. The distance between the brushes and the panel is automatically adjustable. The copper centrifuge “Cecumat” removes the copper abrasion from the rinsing water.

2. FABRICATION OF PCB

2.a. Base material cutting

The PCB cutter can be described as a particular kind of cutting tool that serves various PCB types. The cutter will cut PCBs varying in thickness from phenolic boards that are 2mm thick to thin aluminum and copper boards. A strong handle is another element of the PCB cutter. PCB cutters provide precise, clean cuts including an original design. To avoid any mishaps when working with the PCB cutter, you are advised to fasten a safety guard made of plastic. Grade steel that is hardened comprises the lower as well as top shearing blocks. Hardened alloy makes up these blocks. They are strong as a result. A quality PCB cutter provides a clear, exact cut. To ensure accurate cutting, the user fastens a ruler onto that cutting platform.



Detaching of the printed circuit boards from the base material is a task that is performed by the LPKF ProtoMats or ProtoLasers. One or more boards are arranged on a base material and separated using a milling tool or an LPKF ProtoLaser. An extensive parameter/tool library delivers the settings for the most important materials. Creation of panels is also optimally supported by the LPKF software.



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The operation of a cutting machine typically involves feeding the core material onto the machine, aligning it, and then cutting it to the desired length and diameter using a cutting blade or saw. Some **core-cutting** machines can also perform other functions, such as slitting, rewinding, and perforating.

Cutting can be described as a technique that includes physically dividing a thing into its component pieces. Saws and knives are frequently utilized. However, PCB cutting often involves the use of the PCB cutter. When the overall tension of these cutting tools exceeds the maximum strength of that thing being cut, then cutting occurs. A PCB's cutting procedure aids in producing the right board dimensions. Copper lines are another component of the circuit boards. A big PCB piece can be divided up into smaller ones. To get a good cut, you'll need a reliable PCB cutter, though. Various PCB cutting instruments are available for use during the process of cutting. A vital step before PCB cutting is preparation. The ultimate objective of the cutting of the PCB should be to produce clear and accurate cuts. As a result, it's crucial to cleanly wipe the PCB using a very clean cloth.

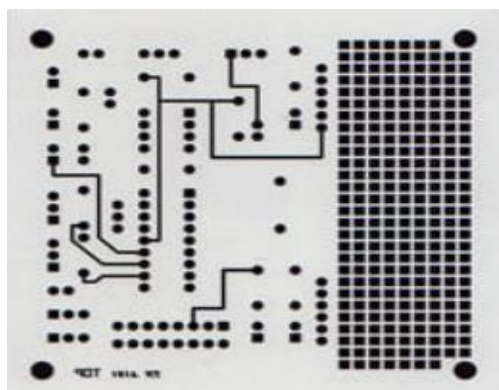
2.b. Through hole plating

The point of plated through holes is so you can use both sides of your printed circuit board and connect to other layers of the board. The plating on the through holes is copper, a conductor, so it allows electrical conductivity to travel through the board.

Non-plated through holes do not have conductivity, so if you use them, you can only have useful copper tracks on one side of the board. You cannot connect to the other side or other boards because there is no way for electricity to travel through. You can use non-plated through holes either to affix a PCB to its operational location or to mount components, but not to connect to other boards or the other side of the board.

2.c. Layer film generation

Films for all of the copper and solder mask layers are made from photographically exposed Mylar. We generate these films from your design files, creating an exact (1:1) film representation of your design. When **Gerber files** are submitted, each individual **Gerber file** represents one layer of the **PCB Board**. This step is an electrochemical process which builds copper thickness into the holes and onto the surface of the PCB. Once the copper thickness is built up on the circuitry and in the holes, we plate an additional layer of tin to the exposed surface. This tin will protect the plated copper during the etching process and be later removed.





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2.d. Laminating

Lamination describes the process of building up successive layers of a material and binding those layers to strengthen, protect and waterproof a variety of substances. The lamination process is an important step in building up a printed circuit board (PCB). Circuit board manufacturers use lamination to ensure copper does not inadvertently conduct current or a signal. Copper is laminated onto the substrate—the physical canvas to which all components of a printed circuit board assembly (PCBA) are attached.

Types of PCB Lamination

- a) multilayer PCBA
- b) Teflon (PTFE) microwave laminates
- c) Sequential lamination

Printed circuit boards (PCBs) are an essential component in electronic devices, ranging from simple devices like calculators to complex systems like computers and smartphones. A PCB is a flat board made of a non-conductive substrate material with conductive pathways and components attached to it. One of the critical components of a PCB is the **PCB laminate**.

A Printed Circuit Board finds its genesis in the **PCB laminate**. A Laminate is a non-conductive substrate, or the base material used to create PCBs. It is a composite material made up of layers of fiberglass cloth that have been impregnated with an epoxy resin. The fiberglass layers are stacked on top of each other and pressed together with heat and pressure to create a solid sheet of material. The result is a rigid, flat board that can support the conductive pathways and components that make up the PCB.

2.e. Spray developing

Three acrylic plastic tanks with drain trip, mounted in a frame made of PVC profiles Self-lance motors (DC-voltage) Adjustable plate holder for receiving the printed circuit boards Glass heater mounted inside the etching tank Control unit with switched power supply for motors Drip pan made of PVC plastic, glass thermometer Main feature of the Spray Etching Devices are the spray tubes. They are moved by an powerful DC-motor and while turning the etching liquid will be sprayed evenly onto the etched surface. Thus a fast and accurate etching is achieved.





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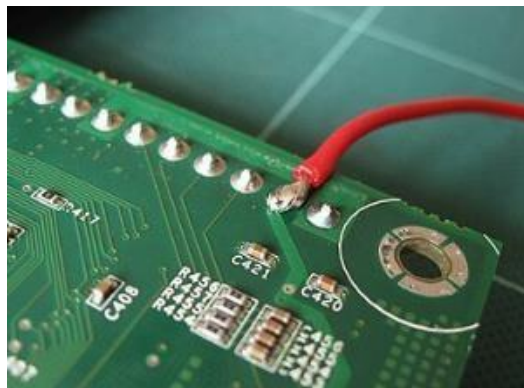


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2.f. Solder resist masking

Solder mask, solder stop mask or solder resist is a thin lacquer-like layer of polymer that is usually applied to the copper traces of a printed circuit board (PCB) for protection against oxidation and to prevent solder bridges from forming between closely spaced solder pads. A **solder bridge** is an unintended electrical connection between two conductors by means of a small blob of solder. PCBs use solder masks to prevent this from happening. Solder mask is not always used for hand soldered assemblies, but is essential for mass-produced boards that are soldered automatically using reflow or wave soldering techniques.

Solder mask comes in different media depending upon the demands of the application. The lowest-cost solder mask is epoxy liquid that is silkscreened through the pattern onto the PCB. Other types are the liquid photoimageable solder mask (LPSM or LPI) inks and dry-film photoimageable solder mask (DFSM). LPSM can be silkscreened or sprayed on the PCB, exposed to the pattern and developed to provide openings in the pattern for parts to be soldered to the copper pads.



(Printed circuit board with green solder mask coating)

3. DESIGN FOR TESTABILITY

3.a. Design for Testability

Designing for testability in a PCB design (DFT) is a critical step in the design for manufacturability (DFM) process. This critical concept boils down to developing a consistent product for the lowest possible manufacturing cost while maintaining an acceptable rate of defects. Considering testability throughout the PCB Design involves outlining the creation process to understand test point requirements and isolate faults quickly. Both for manufacturing errors and component failures, DFT is paramount in designing for profitability. In this paper, we will explore DFT in depth, and specifically look at in-circuit testing (ICT).

ICT testing can detect a number of defects in Printed Circuit Boards, on both the manufacturing and component fronts. There are two types of ICT test systems. One system utilizes a test fixture, which clamshells the printed circuit assembly (PCA) under test and probes various nets to perform the test. The second is a flying probe test, where the probes are controlled by a computer system to make electrical contact with specific nets of the PCA under test. Some example PCB design tests check for shorts/opens, missing components, components placed with the wrong



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polarization or even the bad value, and a number of other aspects.



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3.b. Ad-hoc design

Ad hoc describes a process not planned and can be an adequate description of how some hardware designers and electrical engineer's work. The truth is an ad-hoc design process has merit. Many designers and engineers will use this type of process to get them unstuck when confronted with a problem. However, when is it more advantageous to adopt an ad-hoc design process versus a structured approach? Before we can decide, it's important to understand the benefits and drawbacks of using either in our own work.

The structured design process has 5 main phases:

1. Problem Analysis
2. Problem Modeling/Design
3. Development on that Design or Model
4. Testing & Documentation
5. Product Deployment

An ad hoc approach responds to the realities of product design. Rarely within your work as a hardware designer or electrical engineer will you be given a comprehensive set of system requirements and constraints needed to design a product. Thus, having the ability to switch to an ad hoc design style is necessary. Doing so means you can adapt, amend, and adopt elements of it to suit your purpose.

Believe it or not, an ad hoc approach does use a structure, however its structure isn't predetermined. This allows for more flexibility throughout the design process, especially if you happen to be working on a poorly defined task, or don't have specified requirements and constraints. While it is never advisable to allow the overall design process to be completely ad hoc, implementing this approach when confronted with a singular problem (or series of related problems) within the overall design process will help you quickly find workable solutions; allowing you to fill in the missing details as you go.

3.c. Generic scan based design

The control-ability and observability can be enhanced by providing more accessible logic nodes with use of additional primary input lines and multiplexers. However, the use of additional I/O pins can be costly not only for chip fabrication but also for packaging. A popular alternative is to use scan registers with both shift and parallel load capabilities.

The boundary scan test method is also used for testing printed circuit boards (PCBs) and multichip modules (MCMs) carrying multiple chips. Shift registers are placed in each chip close to I/O pins in order to form a chain around the board for testing. With successful implementation of the boundary scan method, a simpler tester can be used for PCB testing.

On the negative side, scan design uses more complex latches, flip-flops, I/O pins, and interconnect wires and, thus, requires more chip area. The testing time per test pattern is also increased due to shift time in long registers. The level sensitivity is to ensure that the sequential circuit response is independent of the transient characteristics of the circuit, such as the component and wire delays. Thus, LSSD removes hazards and races. Its ATPG is also simplified since tests have to be generated only for the combinational part of the circuit.



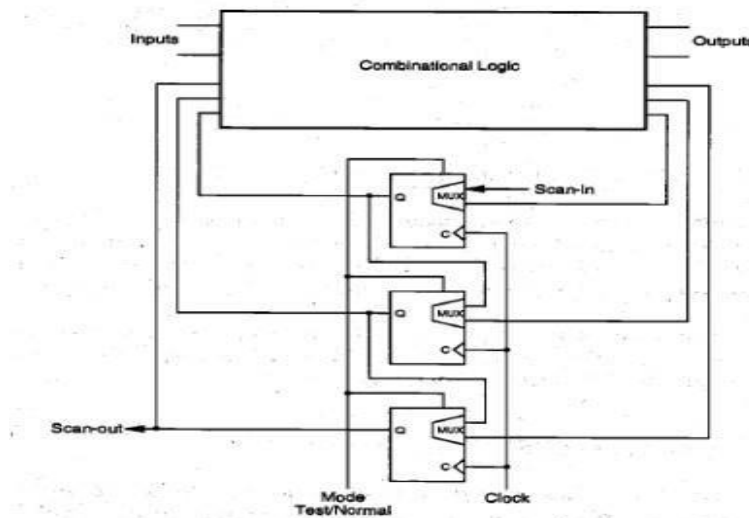
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3.d. Classical scan based design

The storage cells in scan design can be implemented using edge-triggered D flipflops, master-slave flip-flops, or level-sensitive latches controlled by complementary clock signals to ensure race-free operation. Figure 2 shows a scan-based design of an edge-triggered D flip-flop. In large high-speed circuits, optimizing a single clock signal for skews, etc., both for normal operation and for shift operation, is difficult. To overcome this difficulty, two separate clocks, one for normal operation and one for shift operation, are used.

Since the shift operation does not have to be performed at the target speed, its clock is much less constrained. In the test mode, the scan-in signal is clocked into the scan path, and the output of the last stage latch is scanned out. In the normal mode, the scan-in path is disabled and the circuit functions as a sequential circuit.

An important approach among scan-based designs is the level sensitive scan design (LSSD), which incorporates both the level sensitivity and the scan path approach using shift registers. The level sensitivity is to ensure that the sequential circuit response is independent of the transient characteristics of the circuit, such as the component and wire delays. Thus, LSSD removes hazards and races. Its ATPG is also simplified since tests have to be generated only for the combinational part of the circuit.

3.e. Automatic test equipment

Automatic test equipment or **automated test equipment (ATE)** is any apparatus that performs tests on a device, known as the device under test (DUT), equipment under test (EUT) or unit under test (UT), using automation to quickly perform measurements and evaluate the test results. An ATE can be a simple computer-controlled digital multimeter, or a complicated system containing dozens of complex test instruments (real or simulated electronic test equipment) capable of automatically testing and diagnosing faults in sophisticated electronic packaged parts or on wafer testing, including system on chips and integrated circuits.

Automated test equipment (ATE) is computer-controlled test and measurement equipment that allows for testing with minimal human interaction. The tested devices are referred to as a device under test (DUT). The advantages of this kind of testing include reducing testing time, repeatability, and cost efficiency in high volume. The chief disadvantages are the upfront costs for programming



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and setup.



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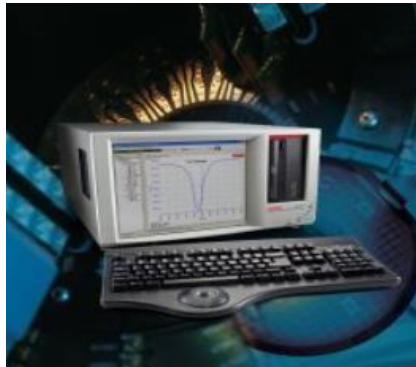
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Automated test equipment can test printed circuit boards, interconnections, and verifications. They are commonly used in wireless communication and radar. Simple ATEs include volt-ohm meters that measure resistance and voltages in PCs; complex ATE systems have several mechanisms that automatically run high-level electronic diagnostics.



4. SELF TEST AND TEST ALGORITHMS BUILD

4.a. In Self Test

Built-in self-test, or BIST, is a structural test method that adds logic to an IC which allows the IC to periodically test its own operation. Two major types are memory BIST and logic BIST. Memory BIST, or MBIST, generates patterns to the memory and reads them to log any defects. Memory BIST also consists of a repair and redundancy capability. In this technology, each die has spare circuits. If a circuit is bad, the defective circuit is disconnected and replaced with a good one. Memory BIST is also used to obtain known good memory stacks for 2.5D/3D devices.

Logic BIST, or LBIST, uses a Pseudo-Random Pattern Generator to generate input patterns that are applied to internal scan chains. The results are compressed into a signature. Then, a Multi-Input Signature Register determines whether the signature is correct or not to tell if all tests passed. LBIST is most often used for safety-critical and high-reliability applications such as automotive. However, LBIST requires a very clean design with no unknown states, as this would corrupt operation. This means much more stringent design and test rules and insertion of LBIST is more complex than scan. LBIST also incurs significant overhead in timing, area, and power.

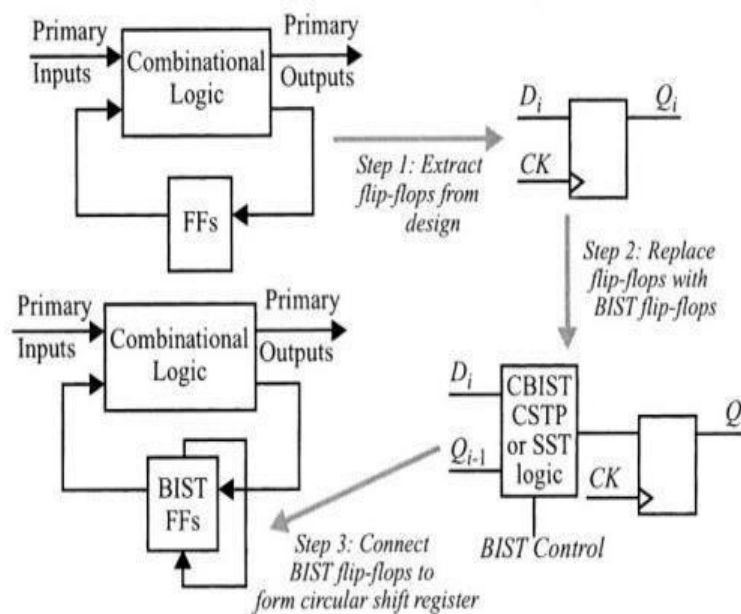
4.b. Test pattern generation for BIST

A Test Pattern Generator (TPG) is used for generating different test patterns in Built-In Self-Test (BIST) schemes. This work generates Multiple Single Input Change (MSIC) vectors in a pattern, applies each vector to a scan chain as an SIC vector. A MSIC-TPG and Accumulator based TPG are designed and developed a reconfigurable Johnson counter and a scalable SIC counter to generate a class of minimum transition sequences. The Test Pattern Generator is flexible to both the test-per-clock and the test-per-scan schemes. A theory is also developed to represent and analyze the sequences and to extract a class of MSIC sequences. Analysis results show that the produced Multiple Single Input Change sequences have the favorable features of uniform distribution and low input transition density.



4.c. Circular BIST

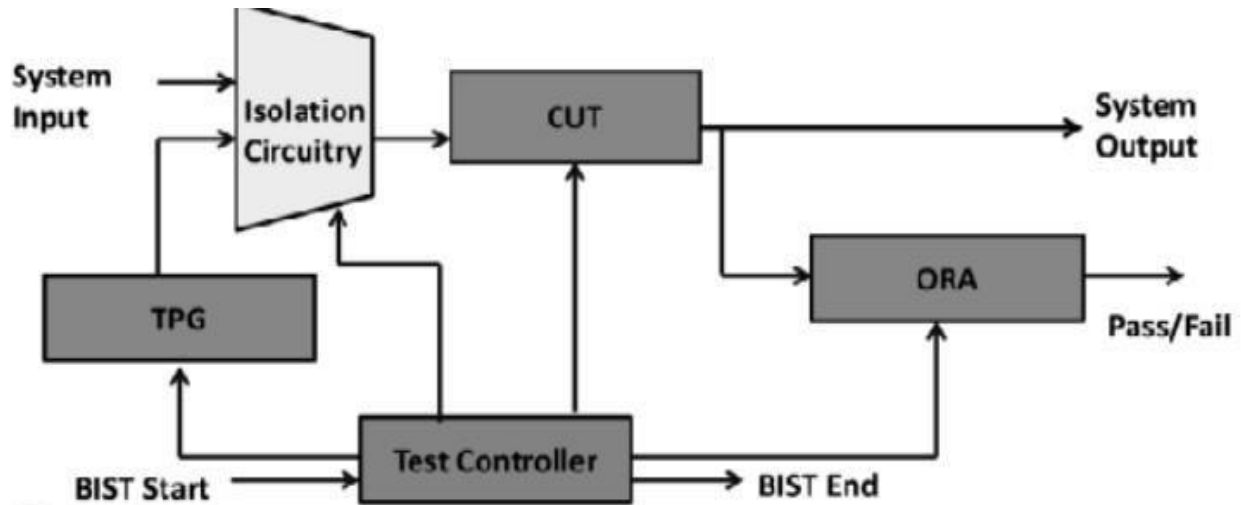
BIST is a method of testing a circuit by embedding test logic within the circuit itself. The test logic can be either hardware or software, depending on the design and implementation of the circuit. The Circular BIST approach forms a large MISR-like structure from the existing flipflops in the CUT. In the BIST mode of operation, the output responses of the CUT are linearly combined (via exclusive-OR gates) with the contents of the circular BIST chain while the resulting contents of the chain are used as the next test pattern to the CUT. Though the circular BIST chain performs output response compaction in a manner similar to a MISR used for signature analysis, there is no primitive characteristic polynomial associated with the circular BIST chain.



As a result, there is no need to worry about finding primitive polynomials for circular BIST chains of varying lengths. An alternative way of looking at the BIST approach is to construct one large BILBO from all flip-flops in the CUT using as the characteristic polynomial. The flip-flops are augmented with additional logic to operate in a BIST mode to test the combinational logic as well as the flipflops themselves. The primary motivation for the development of Circular BIST was a direct result of the introduction of a behavioral model synthesis system since the designer was removed from intimate knowledge of the gate-level implementation of the synthesized design.

4.d. BIST Architectures

BIST is a DFT approach that involves inserting additional hardware capabilities into integrated circuits to allow them to undertake self-testing, lowering reliance on an external ATE and hence reducing testing expense. The BIST principle may be used for almost any type of circuit. BIST is also a solution for testing circuits that do not have direct connections to external pins, such as embedded memory used by devices.



LBIST is most often used for safety-critical and high-reliability applications such as automotive. However, LBIST requires a very clean design with no unknown states, as this would corrupt operation. This means much more stringent design and test rules and insertion of LBIST is more complex than scan. LBIST also incurs significant overhead in timing, area, and power.

BIST stands for Built-In Self-Test, a DFT technique used in VLSI to test the functionality of integrated circuits (ICs) during the manufacturing process and throughout the product's life. BIST involves embedding self-test circuitry within the IC design, which can be activated to perform various tests on the circuit. This circuitry can be designed to test various aspects of the IC, such as logic gates, memory, and communication interfaces. BIST can also be used to test for various types of faults, such as stuck-at faults, transition faults, and delay faults.

4.e. Testable Memory Design

Design for Testability (DFT) techniques are effective ways to reduce FBT test programming complexity. This is accomplished by improving Observability and Controllability attributes. This often implies adding test points, but access improvements can be gained from many design activities. We examine some failure modes and show that many of them need to be tested with FBT. Still others require DFT to enable FBT to detect them. We suggest a more pro-active approach that purposely places boundary scan access to internal circuit locations necessary or instrumental for better tests. This approach requires test and design collaboration during the design process. Designers must understand the test requirements early enough to add the necessary access points so that path sensitization and diagnostic attributes are also improved.

Design verification tests (DVTs) are performed by designers before the product is manufactured. Though the tests are long and complex, there is no need to automate them since they will be run only once. They include environmental stress screening (ESS) tests that provide information about the likelihood that the product will continue working properly for some time and under certain environmental strain. While the tests functionally exercise the unit under test (UUT), as we will discuss in greater detail, this is not a functional board test (FBT) that is the subject of this paper.



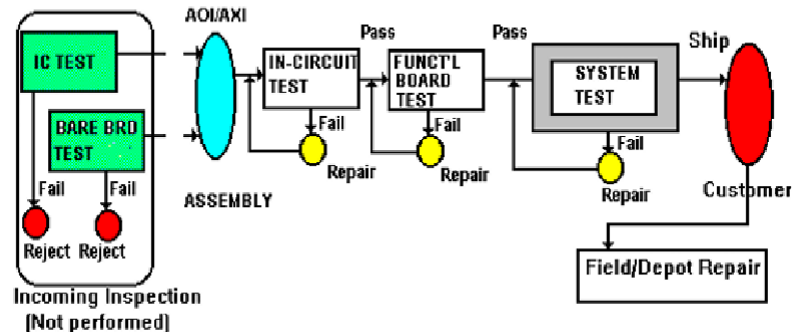
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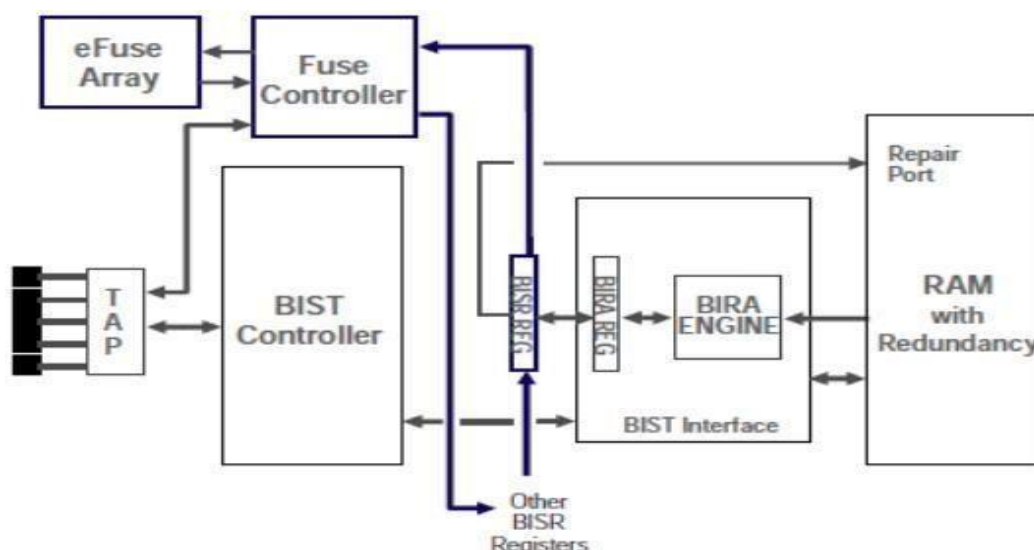


When complex measurements are needed to ensure functionality, increased cost of both test equipment price and lack of availability may be limiting factors. Designs can usually accommodate existing ATEs and test set ups, provided this is done during the design process. We propose a parallel design and test engineering activity. We argue that while the potential benefits are great, the added costs are insignificantly small.

4.f. Test generation for Embedded RAMs

Early embedded memories usually were six-transistor static RAMs that did not require refresh; consequently, test requirements were modest. However, the newest processor designs often incorporate smaller, less stable, four-transistor SRAMs or even single-transistor dynamic RAMs. Address decoders must be stressed at the highest operating speed to confirm that they can switch from any address to any other address at maximum frequency.

Sense amplifiers may be presented with a signal that resembles noise. The test requirement is to distinguish a high from a low. A worst-case test might place a low or high on the most distant bit line, with a minimum time to pre-charge from the opposite state. Specific algorithmic patterns can be applied to test for sense-amplifier/bit-line charging problems.





Today's embedded memories have one of three access modes that can be used for testing: interleaved access through a logic address/data bus, direct access to the RAM through a test mode, or serial access through a test port. The serial-access mode may have the least negative impact on device performance, but it is the most challenging for test.

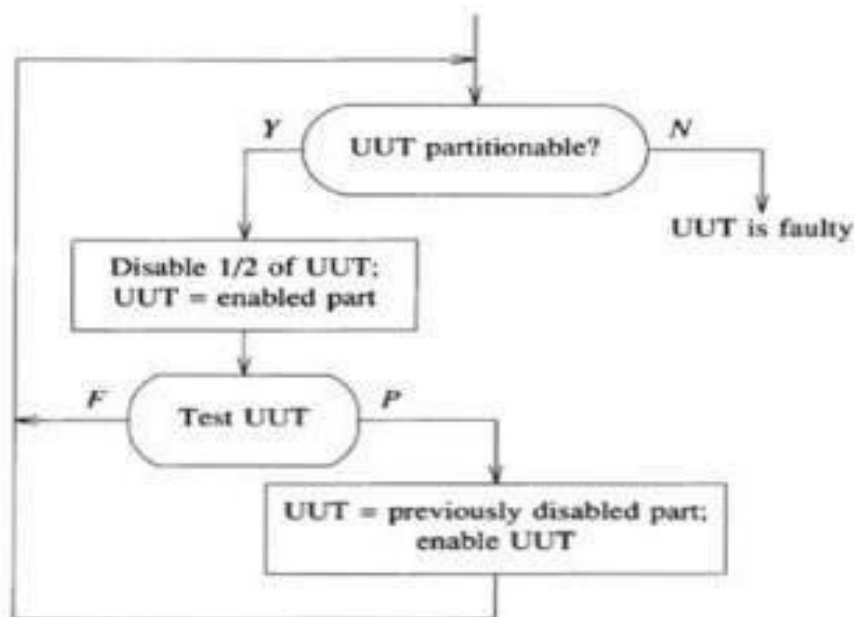
A test system must present full algorithmic patterns to the device, without restriction of the address and data mix. Failure data must be stored and presented in a way that preserves the address and type of each failure and the test conditions under which it occurred, even if data is pipelined. Several bits of memory address come out of the pattern generator in parallel, interspersed with data bits. They must be presented to the memory through one pin.

5. FAULT DIAGNOSIS LOGIC LEVEL DIAGNOSIS

5.a. Diagnosis by UUT reduction

A unit under test (UUT) fails when its observed behavior is different from its expected behavior. Diagnosis consists of locating the physical fault(s) in a structural model of the UUT. The degree of accuracy to which faults can be located is called diagnostic resolution. Functionally equivalent faults (FEF) cannot be distinguished. The partition of all faults into distinct subsets of FEF defines the maximal fault resolution. A test that achieves the maximal fault resolution is said to be a complete fault-location test.

Repairing the UUT often consists of substituting one of its replaceable units (RU) referred as a faulty RU, rather than in an accurate identification of the real fault inside an RU. We characterize this process by RU resolution. Suppose that the results of the test do not allow to distinguish between two suspected RUs U1 and U2. We could replace now one of these RUs, say U1 with a good RU, and return to the test experiment. If the new results are correct, the faulty RU was the replaced one; otherwise, it is the remaining one U2. This type of procedure we call sequential diagnosis procedure.





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The diagnosis process is often hierarchical, carried out as a top-down process (with a system operating in the field) or bottom-up process (during the fabrication of the system).

In the top-down approach (system → boards → ICs) first-level diagnosis may deal with "large" RUs like boards called also field-replaceable units. The faulty board is then tested in a maintenance center to locate the faulty component (IC) on the board. Accurate location of faults inside a faulty IC may be also useful for improving its manufacturing process.

In the bottom-up approach (IC → boards → stem) a higher level is assembled only from components already tested at a lower level. This is done to minimize the cost of diagnosis and repair, which increases significantly with the level at which the faults are detected.

5.b. Fault Diagnosis for Combinational Circuits

A method is developed for obtaining a highly compressed fault table for two-level combinational circuits. A set of operations is defined through which the minimal test set for detecting stuck-at faults is obtained from the compressed fault table. The method is equally suitable for sum of products form or product of sums form realization of logic functions and generates the test set directly from the algebraic expression of the logic function.

As transistors become increasingly smaller and faster and noise margins become tighter, circuits and chip specially microprocessors tend to become more vulnerable to permanent and transient hardware faults. Most microprocessor designers focus on protecting memory elements among other parts of microprocessors against hardware faults through adding redundant error-correcting bits such as parity bits. However, the rate of soft errors in combinational parts of microprocessors is considered as important as in sequential parts such as memory elements nowadays. The reason is that advances in scaling technology have led to reduced electrical masking. This paper proposes and evaluates a logic level fault-tolerant method based on parity for designing combinational circuits. Experimental results on a full adder circuit show that the proposed method makes the circuit fault-tolerant with less overhead in comparison with traditional methods. It will also be demonstrated that our proposed method enables the traditional TMR method to detect multiple faults in addition to single fault masking. Keywords: Soft Error, Transient Fault, Fault-Tolerance, Combinational Circuits, Full Adder.

Fault-tolerance techniques are generally accomplished by using redundancy in hardware, software, time and information. In this paper, we have used hardware redundancy in combinational circuits. Some of the fault-tolerant hardware methods are Duplication With Comparison (DWC) in which the module is duplicated, results are compared and if one mismatch occurs, an error flag is raised.

Using these methods, triple modules and voting circuits are implemented onto an Application Specific Integrated Circuit (ASIC) or a Field-Programmable Gate Array (FPGA). When a fault occurs, the voting circuit neglects the value of a faulty module and takes a correct value of the other two non-faulty modules. These methods come with high area and power dissipation penalties and are inherently proposed for detecting or masking a single fault. This paper is organized as follows: section 2 presents a brief background of fault sensitivity in combinational and sequential circuits; in section 3 we proposed a new fault-tolerance technique in combinational circuits. The diagnosis process is often hierarchical, carried out as a top-down process (with a system operating in the field) or bottom-up process (during the fabrication of the system). In the top-down approach first-level diagnosis may deal with "large" RUs like boards called also field-replaceable units.



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5.c. Self-checking design

PCB assembly testing methods are an integral part of the manufacturing process. Reputable electronics contract manufacturers (ECMs) offer a variety of PCB testing methods, but the seven main types include:

1. In-circuit testing
2. Flying probe testing
3. Automated optical inspection (AOI)
4. Burn-in testing
5. X-Ray inspection
6. Functional testing
7. Other functional testing (solderability, contamination, and more)

Here's a primer on the most important types of PCB testing. This should prepare you better for discussions with your ECM:

7 TYPES OF PCB TESTING METHODS

1. IN-CIRCUIT TESTING

In-circuit testing (ICT) is the most robust type of PCB testing in existence. The high price reflects that -- tens of thousands of dollars, though the cost will depend on board and fixture size, among other factors.

An ICT, also known as a bed-of-nails test, **powers up and actuates the individual circuitry** on the board. In most cases, the test is designed for 100% coverage, but you'll get closer to 85-90% coverage. The nice thing about ICT is that the 85-90% you get is totally free of human error.

2. FLYING PROBE TESTING

Flying probe testing is a tried-and-true option that's **less expensive** than in-circuit testing. It's a nonpowered type of test that checks for:

- Opens
- Shorts
- Resistance
- Capacitance
- Inductance
- Diode issues

The test works through the use of needles attached to a probe on an x-y grid obtained from basic CAD. Your ECM programs coordinates to match the circuit board and then runs the program.

3. AUTOMATED OPTICAL INSPECTION (AOI)

AOI uses either a single 2D camera or two 3D cameras to take photos of the PCB. The program then compares the photos of your board to a detailed schematic. If there is a board that does not match the schematic to a certain degree, the board is flagged for inspection by a technician.



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AOI can be **useful for detecting issues early** to ensure production is shut down ASAP. However, it does not power up the board and may not have 100% coverage for all part types. Never rely solely on an automated optical inspection. AOI should be used in conjunction with another test. Some of our favorite combos are:

- AOI and flying probe
- AOI and in-circuit test (ICT)
- AOI and functional testing

4. BURN-IN TESTING

As the name suggests, burn-in testing is a more intense type of testing for PCBs. It's designed to detect early failures and establish load capacity. Because of its intensity, burn-in testing **can be destructive to the parts** being tested.

Burn-in testing pushes power through your electronics, usually at its maximum-specified capacity. The power is run through the board continuously for 48 to 168 hours. If a board fails, it is known as an infant mortality. For military or medical applications, boards with high infant mortality are clearly not ideal.

5. X-RAY INSPECTION

Also referred to as AXI, this type of "testing" is really more of an inspection tool, at least for most ECMs. During this test, an X-ray technician is able to locate defects early during the manufacturing process by viewing:

- Solder connections
- Internal traces
- Barrels

X-ray testing **can check elements that are usually hidden** from view, such as connections and ball grid array packages with solder joints underneath the chip package. While this check can be very useful, it does require trained, experienced operators.

6. FUNCTIONAL TESTING

There are customers who do like a good, old-fashioned functional test. Your ECM uses this to **verify that the product will power up**. This test does require a few things:

- External pieces of equipment
- Fixtures
- Requirements for UL, MSHA, and other standards

This functional test and its parameters are usually provided by the customer. Some ECMs can help develop and design such a test.



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7. OTHER FUNCTIONAL TESTS

There are other types of functional tests that can be used to check your PCB, depending on the circumstances. A PCB functional test verifies a PCB's behavior **in the product's end-use environment**. The requirements of a functional test, its development, and procedures can vary greatly by PCB and end product. Other PCB assembly testing types include:

- **Solderability test:** Ensures surface sturdiness and increases chances of forming a reliable solder joint
- **PCB contamination testing:** Detects bulk ionics that can contaminate your board, causing corrosion and other issues
- **Micro-sectioning analysis:** Investigates defects, opens, shorts, and other failures
- **Time-domain reflectometer (TDR):** Finds failures in high-frequency boards,
- **Peel test:** Finds the measure of strength required to peel the laminate from the board
- **Solder float test:** Determines the level of thermal stress a PCB's holes can resist.

5.d. System Level Diagnosis

PCB testing and inspection cover a wide variety of printed circuit board testing methods that check if a PCB meets standards. Some of these PCB standards revolve around ensuring the PCB functions properly according to a project's specifications and that it doesn't have any defects. Electric board testers and other circuit board testing methods are used to conduct these inspections and PCB tests. Circuit board testing procedures evaluate several components of PCBs. These components are analyzed in detail to ensure their quality. The primary components tested can be found below:

- **Lamination:** Lamination quality is essential to the lifespan of a PCB — peeling laminate can cause issues in the final functionality of a board. Generally, tests on lamination will look at the laminate's resistance to peeling by force or application of heat.
- **Copper plating:** The copper foil on a PCB is laminated to the board to provide conductivity, but the quality of the copper is often tested, with tensile strength and elongation analyzed in detail.
- **Solderability:** Testing the solderability of a material is essential for a functioning PCB since it ensures that components can be attached firmly to the board and prevents soldering defects in the final product. The most commonly analyzed factor is wetting, which refers to how well a surface accepts liquid solder.
- **Hole wall quality:** Hole wall quality is another essential part of a PCB, ensuring that the hole walls will not crack or delaminate when the PCB goes into the field. Hole walls are generally analyzed in environments with cycling and quickly changing temperatures to see how well



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they react to thermal stress.



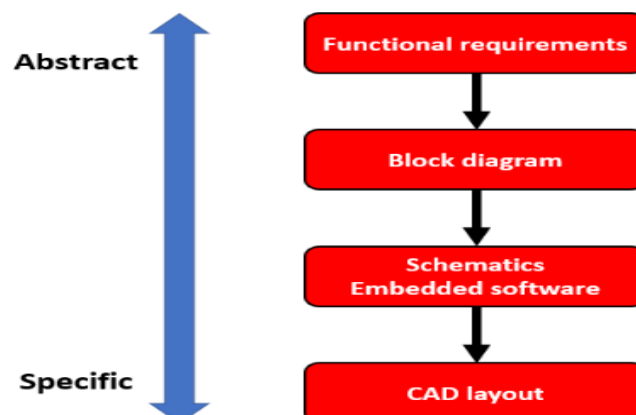
- **Electrical:** Electrical conductivity is essential for any PCB, so the ability of a PCB to pass electric currents with minimal leakage is a common test.
- **Environment:** Many PCBs operate in humid environments, so a common test for PCBs is for water absorption. In these types of tests, the PCB is weighed before and after being put in a humid environment, and any significant weight change results in a failing grade.
- **Cleanliness:** Cleanliness for PCBs is the ability to resist environmental factors like corrosion and humidity. Generally, these tests include analyzing PCBs before and after they're put through varying environmental conditions.

Most of these factors are analyzed in early materials testing and environmental tests. However, factors like electrical conductivity and general functionality are analyzed with various methods and equipment. Several PCB testing methods are available, and no single one will catch every problem or meet the requirements of every designer. Each testing method should be considered closely to determine if it meets the specific needs of your manufacturing environment.

5.e. Abstraction hierarchy

Taking design requirements and forming a functional block diagram for a new product is the core idea in using system modeling and abstraction levels for electronics development. Implementing a systems-level design process and successfully progressing towards a PCB layout requires properly completing the first step: gathering functional requirements for your new product. This will form the foundation for your new product and allow you to define a block diagram that represents your system's functionality.

One important point to consider in design reuse as part of system-level design and modeling is component sourcing. If you're reusing an old functional block in a new system, it's important to check that the components in that block are available on the market in the quantities you need. You should also check whether these required components will go obsolete as this will interfere with successive manufacturing runs for your new product.





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If you've taken a modular approach to designing schematics for each functional block, you can link them together in a hierarchical fashion, and your system will start to nicely reflect the intended functionality you created in your block diagram.

Once you've captured your schematics in a PCB layout, arranged components, and routed your board, you're ready for the final design verification steps. This can include post-layout simulations, batch design rule checks, and DFM checks. If you're designing an embedded system, software development will need to proceed alongside the hardware development portion of the project. There is no perfect time to start coding software for a new product, but the software functionality should be defined at the block diagram level alongside the hardware functionality.

5.f. Fault trees

Fault trees use a top-down approach to discover the cause of a failure. Each graphical fault tree consists of two different types of events and logic gates that connect events. Boolean logic describes the logical relationship between low-level, undesired system states—or basic events—that can cause the failure of a system, or top event. An engineering team can use one or more fault trees to show combinations of failure states of a component. We can use the symbols shown in the following table to build a map that shows how the events unfold.

Because FTA works from the top-down, we begin the process by defining a primary failure. The primary failure becomes the top event in a fault tree. From there, we use available technical information to identify basic events and logic gates to show the relationship between the primary event and the basic events. Then, we follow the same process to identify other basic events and show the logical relationships to the primary event. Each logic gate represents a fault state. While the next figure shows a small sample of an FTA, actual fault trees have many branches and events.



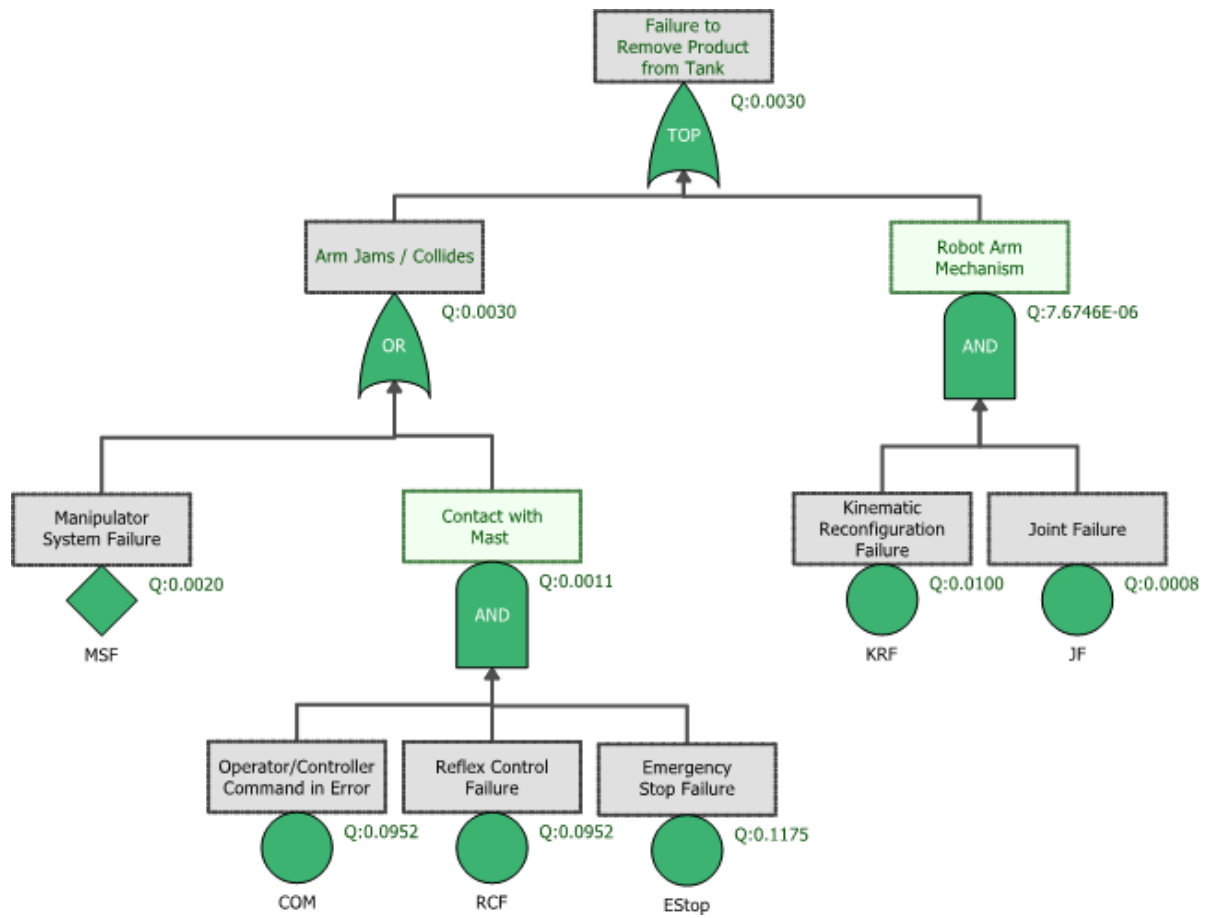
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The analysis portion of FTA begins with cut sets—or a set of combined basic events that can cause the primary event. As the analysis continues, the cut sets reduce to minimal cut sets or the smallest number of events that can cause the primary event. Every analysis can conclude with a probability calculation for the minimal cut set. After a team assigns probabilities to each basic event, they can use reliability and probability equations to determine the reliability of the system or the probability of the top event occurring.

Failure Mode and Effects Analysis

As the name implies, Failure Mode and Effects Analysis (FMEA) determines possible failure modes and considers the level of impact of those failure modes on the performance of a system. In contrast to the FTA approach that only studies critical or safety systems, FMEA considers all potential failure modes and then identifies, evaluates, and prioritizes the possible failures. FMEA works well during the design stages of a circuit or product, and provides value by showing possible operational challenges or by eliminating cascading problems.

Within the FMEA approach, every failure mode receives a risk score based on severity (S), occurrence (O), and detectability (D), and receives a Risk Priority Number that equals the product of the three factors. In most instances, design teams will continue analyzing failure modes that have an RPN above 100 and take corrective actions. The FMEA approach also allows teams to assess the impact of a failure on the entire system operation.

5.g. Fuzzy logic

Fuzzy logic and artificial neural network are integrated into the fuzzy back-propagation network (FBPN) for printed circuit board industry. The fuzzy back propagation network is constructed to incorporate production-control expert judgments in enhancing the model's performance. Parameters chosen as inputs to the FBPN are no longer considered as of equal importance, but some sales managers and production control experts are requested to express their opinions about the importance of each input parameter in predicting the sales with linguistic terms, which can be converted into pre-specified fuzzy numbers, aggregated and corresponding input parameters when fed into the FBPN. The proposed system is evaluated through the real life data provided by a printed circuit board company. Model evaluation results for research indicate that the Fuzzy back-propagation outperforms the other three different forecasting models in MAPE.